AndesCore™ AX66 Processor

Superscalar Out-of-Order Exec. Multicore Cluster

Benefit

Performance

- AndeStar™ V5 Instruction Set Architecture (ISA), compliant to RISC-V technology
- Andes extensions, architected for performance and functionality enhancements
- 64-bit, 13-stage pipeline CPU architecture
- 16/32-bit mixable instruction format for compacting code density
- 4-wide frontend decode to optimize instruction throughput
- 128-entry re-order buffer (ROB) to fully utilize the computation resources
- 8 execution pipes for instruction parallelism
- Aggressive branch prediction to optimize performance on various jumps
- Shared cache way allocation support

Security

- Physical Memory Protection (PMP) and ePMP with Optional IOPMP IP to form a complete secure platform.

Power Management

- PowerBrake and WFI (Wait For Interrupt) for power management at different occasions

Applications

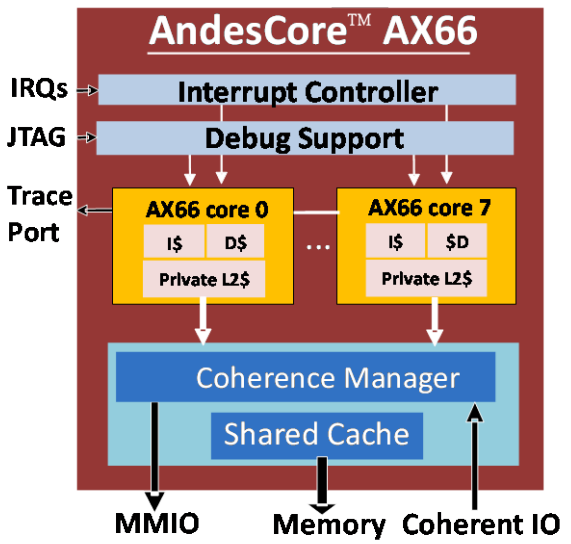
- Networking and Communications
- Android devices
- Video and Multimedia Processing
- SmartNIC or DPU
- AI SoC
- Edge servers

General Descriptions

AndesCore™ AX66 64-bit multicore CPU IP is the 2nd generation of Andes out-of-order processor AX60-series based on AndeStar™ V5 architecture. It supports RISC-V standard “G” (IMAFD) extensions, “B” bit-manipulation, Vector and Vector Cryptography, Hypervisor and AIA (Advanced Interrupt Architecture), and Andes performance/functionality enhancements. Also it is fully compliant to RVA23 profile.

The AX66 supports up to 8 cores, each with private instruction/data L1 caches, a private L2 cache, and a shared L3 cache. All caches support aggressive outstanding transaction capabilities and instruction/data prefetch. Coherence Manager ensures private data cache coherence and I/O coherence for cache-less bus managers. Other AX66 features include ECC for cache memory soft error protection, AIA supporting wired and message signal interrupts, and PowerBrake and WFI for power management.

Functional Blocks



Key Features

CPU Core

- AndeStar™ V5 state-of-the-art ISA supporting 64-bit RISC-V architecture. Little endian
- RV64GCBV and Vector Cryptography
- Hypervisor and AIA
- 13-stage pipeline, out-of-order execution with 128-entry reorder buffer (ROB)
- 4-wide decode, rename, dispatch, and graduate
- 8 execution pipes, including:
  - 4 integer ALUs: 1 with branch instructions, 2 with scalar crypto (when vector crypto not configured)
  - 2 full load/store units
  - 2 Floating-Point/Vector units (FPU/Vector): For the FP units, one is with full set, and one is without divide/square root instructions. The 128bit Vector/Vector Crypto units are configurable with none, single and dual option.
- Dynamic branch prediction
  - TAGE branch predictor with loop predictor
  - 2-level Branch Target Buffer (BTB)
  - Return Address Stack (RAS)
- Privilege Modes:
  - Machine (M), Supervisor(S) and User (U) privilege modes without Hypervisor
  - Machine (M), Hypervisor-Extended Supervisor (HS), Virtualized Supervisor (VS) and Virtualized User (VU) with Hypervisor
- Memory management unit (MMU)
  - Bare, Sv39, and Sv48 ; Sv39x4 and Sv48x4 with Hypervisor.
  - 16/32-entry fully associative L1 ITLB/DTLB
  - Up to 1024-entry 4-way L2 TLBs
- 16 physical memory protection (PMP) regions
- 16 programmable physical memory attributes (PPMA) regions

Private Cache Controllers

- L1 instruction cache and data cache: 64KiB, 4-way, and 64-byte lines
- Private L2 cache: configurable 128KiB-1MiB size
- Instruction/data prefetch
- Store write-around
- ECC: Single error correction and double error detection (SECDED)

Shared Cache Controller

- 256KiB-32MiB, 16-way, pseudo-random replacement
- 64-byte cache line size
- Instruction and Data prefetch
- Configurable multi-cycle SRAM accesses
- SECDED ECC error protection
- Cache way allocation support

Multicore Cache Coherent Cluster

- Support up to 8 cores
- Bus Interfaces
  - 128/256-bit main memory AXI4 bus interface with up to 128 outstanding requests
  - 128/256-bit memory mapped I/O (MMIO) interface
  - 64/128/256-bit I/O coherence port (IOCP)
  - Asynchronous and Synchronous N:1 core vs. external-bus clock ratios

Power Management

- PowerBrake technology to reduce peak power consumption
- WFI (Wait for Interrupt) instruction for software-controlled stalls

Advanced Interrupt Architecture (AIA)

- RISC-V AIA v1.0 spec
- Up to 1023 APLIC interrupt sources
  - APLIC direct mode
  - APLIC-MSI mode
- Support of Message-Signaled interrupts and Inter-Processor Interrupts through IMSIC
- Virtualized Interrupt support for Hypervisor

Debug Module

- One JTAG debug interface and one debug module for all cores
- Up to 8 triggers per core
- Exception redirection handling

Instruction Trace Interface

- RISC-V Processor Trace v1.0 spec

Development Tools

- AndeSight™ IDE (Eclipse-based)
  - Compiler, Debugger, Profiler, Register Bit-field Display/Update, RTOS Awareness, and more
  - Demo examples and sample projects
- RTOSes
  - Open-source: FreeRTOS, Zephyr
- Linux SMP kernel and platform drivers
- FPGA Development Boards through Online AndeShape™ AndesBoardFarm
- AICE-MICRO Debugging Hardware

Product Package

- AndesCore™ AX66 Multicore Processor with AE350 Platform Soft IP Package
  - Pre-integrated AX66 CPU subsystem with APLIC, Debug Module, and AXI Platform
  - Multicore cluster configurable up to 8 cores

AE350 Platform Pre-integrated with AX66

Benefit

Convenience

- A rich collection of high-quality and configurable AXI/AHB/APB IPs required by most embedded systems
- Pre-integrated platform to jump-start SoC designs
- AXI exclusive accesses to implement the atomic operations to non-cacheable AXI spaces

Flexibility

- Scalability of AXI Bus Matrix and AHB/APB Bus Bridge to connect various AMBA components
- Configurable Advanced Platform-Level Interrupt Controller to simplify SoC integration

Efficiency

- Low latency level-one/two memories for best CPU performance
- Bus matrix to allow simultaneous transfers of independent transactions
- DMA controller for fast data movement without software intervention

General Descriptions

The AE350 platform pre-integrated with AX66 CPU is a system design that serves various purposes such as to exploring the product features, evaluating the performance indexes and determining the configuration options.

It contains CPU/Cache memories/Interrupt controller subsystem interfaced to AXI Bus Matrix and AHB/APB Bus Bridge with Platform IP components attached.

Design support includes such as scripts and test cases for integration, simulation, emulation, and prototyping. This pre-integrated platform is ideal for minimizing development efforts by providing a verified reference that is both performance optimized and feature ready for the majority of the applications.

Platform IP Components

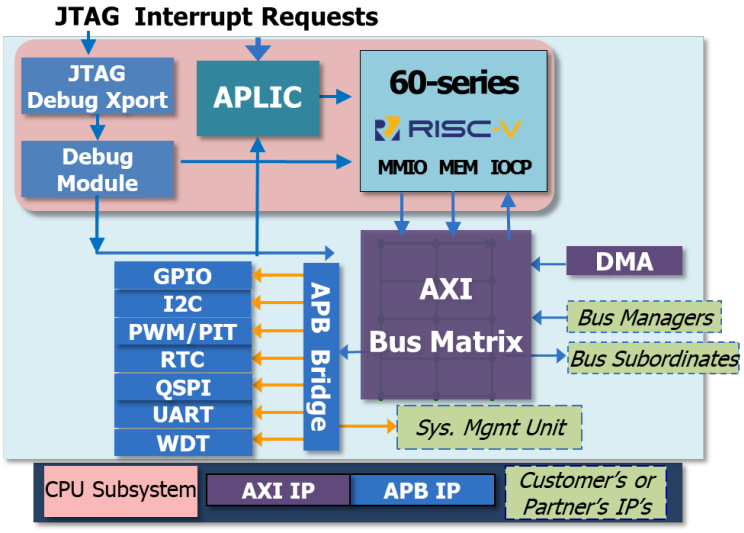
Bus Controller/Bridge

atcbmc300	AXI Bus Matrix Controller
atcaxi2ahb100	Sync. AXI-to-AHB Bridge
atcaxi2ahb200	Async. AXI-to-AHB Bridge
atcbusdec200	AHB Bus Decoder
atcapbbrg100	AHB-to-APB Bridge
atcsizedn300	AXI Downsizer

Bus Components

atcdmac300	DMA Controller (DMAC)
atcuart100	UART Controller
atcspi200	Quad speed SPI Controller
atciic100	I2C Controller (IIC)
atcgpio100	GPIO
atcpit100	Programmable Interval Timer (PIT)/PWM
atcwdt200	Watchdog Timer (WDT)
atcrtc100	Real Time Clock (RTC)
atcexmon300	AXI Exclusive Accesses

Functional Blocks



Andes Technology Corporation
10F, No. 1, Sec. 3, Gongdao 5th Rd., East Dist.,
Hsinchu City, Taiwan R.O.C 30069
Tel: +886-3-5726533
Website: www.andestech.com
Email: sales@andestech.com