AndesCore™ AX65 Processor

Superscalar Out-of-Order Exec. Multicore Cluster

Benefit

Performance

- AndeStar™ V5 Instruction Set Architecture (ISA), compliant to RISC-V technology
- Floating point extensions
- Andes extensions, architected for performance and functionality enhancements
- 64-bit, 13-stage pipeline CPU architecture
- 16/32-bit mixable instruction format for compacting code density
- 4 wide frontend decode to optimize instruction throughput
- 128-entry out-of-order execution to fully utilize the computation resources
- 8 pipelines to explore instruction parallelism
- Branch prediction to optimize performance on conditional jumps
- Return Address Stack (RAS) to speed up procedure returns
- Flexibly configurable Platform-Level Interrupt Controller (PLIC) for real-time performance and a wide range of system usages

Security

- Physical Memory Protection (PMP) and latest architecture enhancement extension (Smepmp) for access permission controls

Flexibility

- Easy arrangement of preemptive interrupts
- StackSafe™ hardware to detect runtime overflow/underflow
- ECC on cache memories for fault protection

Power Management

- PowerBrake and WFI (Wait For Interrupt) for power management at different occasions

Applications

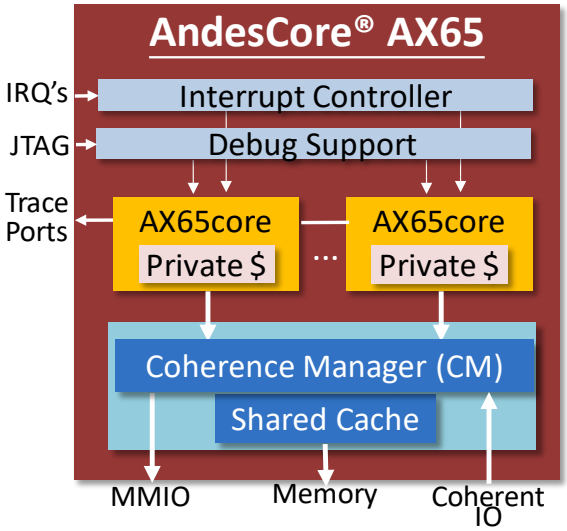
- Networking and Communications
- Advanced Driver-Assistance Systems
- Video and Image Processing
- Storage and Media Streaming

General Descriptions

AndesCore™ AX65 64-bit multicore CPU IP is a 13-stage superscalar out-of-order processor based on AndeStar™ V5 architecture. It supports RISC-V standard “G” (IMAFD) extensions, “C” 16-bit compression, “B” bit-manipulation, scalar cryptography, CMO cache-management operation instructions, and Andes performance/functionality enhancements. Also it is fully compliant to RVA22 profiles. It features MMU for Linux based applications, state-of-the-art TAgged GEometric length (TAGE) algorithm for highly accurate branch predictions.

The AX65 supports up to 8 cores, each with private instruction/data caches, and a shared cache. All caches support aggressive outstanding capabilities and instruction/data prefetch. Coherence Manager ensures private data cache coherence and I/O coherence for cache-less bus masters. Other AX65 features include ECC for cache memory soft error protection, Platform-Level Interrupt Controller (PLIC) with enhancements for vectored dispatch and priority-based preemption, StackSafe™ for software quality improvement, and PowerBrake and WFI for power management.

Functional Blocks



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Key Features

CPU Core

- AndeStar™ V5 state-of-the-art ISA supporting 64-bit RISC-V architecture. Little endian
- RV64GCB and scalar cryptography instructions:
  - Half precision (Zfh), Single precision (F), and double precision (D) floating point extensions
  - Bit-manipulation Zba, Zbb, Zbc, and Zbs
  - Scalar cryptography Zbk, Zkn, Zks, and Zkt
- RISC-V cache-management operation (CMO) instructions
- 13-stage pipeline, out-of-order execution with 128-entry reorder buffer (ROB)
- 4-wide decode, rename, dispatch, and graduate
- 8 execution pipes, including:
  - 4 integer ALUs: 2 with scalar cryptography instructions, and 1 with branch instructions
  - 2 full load/store units
  - 2 floating-point units (FPUs): 1 full set, and 1 without divide, square root instructions
- Dynamic branch prediction
  - TAGE branch predictor with loop predictor
  - 2-level Branch Target Buffer (BTB)
  - Return Address Stack (RAS)
- Machine (M), supervisor (S), and user (U) privilege modes
- Memory management unit (MMU)
  - Svnapot, Svpbmt, Svinval
  - Bare, Sv39, and Sv48 VA translations
  - 16/32-entry fully associative L1 ITLB/DTLB
  - Up to 1024-entry 4-way L2 TLBs
- 16 physical memory protection (PMP) regions
- 16 programmable physical memory attributes (PPMA) regions

Private Cache Controller

- 64KB 4-way instruction cache and data cache
- 64-byte cache line size
- Data cache prefetch and write around
- ECC: Single error correction and double error detection (SECDED)

Shared Cache Controller

- 256KB/512KB/1MB/2MB/4MB/8MB, 16-way, pseudo-random replacement
- 64-byte cache line size
- Prefetch
  - Instruction: prefetch after a miss
  - Data: prefetch after sequential misses; tracking 8 address sequences
- Configurable multi-cycle SRAM accesses
- SECDED ECC error protection

Multicore Cache Coherent Cluster

- Support up to 8 cores
- Bus Interfaces
  - 256-bit main memory AXI4 bus interface
  - 256-bit memory mapped I/O (MMIO) interface
  - 256-bit I/O coherence port (IOCP)
  - Asynchronous and Synchronous N:1 core vs. external-bus clock ratios

Power Management

- PowerBrake technology to reduce peak power consumption
- WFI (Wait for Interrupt) instruction for software-controlled stalls

Platform-Level Interrupt Controller (PLIC)

- Up to 1023 PLIC interrupt sources
- Up to 255 PLIC interrupt priority levels
- Up to 16 PLIC interrupt targets
- Enhanced Interrupt Features
  - Vectored interrupt dispatch
  - Priority-based preemption
  - Selectable edge trigger or level trigger

Debug Module

- One JTAG debug interface and one debug module for all cores
- Up to 8 triggers per core
- Exception redirection handling

Instruction Trace Interface

- Compliant to the ratified RISC-V Processor Trace Specification for each core

Development Tools

- AndeSight™ IDE (Eclipse-based)
  - Compiler, Debugger, Profiler, Register Bit-field Display/Update, RTOS Awareness, and more
  - Demo examples and sample projects
- RTOSes
  - Open-source: FreeRTOS, Zephyr
  - Commercial: ThreadX, µC/OS-II
- Linux SMP kernel and platform drivers
- FPGA Development Boards through Online AndeShape™ AndesBoardFarm
- AICE-MICRO Debugging Hardware

Product Package

- AndesCore™ AX65 Multicore Processor with AE350 Platform Soft IP Package
  - Pre-integrated AX65 CPU subsystem with PLIC, Debug Module, and AXI Platform
  - Multicore cluster configurable up to 8 cores

AE350 Platform Pre-integrated with AX65

Benefit

Convenience

- A rich collection of high-quality and configurable AXI/AHB/APB IPs required by most embedded systems
- Pre-integrated platform to jump-start SoC designs
- AXI exclusive accesses to implement the atomic operations to non-cacheable AXI spaces

Flexibility

- Scalability of AXI Bus Matrix and AHB/APB Bus Bridge to connect various AMBA components
- Configurable Platform-Level Interrupt Controller to simplify SoC integration

Efficiency

- Low latency level-one/two memories for best CPU performance
- Bus matrix to allow simultaneous transfers of independent transactions
- DMA controller for fast data movement without software intervention

General Descriptions

The AE350 platform pre-integrated with AX65 CPU is a system design that serves various purposes such as to exploring the product features, evaluating the performance indexes and determining the configuration options.

It contains CPU/Cache memories/Interrupt controller subsystem interfaced to AXI Bus Matrix and AHB/APB Bus Bridge with Platform IP components attached.

Design support includes such as scripts and test cases for integration, simulation, emulation, and prototyping. This pre-integrated platform is ideal for minimizing development efforts by providing a verified reference that is both performance optimized and feature ready for a majority of the applications.

Platform IP Components

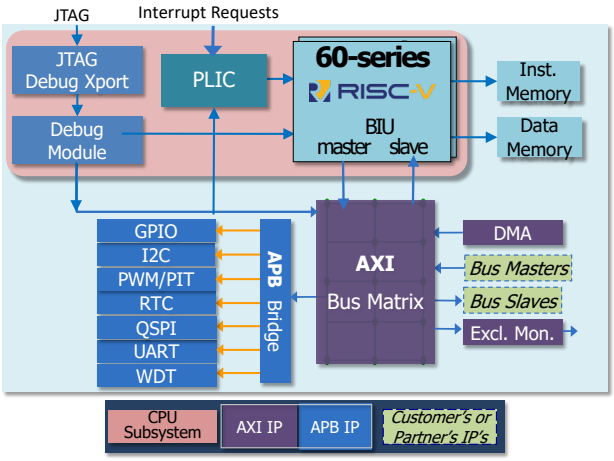
Bus Controller/Bridge

atcbmc300	AXI Bus Matrix Controller
atcaxi2ahb100	Sync. AXI-to-AHB Bridge
atcaxi2ahb200	Async. AXI-to-AHB Bridge
atcbusdec200	AHB Bus Decoder
atcapbbrg100	AHB-to-APB Bridge
atcsizedn300	AXI Downsizer

Bus Components

atcdmac300	DMA Controller (DMAC)
atcuart100	UART Controller
atcspi200	Quad speed SPI Controller
atciic100	I2C Controller (IIC)
atcgpio100	GPIO
atcpit100	Programmable Interval Timer (PIT)/PWM
atcwdt200	Watchdog Timer (WDT)
atcrtc100	Real Time Clock (RTC)
atcexmon300	AXI Exclusive Accesses

Functional Blocks



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