AndesCore™ A(X)46MP(V) Vector Processor

64/32-bit RISC-V Multicore Processor with 2048-bit Vector and AMM

Benefit

Performance

- 32 and 64-bit in-order dual-issue 8-stage CPU core with configurable 0-2048bit VPU and Andes Matrix Multiply (AMM) Extension
- Private L2 cache, shared Level-3 cache and coherence support
- AndeStar™ V5 Instruction Set Architecture (ISA)
- Separately licensable Andes Custom Extension™ (ACE) for customized scalar and vector acceleration
- Support both RV32(A46MP and A46MPV) and RV64(AX46MP and AX46MPV) architecture; RV64 cores also support RV64/32 Dynamic UXL for running RV64 and RV32 user-mode applications
- Linux-capable Memory Management Unit (MMU)
- Physical Memory Protection (PMP) and programmable Physical Memory Attribute (PPMA)
- Platform-Level Interrupt Controller (PLIC) with Andes-enhanced vectored dispatch
- Andes Streaming Port (ASP) and High-Bandwidth Vector Memory (HVM) support
- Full-arithmetic BF16 vector/scalar instructions with mode bit control

Flexibility

- Multiprocessing up to 16 cores with hardware managed data coherence
- Configurable VPU vector length (VLEN) and datapath length (DLEN)
- ECC or Parity for SRAM error protection
- StackSafe™ hardware to help measuring stack size, and detecting runtime overflow/underflow
- Versatile configurations to tradeoff between core size and performance requirements

Power Management

- PowerBrake and WFI (Wait For Interrupt) for different power saving occasions

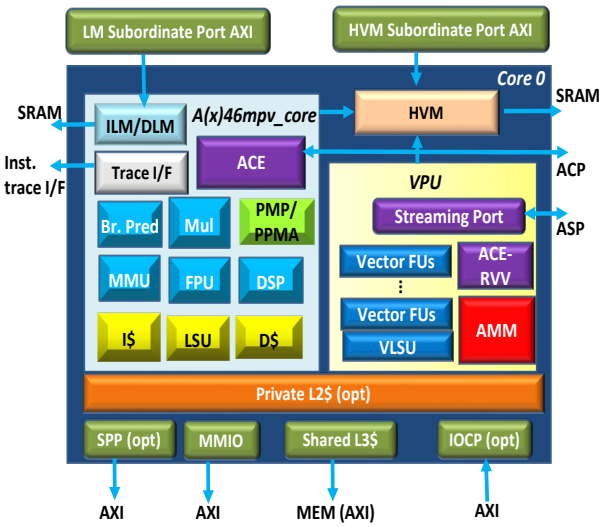
Applications

- Computer Vision and Image Processing
- Digital Signal Processing
- Machine/Deep Learning Acceleration
- Real-time Control
- Networking

General Descriptions

AndesCore™ A(X)46MP(V) 32/64-bit multicore CPU IP is an 8-stage superscalar processor with Vector Processing Unit (VPU) based on AndeStar™ V5 architecture and Andes Matrix Multiply (AMM) extension. It supports RISC-V standard “G (IMA-FD)”, “ZC” compression, “B” bit manipulation, DSP/SIMD ‘P’ (draft), “V” (vector), CMO (cache management) extensions, Andes performance enhancements, plus Andes Custom Extension™ (ACE) for user-defined instructions. It supports all RVA22 profile mandatory ISAs. It features MMU for Linux based applications, dynamic branch prediction for efficient branch execution, dual-issue of common instruction pairs, level-1 private instruction/data caches, private level-2 cache and local memories for low-latency accesses. The A(X)46MP(V) symmetric multiprocessor supports up to 16 cores and a shared level-3 cache controller. Coherence Manger ensures data coherence among CPU accesses and IO transactions from external bus managers. All caches are non-blocking with prefetch support. The A(X)46MPV have a powerful VPU with up to 2048b VLEN and Matrix unit, is excellent for computations involving large arrays of data.

CPU Functional Blocks



Key Features

Scalar Unit

- 8-stage in-order dual issue pipeline
- AndeStar™ V5 architecture
  - RISC-V RV64 and RV32 GCBPV, little endian:
  - Andes V5 performance/code size extensions
- Machine (M), Supervisor (S), User (U) privileges
- MMU with SV32(RV32), Sv39/Sv48/SV57(RV64) virtual memory translation
- Dual memory load/store units
- PMP up to 32 regions and programmable PMA up to 16 regions
- Multiplier options for sequential 1/2/4/8-bit per cycle or fast pipelined 2 cycles
- Optional branch prediction with Branch Target Buffer (BTB) and Return Address Stack (RAS)

Vector Processing Unit for A(X)46MPV

- In-order, dual-issue
- RISC-V V-extension (RVV) 1.0 spec.
  - Data formats:
    - Standard: int8/16/32/64, fp16/32/64, bf16(draft)
    - Andes extended: bf16 full arithmetic mode
  - Andes extended instructions
    - Vector Int4 load
    - Vector Dot Product
  - Vector Unit-Stride, Strided, Indexed, Segment Load/Store
- Custom RVV instructions based on ACE-RVV
- Configurable VLEN/DLEN from 128/128 to 2048/1024 bits with 1:1 or 2:1 ratio
- Multiple chainable parallel functional units
- Dual load or one load +one store for simultaneous unit-stride accesses
- Andes Streaming Port (ASP) load/store
- Andes Matrix Multiply (AMM) Extension with 2D load/store and matrix multiply support for INT8 data type to accelerate matrix multiply for edge AI

Andes Custom Extension™ (ACE)

- Customized instructions for acceleration (separately licensable)
- Instruction feature highlights
  - Standard and custom-defined operands
  - Vector instructions with RVV formats executing in VPU
  - Scalar instructions executing in background
- Design support
  - Design using standard languages (C, Verilog)
  - Automatic opcode assignment
  - Automatic generation of housekeeping RTL
  - Automated instruction function verification

Level-1/2 Memory Subsystem

- Private L1 Instruction and Data Caches
  - Separately configurable from 16KB to 64KB
  - 4-way set associative
- Optional Private Unified L2 cache from 64kB to 512KB, 8-way set associative
- High-bandwidth Vector Memory (HVM) interfaces
  - Configurable from 4KB to 4GB
  - Accessible by scalar and vector load/store
  - DLEN-wide interface for fast vector loads/stores
  - 1 or 2 manager ports for processor accesses, supporting out-of-order responses
  - 1 subordinate port for external accesses
- Instruction/Data Local Memory (ILM/DLM)
  - Separately configurable from 4KB to 16MB
  - Accessible by scalar unit only
  - LM subordinate port for external accesses
- MemBoost - Enhanced Memory Performance
  - Data cache write-around
  - Instruction and data prefetch
  - Multiple outstanding D-Cache misses
- Optional error protection: Parity or ECC for instruction cache, and ECC for the rest memory

HVM Reference Design

- Sharable by up to 16 cores
- Up to 64 memory banks with out of order response

Level-3 Shared Cache Controller

- Configurable cache size, 256KB to 32MB
- 64-byte cache line size, 16-way, pseudo random cache line replacement policy
- Up to 64 outstanding transactions
- Multiple tag and data banks with bank interleaving
- Multi-cycle control to match SRAM timing
- Optional ECC error protection
- Instruction and Data Prefetch

Multicore Cache Coherence

- Supporting up to 16 cores
- Coherence among data caches, L2 caches and IO Coherent Port transactions

Bus Interfaces

- All configurable data width from 128 to 512 bits except 64-bit SPP
- Synchronous N:1 core-to-bus clock ratios or Asynchronous bus clock

- Memory port for cacheable accesses
- MMIO port for non-cacheable accesses
- IOCP (IO Coherence Port) for external bus manager accesses
- Shared Peripheral Port (SPP) for external peripherals

Power Management

- PowerBrake technology to reduce peak power consumption
- WFI (Wait for Interrupt) instruction for software controlled stalls

Platform-Level Interrupt Cont. (PLIC)

- Over 1000 PLIC interrupt sources
- Up to 255 PLIC interrupt priority levels
- Up to 16 PLIC interrupt targets
- Enhanced interrupt features
  - Vectored interrupt dispatch
  - Priority-based preemption
  - Selectable edge trigger or level trigger

External Debug Module

- Secure debug
- RISC-V Debug 1.0 JTAG debug interface with up to 8 triggers
- Exception redirection handling

Trace Interface

- RISC-V Trace 1.0 Instruction Trace interface

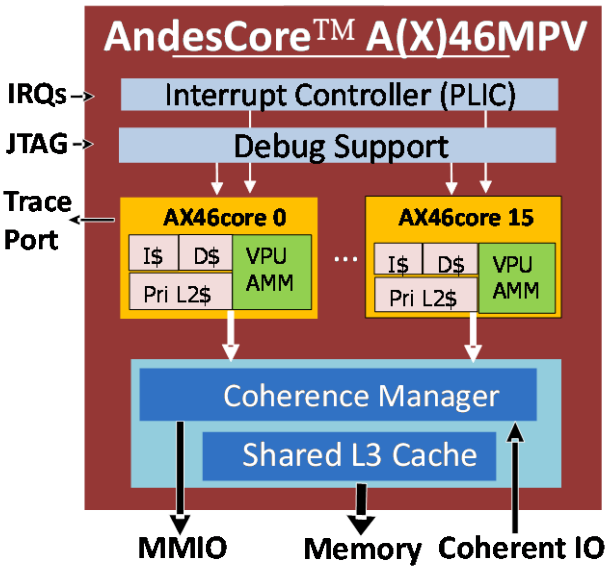
Development Tools

- AndeSight™ IDE (Eclipse-based)
  - Project Management, Streamlined GUI, Feature-rich Editor, Optimized Toolchains, Source Level Debugger, Profiling Analysis, Flash ISP, RTOS Awareness, and more
  - Tested platforms: Windows and Linux
  - Demo examples and sample projects
  - RTOS: FreeRTOS, Zephyr
  - Linux SMP kernel and platform drivers
  - Optimized compute library: DSP, Vector
  - Peripheral drivers for AndeShape™ platform
  - Near cycle-accurate simulator
- FPGA Development Boards
  - AndeShape™ Board Farm
- Debugging Hardware
  - AICE-MINI+, AICE-MICRO
- COPILOT: automation tool for ACE

Product Packages

- AndesCore™ A(X)46MP(V) series with 1 – 16 cores and AE350 AXI Platform
  - AX46MPV Standard: RV64 with 128/256b VLEN
  - AX46MPV Advanced: RV64 with 256-2048b VLEN
  - AX46MP: RV64 without VPU
  - A46MPV: RV32 with 128/256b VLEN
  - A46MP: RV32 without VPU

Multicore Functional Block



AXI-Based Platform Pre-integrated with A(X)46MP(V)

Benefit

Convenience

- A rich collection of high-quality and configurable AXI/AHB/APB(AE350) IPs required by most embedded systems
- Pre-integrated platform to jump-start designs
- AXI exclusive accesses to implement the atomic operations to non-cacheable AXI spaces

Flexibility

- Scalability of AXI Bus Matrix and AHB/APB Bus Bridge to connect various AMBA components
- Configurable PLIC to simplify SoC integration

Performance

- Low latency level-one memories for best CPU performance
- Bus matrix to allow simultaneous transfers of independent transactions
- DMA controller for fast data movement without software's intervention

General Descriptions

The AXI-based platform pre-integrated with A(X)46MPV is a system design that serves various purposes such as to explore the product features, to evaluate the performance indexes and to determine the configuration options.

It contains the CPU subsystem, including CPU, Local Memories and PLIC, interfaced to AXI Bus Matrix and AHB/APB Bus Bridge with Platform IP components attached.

Design support includes scripts and test cases for integration, simulation, emulation and prototyping. This pre-integrated platform is ideal for minimizing development efforts by providing a verified reference which is both performance optimized and feature ready for most embedded applications.

Platform IP Components

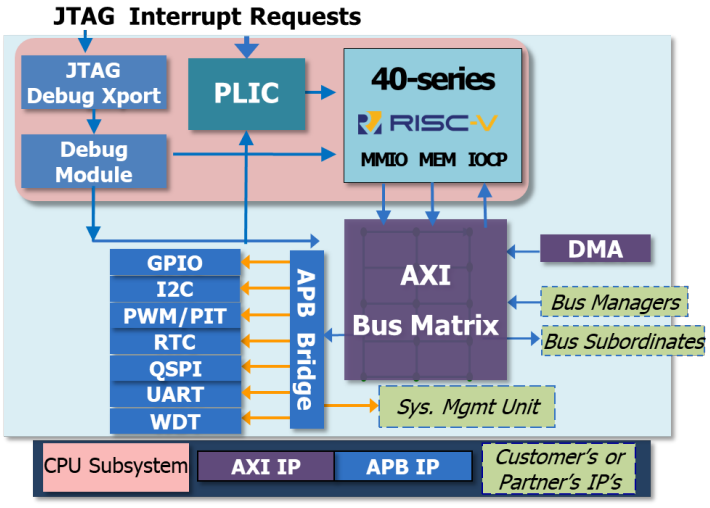
Bus Controller/Bridge

atcbmc300	AXI Bus Matrix Controller
atcaxi2ahb100	Sync. AXI-to-AHB Bridge
atcaxi2ahb200	Async. AXI-to-AHB Bridge
atcbusdec200	AHB Bus Decoder
atcapbbrg100	AHB-to-APB Bridge
atcsizedn300	AXI Downsizer

Bus Components

atcdmac300	DMA Controller (DMAC)
atcuart100	UART Controller
atcspi200	Quad speed SPI Controller
atciic100	I2C Controller (IIC)
atcgpio100	GPIO
atcpit100	Programmable Interval Timer (PIT)/PWM
atcwdt200	Watchdog Timer (WDT)
atcrtc100	Real Time Clock (RTC)
atcexmon300	AXI Exclusive Accesses

Functional Blocks



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