ANDES in Sight

ANDES TECHNOLOGY Newsletter

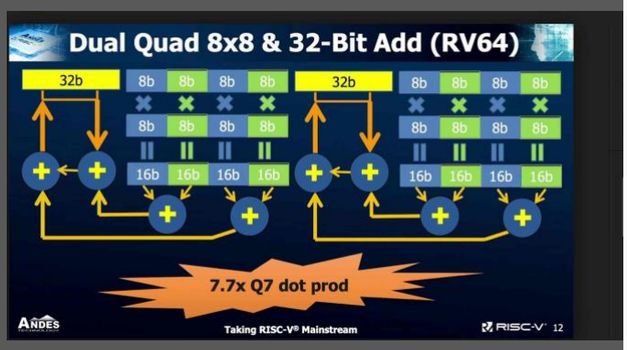
Andes Technology and Silex Insight Announce Strategic Partnership for RISC-V Based Root-of-Trust IP Solutions

Andes Technology, a leading Asia-based supplier of high-performance low-power compact 32/64-bit RISC-V CPU cores, and Silex Insight, a leading provider for flexible security IP cores, are announcing a strategic partnership to bring flexible and energy efficient Root-of-Trust security IP solution based on RISC-V to the industry. Silex Insight's advanced eSecure IP module is a complete solution that enables security applications by shielding confidential information from non-secure applications running on main processor along with security boot, sensitive key materials and assets protection. AndesCore™ N22, a high-efficiency and low-power 2-stage pipeline RISC-V CPU core, is tightly integrated in the eSecure IP module to fully, robustly control the execution of security functions. The highly configurable eSecure module provides a wide-range selection of security features, performance, area and energy consumption that is suitable for applications such as IoT, storage, and communication.

Andes Technology Launches RISC-V FreeStart Program with its Commercial-Grade CPU N22

In June, Andes Technology Corporation (TWSE:6533) announced its RISC-V FreeStart program. The program offers an easy and fast way to build a solid SoC foundation on the commercial-grade RISC-V CPU core N22, available for free download. AndesCore™ N22 is an entry-level, ultra-compact, low-power and performance-efficient RISC-V CPU IP. It delivers the highest 3.95 Coremark/MHz in its class, and offers rich configurable features, including multiplier, interrupt controller, local memory, instruction cache, debug support, and an optional AHB platform. With the RISC-V FreeStart program, SoC engineers can begin designing a RISC-V based SoC without budgeting CPU IP upfront. Read the EETimes article.

Andes Technology, Chair of the RISC-V P Extension Task Group, Reports Progress

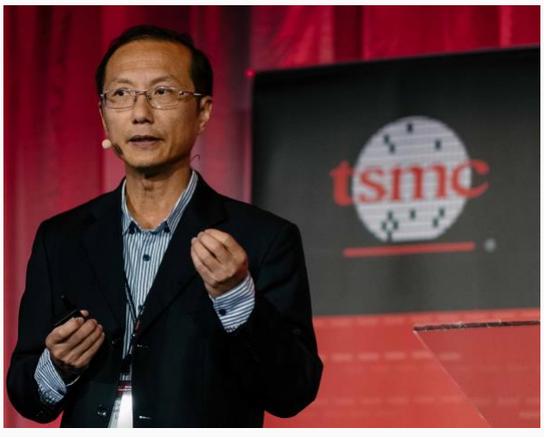


Andes Technology Corp. Senior Director Chuan-Hua Chang reports on RISC-V P Extension Task Group progress, he presented the task group's work on June 11, 2019 at the RISC-V Workshop Zurich, Switzerland. Here is a summary of the work, mainly contributed by Andes:

- Created P extension instruction proposal spreadsheet for TG members to review.
- Released detailed instruction operation specification.
- Released toolchain and simulator binaries for TG members to evaluate the use of these instructions.
- Benchmarked audio and speech codec, neural network for image recognition, and over 200 DSP library functions, and all showed very impressive speedups.

Click for full presentation.

Andes Technology President Frankwell Lin Describes Andes IP in TSMC Process Technology



Frankwell Lin, President of Andes Technology, presented "Andes RISC-V CPU IP Provide Synergism for TSMC Process Portfolio" during the TSMC Europe open innovation platform (OIP) ecosystem forum in Amsterdam on May 27 and 28. The presentation described the open source RISC-V instruction set architecture synergy that RISC-V CPU IP provides to TSMC's ecosystem. The speech was well received by the audience. Andes management and technical team were on hand throughout the day in the TSMC Europe Technology Symposium Exhibition area to describe Andes new RISC-V products and to answer questions from attendees. Andes demos included a face detection system with RISC-V based AndesCore™ AX25 embedded.

Andes Technology Corp. CTO Charlie Su Detailed RISC-V in AIoT/5G at COMPUTEX

To introduce the latest trend of embedded systems, Taiwan RISC-V Alliance held the "New Smart Embedded Solution Forum" focusing on RISC-V x AIoT/5G at COMPUTEX Taipei on May 29. Speakers including Charlie Su, CTO & EVP of Andes Technology, Liu Chung Laung, Chairman of TrendForce and Wayne Dai, Chairman of VeriSilicon. They shared the latest development of RISC-V and market dynamics detailing strategy, technology and applications.

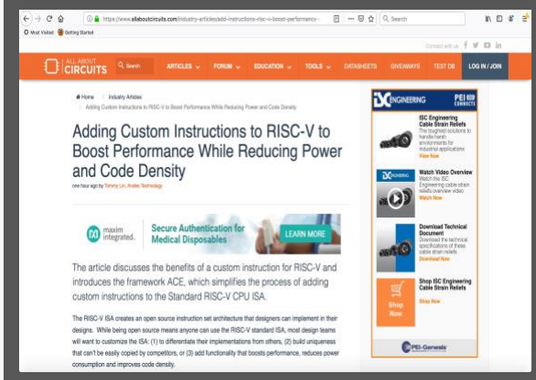
Charlie Su presented "AIoT Embedded Design Architecture and RISC-V Application Trends" that described cutting-edge trends of AI and IoT. In addition to the rise of RISC-V, he introduced Andes' RISC-V based V5 family cores, and detailed how they help customers expand the fields of applications.

Andes Details RISC-V CPU Offerings at TSMC Taiwan Technology Symposium in Hsinchu

On May 23, TSMC technology symposium Taiwan was held in the Hsinchu, Ambassador Hotel. More than 800 attendees joined the important technology conference. Andes sales, marketing, and technical teams joined the grand event and interacted with customers. Many onsite visitors showed a high level of interest in RISC-V and the Andes teams explained its RISC-V solutions and their benefits. Andes also provided a free download of AndeSight™, Andes Eclipse-based integrated development environment.

Click for more details about AndeSight Free Download:

Andes' Tommy Lin Describes Value of Adding Custom Instructions to RISC-V CPU for Differentiation, Security & Power Savings



The All About Circuits article, by Andes Technology's deputy director of business development Tommy Lin, discusses the benefits of custom instructions for RISC-V and introduces the framework ACE, which simplifies the process of adding custom instructions to the Standard RISC-V CPU ISA. The RISC-V ISA creates an open source instruction set architecture that designers can implement in their designs. While being open source means anyone can use the RISC-V standard ISA, most design teams will want to customize the ISA: (1) to differentiate their implementations from others, (2) build uniqueness that can't be easily copied by competitors, or (3) add functionality that boosts performance, reduces power consumption and improves code density.



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