Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
Agenda

- Overview of Andes Technology Corporation
- Operating Results
- Product Applications
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks
Overview of Andes Technology Corporation

Andes Highlights

• Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
• Well-established high technology IPO company
• Just over 190 people; 80% are engineers.
• EETimes’ Silicon 60 Hot Startups to Watch (2012)
• TSMC OIP Award “Partner of the Year” for New IP (2015)
• A founding member of RISC-V Foundation (2016)
• MCU innovation award by China online press (2018)

Andes Mission

• Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

• Smart and Green electronic devices
• Cloud Computing and Internet of Things and Machine Learning
Operating Results
Business Status Overview

- **>160 commercial licensees**
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
  - **>300 license agreements signed**

- **AndeSight™ IDE:**
  - **>17,000 installations**

- **Eco-system:**
  - **>145 partners**

- **>4.5B Accumulative SoC Shipped**
Agreement Growth Analysis

<table>
<thead>
<tr>
<th>Year</th>
<th>IP agreements</th>
<th>Accumulated IP agreements</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2007</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>2008</td>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td>2009</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>2010</td>
<td>12</td>
<td>24</td>
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<tr>
<td>2011</td>
<td>16</td>
<td>40</td>
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<tr>
<td>2012</td>
<td>16</td>
<td>56</td>
</tr>
<tr>
<td>2013</td>
<td>24</td>
<td>80</td>
</tr>
<tr>
<td>2014</td>
<td>27</td>
<td>107</td>
</tr>
<tr>
<td>2015</td>
<td>27</td>
<td>134</td>
</tr>
<tr>
<td>2016</td>
<td>31</td>
<td>165</td>
</tr>
<tr>
<td>2017</td>
<td>39</td>
<td>204</td>
</tr>
<tr>
<td>2018</td>
<td>43</td>
<td>247</td>
</tr>
<tr>
<td>1~3Q 2019</td>
<td>70</td>
<td>317</td>
</tr>
</tbody>
</table>
2Q19 Revenue Analysis

Year-over-year (YoY): +126.8%
Quarter-over-quarter (QoQ): -17.7%

Q19 Revenue Analysis

<table>
<thead>
<tr>
<th>Quarter</th>
<th>QoQ Change</th>
<th>YoY Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>3Q 18</td>
<td>-20,000</td>
<td></td>
</tr>
<tr>
<td>2Q 19</td>
<td>56,364</td>
<td>155,410</td>
</tr>
<tr>
<td>3Q 19</td>
<td>127,851</td>
<td></td>
</tr>
</tbody>
</table>

(NT$ thousands)
1-3Q19 Top 10 Customers Analysis by Revenue

Top 10 Customer Contributed 73% Revenue

(NT$ thousands)

AI (US) 5G (US) Touch Panel (TW) Sensing (TW) Audio (CN) Security IC (CN) AI (US) Touch Panel (TW) Storage (US) AI (TW)
3Q19 Royalty Analysis

YoY +25.9%
QoQ +28.2%

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Royalty (NT$ thousands)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3Q 18</td>
<td>22,655</td>
</tr>
<tr>
<td>2Q 19</td>
<td>22,245</td>
</tr>
<tr>
<td>3Q 19</td>
<td>28,519</td>
</tr>
</tbody>
</table>
1-3Q19 Top Ten Royalty Contributors Analysis by Application

Top 10 Royalty Customers
Contribution Analysis: 93%

(NT$ thousands)
Royalty Analysis

(NT$ thousands)

- **Royalty**
  - 2012: 660
  - 2013: 1,285
  - 2014: 10,819
  - 2015: 12,232
  - 2016: 13,320
  - 2017: 38,287
  - 2018: 74,953
  - 1-3Q 2019: 74,785

- **Customer numbers**
  - 2012: 2
  - 2013: 5
  - 2014: 9
  - 2015: 15
  - 2016: 15
  - 2017: 25
  - 2018: 28
  - 1-3Q 2019: 28

(單位:家數)
Consolidated Gross Margin

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Gross Profit</th>
<th>Gross Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>3Q 18</td>
<td>56,217</td>
<td>99.74%</td>
</tr>
<tr>
<td>2Q 19</td>
<td>155,311</td>
<td>99.94%</td>
</tr>
<tr>
<td>3Q 19</td>
<td>127,528</td>
<td>99.75%</td>
</tr>
</tbody>
</table>
Consolidated Operating Expenses

YoY +93.7%
QoQ -6.3%

63,840 131,918 123,667

(NT$ thousands)

R&D expenses
Administration expenses
Selling expenses

3Q 18 2Q 19 3Q 19
28,072 18,400 14,991
14,485 51,883 54,211
21,283 54,465 54,465

YoY +93.7%
QoQ -6.3%
Consolidated Operating Income (Loss)

QoQ - 83.5%  
YoY - %

(NT$ thousands)

23,393

3Q 18  2Q 19  3Q 19

-10,000  -5,000  0  5,000  10,000  15,000  20,000  25,000

(7,623)  23,393  3,861

-10,000  -5,000  0  5,000  10,000  15,000  20,000  25,000

Consolidated Operating Income (Loss)
Consolidated Operating Margin

YoY
+16.55 pt

QoQ
-12.03pt

(NT$ thousands)

15.05%
3.02%

3Q 18
2Q 19
3Q 19

(13.53%)
Consolidated Net Income (Loss)

QoQ - 83.8%
YoY -%

(NT$ thousands)

3Q 18  | 2Q 19  | 3Q 19
--- | --- | ---
(6,705) | 25,209 | 4,077

Driving Innovations™
Consolidated Net Profit Margin

YoY
+15.09pt

QoQ
-13.03 pt

(NT$ thousands)

16.22%

3.19%

3Q 18
2Q 19
3Q 19

(11.90%)
Consolidated Earnings Per Share

1~3Q19 EPS: 0.13

(NT$)

QoQ -0.49
YoY +0.26

3Q 18
2Q 19
3Q 19

3Q 18
(0.16)

2Q 19
0.59

3Q 19
0.10

(0.30)
1-3Q 19 Revenue Analysis by Payment Model

- License Fee: 57%
- Running Royalty: 21%
- Custom Computing Service: 16%
- Maintenance & Others: 6%
1-3Q 19 Revenue Analysis by Region

- Taiwan: 38%
- USA: 31%
- China: 25%
- Europe: 4%
- Korea: 2%
- Japan: 2%

Driving Innovations™
1-3Q19 Customer Application Analysis

*Based on agreement number
1-3Q19 Revenue Analysis by Product

- V3: 17%
- RISC-V: 34%
- Customer Computing: 49%

Product Revenue Breakdown:

- N8: 19%
- N25: 18%
- Service: 13%
- D25: 12%
- N9: 9%
- NX25: 6%
- AX25: 5%
- ACE: 5%
- TURBU: 3%
- D10: 1%
- S8: 1%
- N15: 1%
- N7: 1%
- N22: 1%
- N13: 1%
- EVB: 1%
- Other: 1%
3Q19 Revenue Analysis - RISC-V

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>3Q18</th>
<th>2Q19</th>
<th>3Q19</th>
</tr>
</thead>
<tbody>
<tr>
<td>V3</td>
<td>30,198</td>
<td>53,086</td>
<td>31,683</td>
</tr>
<tr>
<td>RISC-V</td>
<td>26,166</td>
<td>85,584</td>
<td>27,111</td>
</tr>
<tr>
<td>Custom Computing</td>
<td></td>
<td>16,740</td>
<td>69,057</td>
</tr>
</tbody>
</table>

46% 55% 54%
1-3Q19 Revenue Analysis - RISC-V

(NT$ thousands)

18 Q1-Q3 19 Q1-Q3

<table>
<thead>
<tr>
<th></th>
<th>124,733</th>
<th>149,092</th>
</tr>
</thead>
<tbody>
<tr>
<td>V3</td>
<td>54,399</td>
<td>60,422</td>
</tr>
<tr>
<td>RISC-V</td>
<td>46%</td>
<td>49%</td>
</tr>
<tr>
<td>Custom Computing</td>
<td>29,374</td>
<td>32,340</td>
</tr>
</tbody>
</table>

18 Q1-Q3: 54,399 (NT$ thousands) 46%
19 Q1-Q3: 60,422 (NT$ thousands) 49%
Product Application
A 14-year-old public CPU IP company

A founding member of the RISC-V Foundation

A major open source maintainer/contributor

Active involvement in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group
Example Applications of Andes-Embedded™ SoC

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
- ESL
- Smart Meter
- Smart Lighting

- Communication & IoT

- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition

- Storage & Sensor

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

- Industrial & Video

- and more.....
IoT Application - 1

Bluetooth Speaker

Sigfox LPWAN

Healthcare device

Wearable device

Electronic price tags

Sensor Hub
IoT Application -2

- Wearable devices
- Drone
- Portable Karaoke
- WiFi/GPS/FM/Bluetooth combo
- GPS/Beido in shared bikes
- Contactless payment (NFC)
Andes Embedded in Smart Phones

1 in 5 Smart Phones are with Andes Embedded
Andes Embedded in Consumer Devices, Cars and Datacenters

- **Switch:** MXIC Flash Ctrl
- **Echo Dot2:** Mediatek WiFi IoT
- **Bike Sharing:** GPS Ctrl
- **X-Trail:** ADAS Ctrl

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)
New Products and Ecosystems
Product Lines

◆ New A-series Cores released in Andes Embedded Forum 2018
Andes RISC-V Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

AndesCore™ Processors

Highly optimized design with leading PPA

AndeSight™ Tools

Professional IDE with high code quality

AndeEmbedded™

Handy peripheral IPs to speed up SoC construction

AndeShape™ Platforms

AndeSoft™ Stacks

Extensive SW stacks from bare metal, RTOS to Linux
V5 AndesCore™ Processors

N22
N25F/NX25F/D25F
A25/AX25
A25MP/AX25MP
AndesCore™ RISC-V Families

Cores with higher total performance and RISC-V ISA extensions

Next-Gen

Cache-Coherent Multicores

Linux with FPU/DSP

Fast/Compact with FPU/DSP

Slim and Efficient

A25MP
1/2/4 A25, L2$, L1/I coherence

AX25MP
1/2/4 AX25, L2$, L1/I coherence

A25
N25F, MMU, DSP

AX25
NX25F, MMU, DSP

N25F
V5/32b, FPU, PMP

D25F
N25F, DSP

NX25F
V5/64b, FPU, PMP

N22
V5[e], 32/16 GPR

A25MP
1/2/4 A25, L2$, L1/I coherence

AX25MP
1/2/4 AX25, L2$, L1/I coherence

N25F
V5/32b, FPU, PMP

D25F
N25F, DSP

NX25F
V5/64b, FPU, PMP

N22
V5[e], 32/16 GPR

Cache-Coherent Multicores

Linux with FPU/DSP

Fast/Compact with FPU/DSP

Slim and Efficient

AndesCore™ RISC-V Families

Higher performance

5-stage >1.2GHz
3.58 CoreMark
2.09 DMIPS

2-stage 700MHz
3.95 CoreMark
1.80 DMIPS

32bit

64bit
Bring Andes Strength to RISC-V Core Family

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure
V5 AndesCores: 25-series

- **N25F**: 32-bit, **NX25F**: 64-bit
  - From scratch for the best PPA
  - Very configurable

- **AndeStar V5 ISA**

- **5-stage pipeline**

- **Configurable multiplier**

- **Optional branch prediction**

- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses

- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case, w/o caches)
  - Large config: 136K gates, 1.2GHz (worst case, w/ caches)
  - Best-in-class Coremark: 3.58/MHz
V5 AndesCores: 25-series

- Fast-n-small for control tasks in AR/VR, networking, storage, AI
- N25F/NX25F: +FPU
  - +, -, x, x+, x-: pipelined 4 cycles
  - ÷, √: run in the background
    - 15 for SP, 29 for DP
- A25/AX25: +FP +Linux
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- Whetstone/MHz:

<table>
<thead>
<tr>
<th></th>
<th>NX25F</th>
<th>N25F</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP</td>
<td>1.38</td>
<td>1.30</td>
</tr>
<tr>
<td>SP</td>
<td>1.56</td>
<td>1.58</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Competitor Core 1</th>
<th>Competitor Core 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP</td>
<td>0.50</td>
<td>0.54</td>
</tr>
<tr>
<td>SP</td>
<td>1.09</td>
<td></td>
</tr>
</tbody>
</table>
V5 AndesCores: 22-series

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension

- **2-stage pipeline with AHB-lite main bus**

- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller

- **28nm PPA:**
  - 700 MHz (worst case)
  - 16K gates (minimal)

- **Best per-MHz performance:**
  - 1.8 DMIPS (no inline)
  - 3.95 Coremark
A(X)25MP Cache-Coherent Multicore

- **1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs**
  - RV-GCP ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes’ contribution to RISC-V

- **Hardware Multicore Cache Coherence**
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches

- **Level-2 Cache Controller**
  - 0/128/256K...2MB, 32-byte line, 16-way
  - ECC, SECDED support

- **Bus Interfaces**
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio

- **Platform Level Interrupt, Debug and Trace Support**
ACE: Andes Custom Extension

- **Verilog user.v**
- **concise RTL**
- **semantics, operands, test-case spec**

**COPILOT**
Custom-OPtimized Instruction deveLOpment Tools

- **Extended Tools**
- **Extended ISS**
- **Extended RTL**

**Automated Env. For Cross Checking**
- **Test Case Generator**
- **Compiler Asm/Disasm**
- **Debugger IDE**
- **CPU ISS**
  (near-cycle accurate)
- **CPU RTL**

Extensible Baseline Components

- **Executable or library**
- **Source file**
Aggressive in RISC-V Community

Foundation Task Groups (partial list)

- Contributing hardware architecture extensions
  - Chair of the P-extension (Packed SIMD/DSP) Task Group
  - Co-chair of Fast Interrupts Task Group
  - Closely reviewing activities of other Task Groups
Andes Helps Strengthen RISC-V Ecosystem

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem
RISC-V Software Ecosystem: GNU Toolchain

- **GCC, binutils**: May, 2017
- **Newlib**: Aug, 2017
- **Glibc (rv64i)**: Feb, 2018
- **GDB**: Mar, 2018
- **OpenOCD**: July, 2018
- **Glibc (rv32i)**:
  - Submitted in July 2018 (by Andes)
  - Review in progress
RISC-V Software Ecosystem: LLVM Compilation

- **LLVM:**
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Change status into “official” from LLVM 9: Sep, 2019 (est.)

- **compiler-rt:** Mar, 2018

- **LLD:** Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation
- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)
Andes Position in RISC-V

Complete product portfolio

Reliable RISC-V core IP provider

Extreme low power consumption, high computing efficiency

World’s leading Customer-Extension Capable RISC-V Core
Two Ecosystems: Andes and Knect.me
Knect.me Ecosystem

- **Built up Ecosystem** **Knect.me** to help IoT Developing
  - to **Knect** solutions - Silicon IP’s, SW stacks, tools, applications, systems and products

- **Includes:**
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools

- **To Form a IoT League**
  - to **Knect** chip vendors, partners, application developers, system vendors

---

Knect.me Ecosystem

- Built up Ecosystem **Knect.me** to help IoT Developing
  - to **Knect** solutions - Silicon IP’s, SW stacks, tools, applications, systems and products

- Includes:
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools

- To Form a IoT League
  - to **Knect** chip vendors, partners, application developers, system vendors
FreeStart Program

- **FreeStart Evaluation Program (FSEP)**
  - For all RISC-V enthusiasms and educator/researcher
  - Good for N22 evaluation and research project
  - Fixed-Configuration N22 RTL
  - Sign simple evaluation agreement directly on website

- **FreeStart Mass-production Program (FSMP)**
  - For industrial and academy mass production
  - Full-configuration N22
  - License fee: $0; only running royalty is required when mass production

- **Support Package (FSSP)**
  - For all
  - $20K for 1st year, including
    - 1 year e-service
    - FreeStart AE250 RTL
    - Corvette F1 FPGA board

For more info., please visit [www.andestech.com](http://www.andestech.com)
2019 Event Promotion

RISC-V CON series
RISC-V Roadshow & Workshop Series
TSMC symposium & OIP series
Concluding Remarks
Andes: Trusted Computing Expert

- Andes stretched out for more opportunities in Q1~Q3’19 thru the launch of x6 new RISC-V cores, custom design service and FreeStart program.
- Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.
- Andes has successively signed >15 contracts with design service houses to authorize ASIC design to embed RISC-V core (i.e. Andes RISC-V EasyStart Program) for creating a "win-win" situation.
- Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry
Thank You!

www.andestech.com
Q&A