Andes Technology Corporation
3Q19 Investor Conference Report

Driving Innovations™

Stock #: 6533
2019/12/06

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

Agenda

- Overview of Andes Technology Corporation
- Operating Results
- Product Applications
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks

Overview of Andes Technology Corporation

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Just over 190 people; 80% are engineers.
- EETimes' Silicon 60 Hot Startups to Watch (2012)
- TSMC OIP Award "Partner of the Year" for New IP (2015)
- A founding member of RISC-V Foundation (2016)
- MCU innovation award by China online press (2018)

Andes Mission

- Innovate **performance-efficient** processor solution for **low-power** SoC

Emerging Opportunities

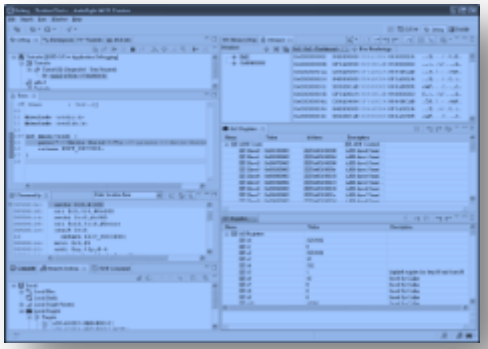
- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

Operating Results

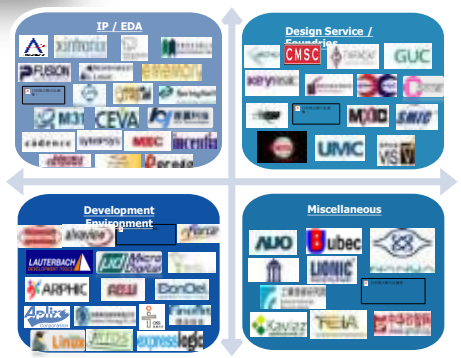
Business Status Overview

- **>160** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
  - **>300** license agreements signed

- AndeSight™ IDE:
  - >**17,000** installations

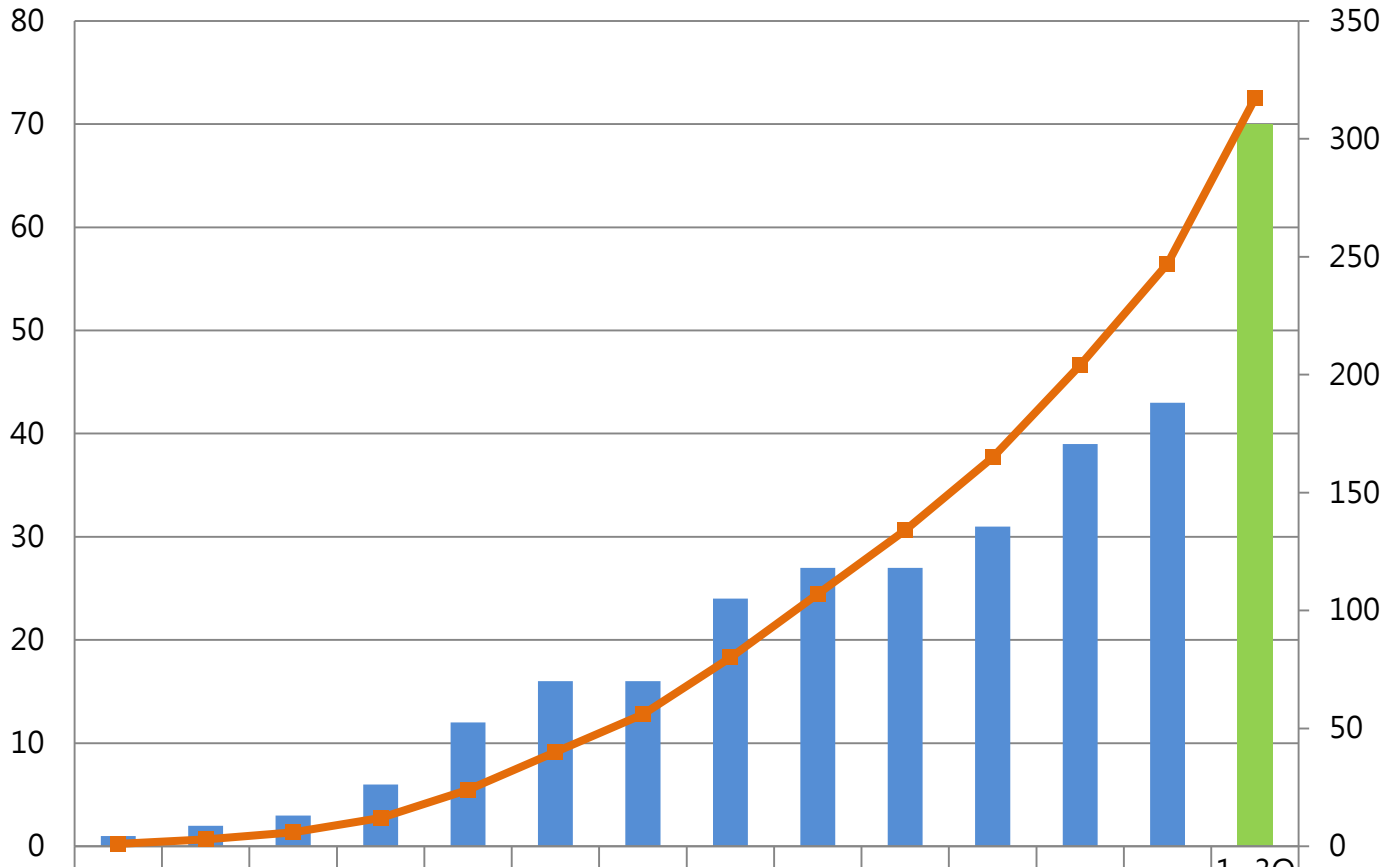


- Eco-system:
  - >**145** partners



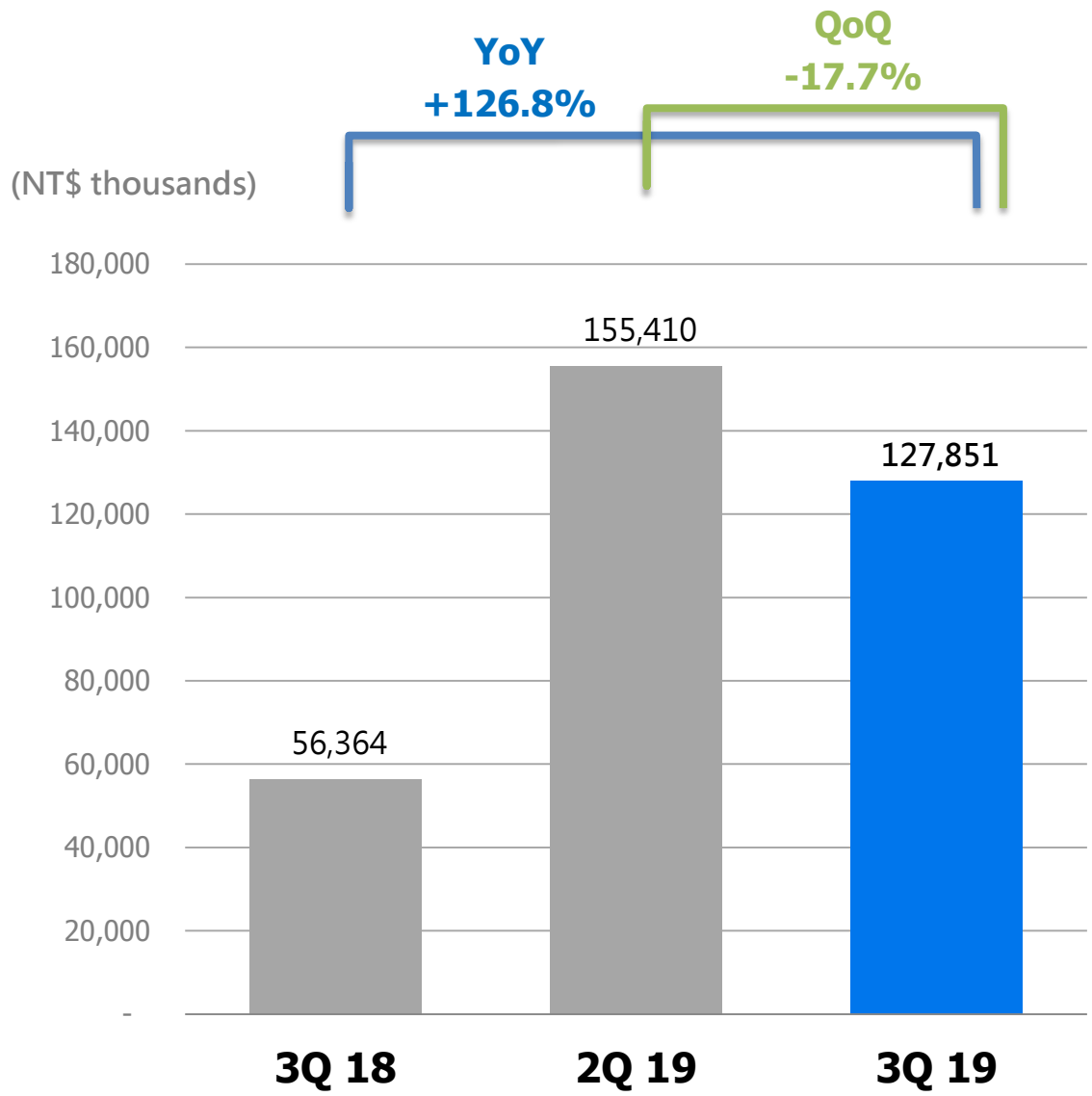
- **>4.5B** Accumulative SoC Shipped

Agreement Growth Analysis



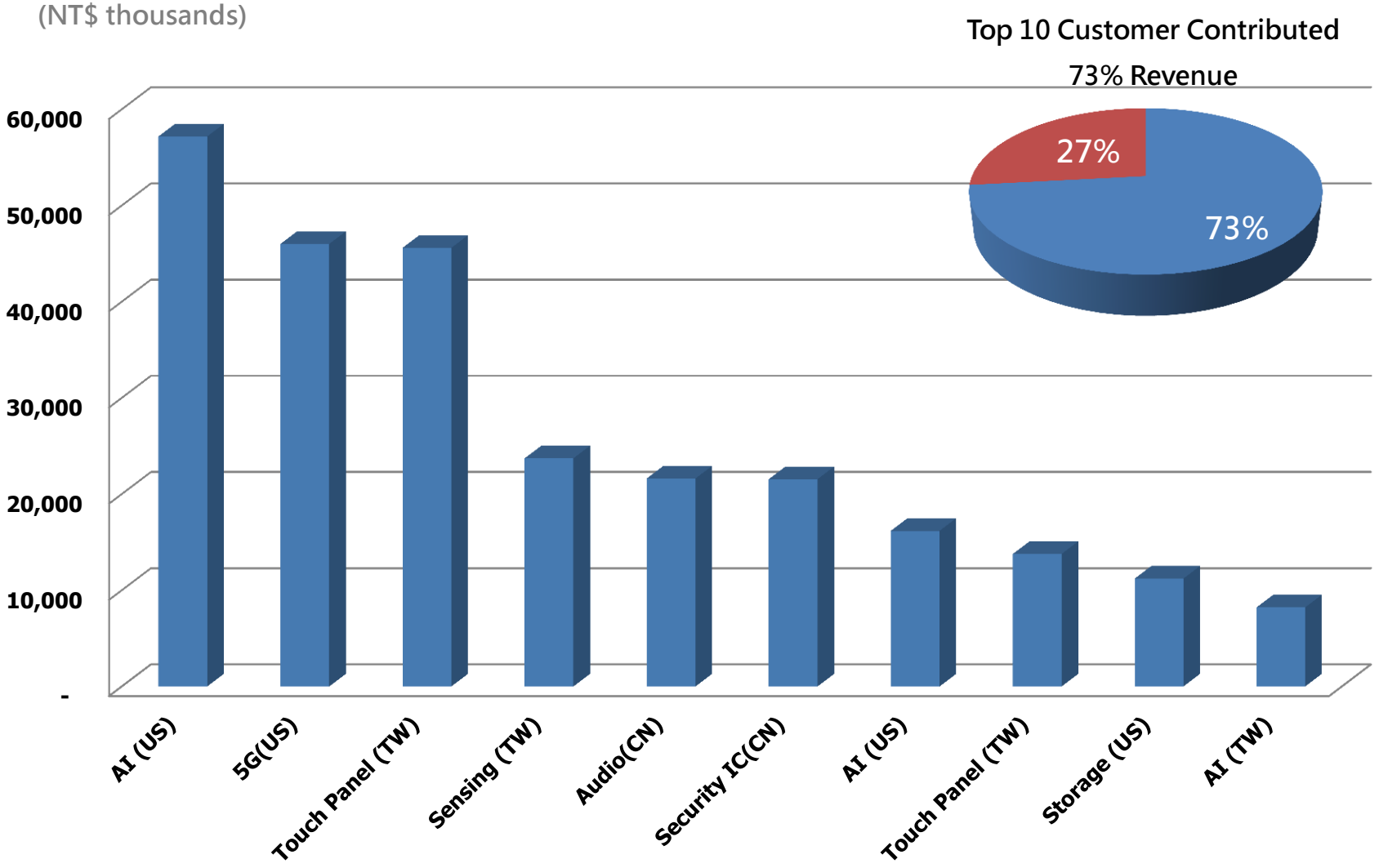
	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	1~3Q 2019
IP agreements	1	2	3	6	12	16	16	24	27	27	31	39	43	70
Accumulated IP agreements	1	3	6	12	24	40	56	80	107	134	165	204	247	317

2Q19 Revenue Analysis

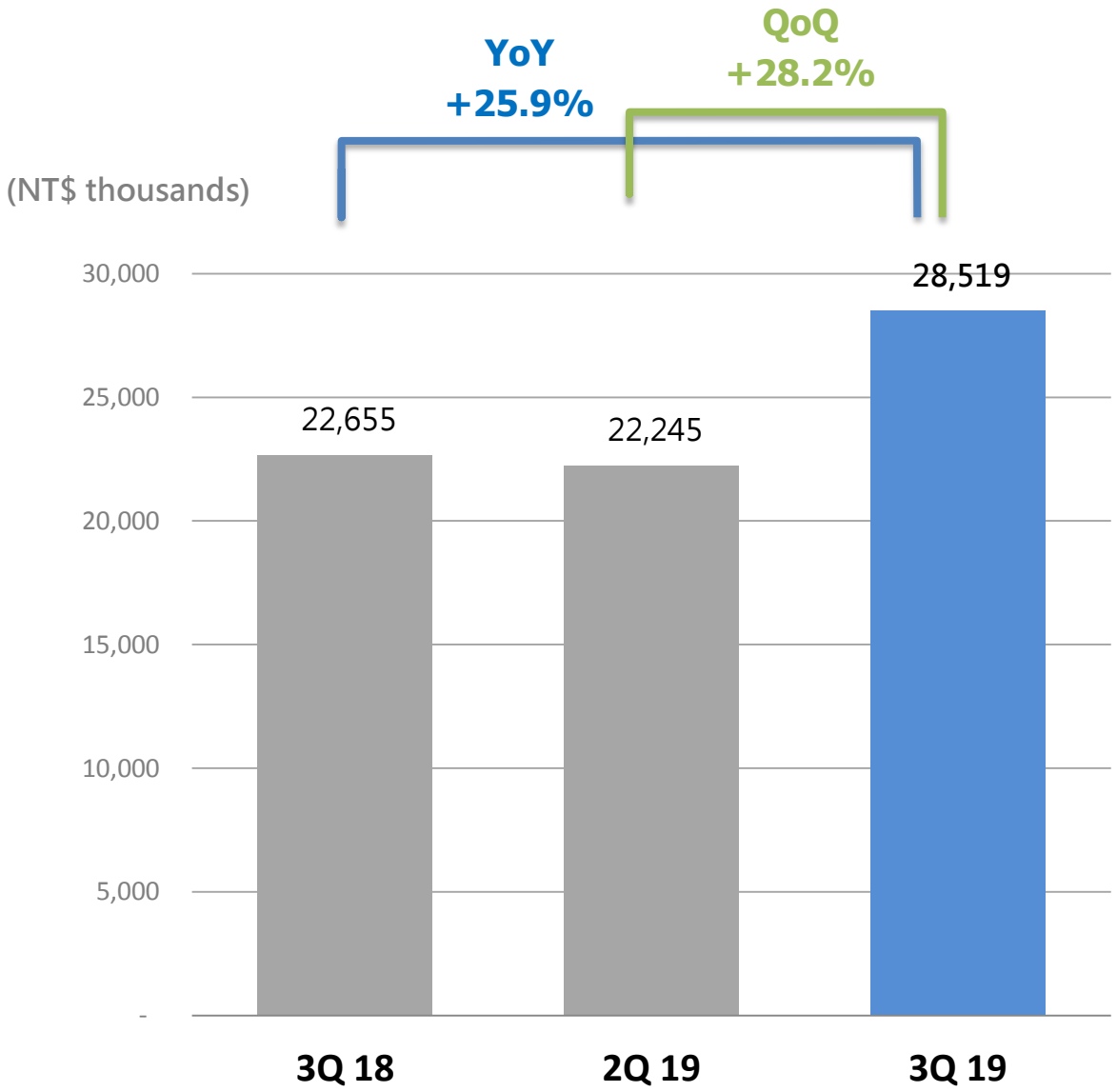


1-3Q19 Top 10 Customers Analysis by Revenue

(NT$ thousands)

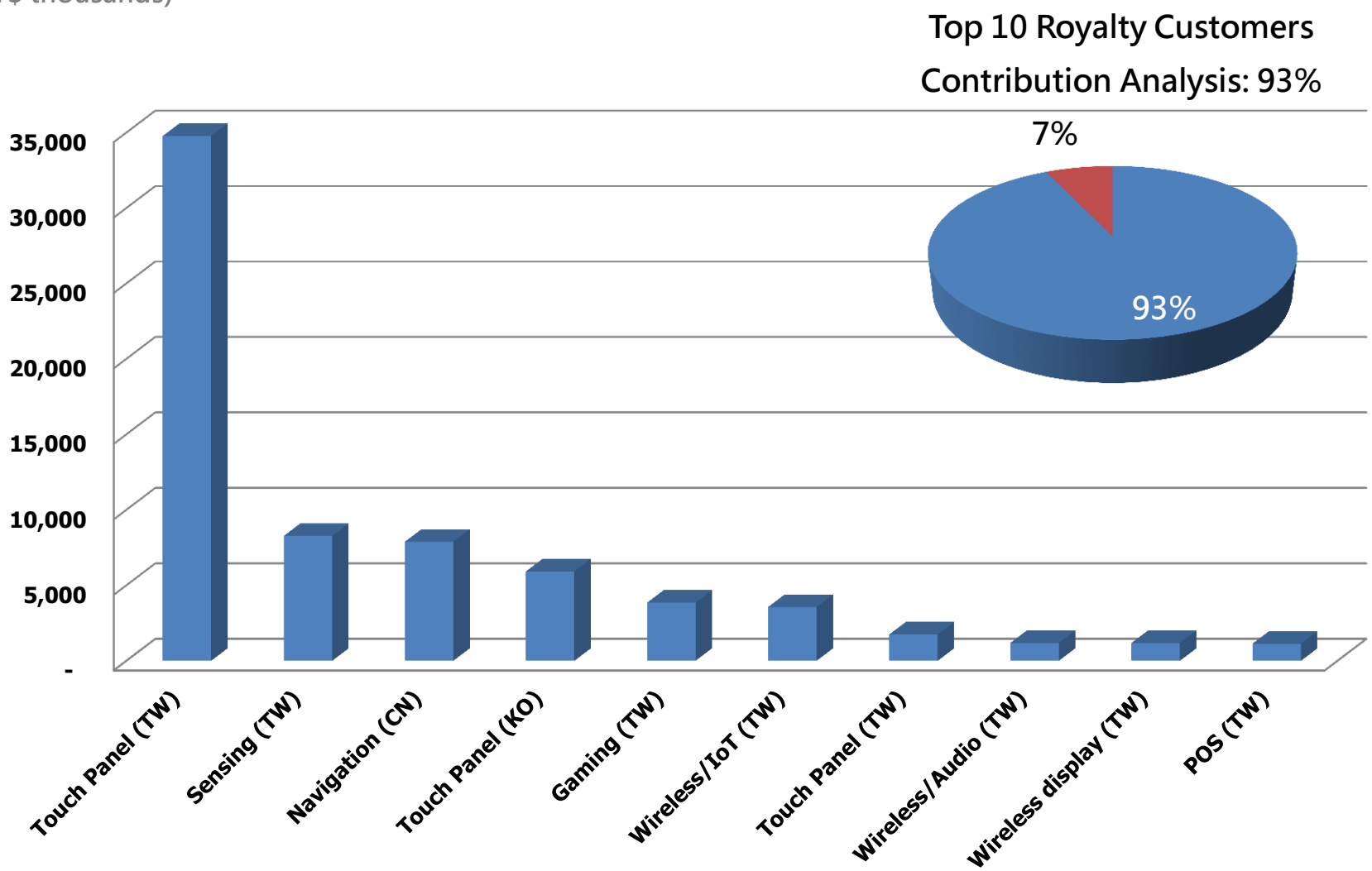


3Q19 Royalty Analysis



1-3Q19 Top Ten Royalty Contributors Analysis by Application

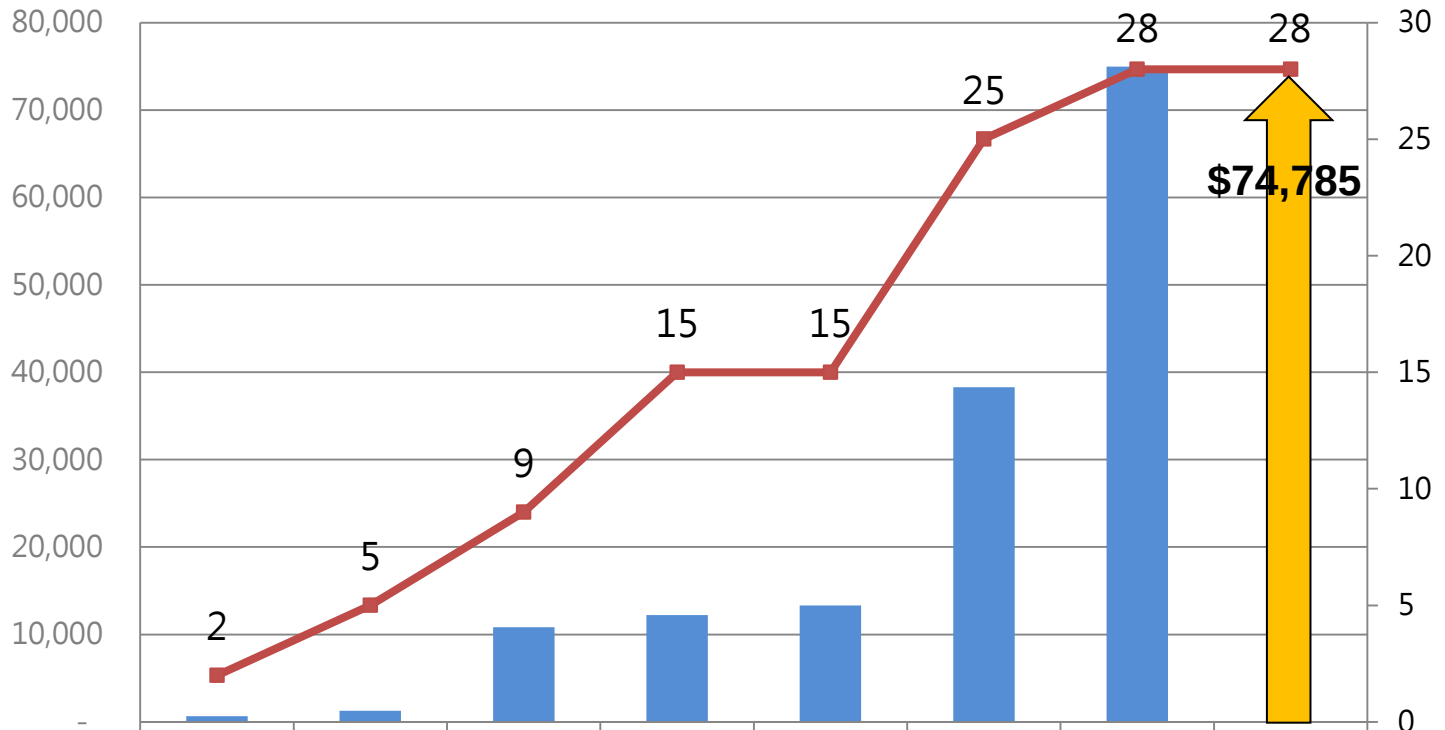
(NT$ thousands)



Royalty Analysis

(NT$ thousands)

: 2019 till Q3 royalty collected

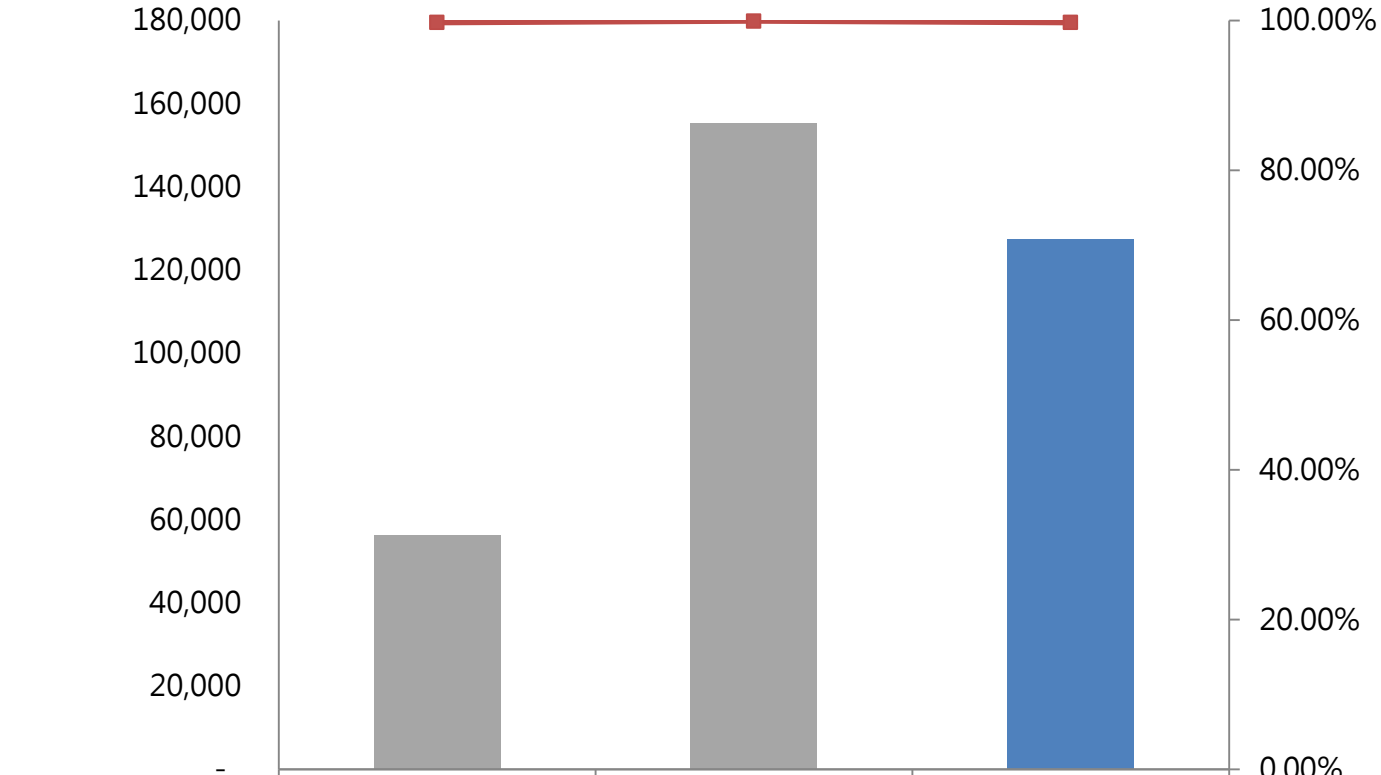


	2012	2013	2014	2015	2016	2017	2018	1-3Q 2019
Royalty	660	1,285	10,819	12,232	13,320	38,287	74,953	74,785
Customer numbers	2	5	9	15	15	25	28	28

(單位:家數)

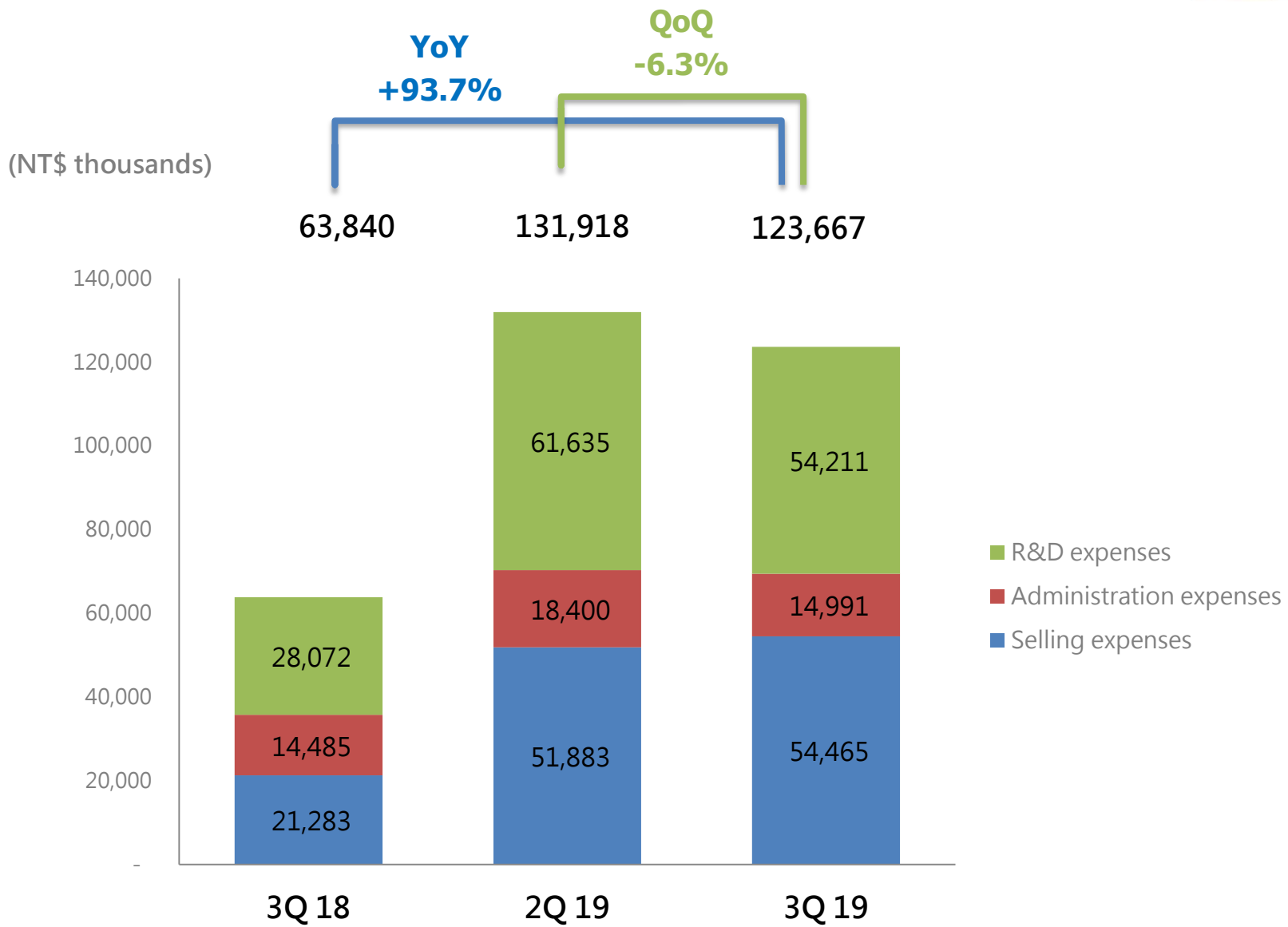
Consolidated Gross Margin

(NT$ thousands)

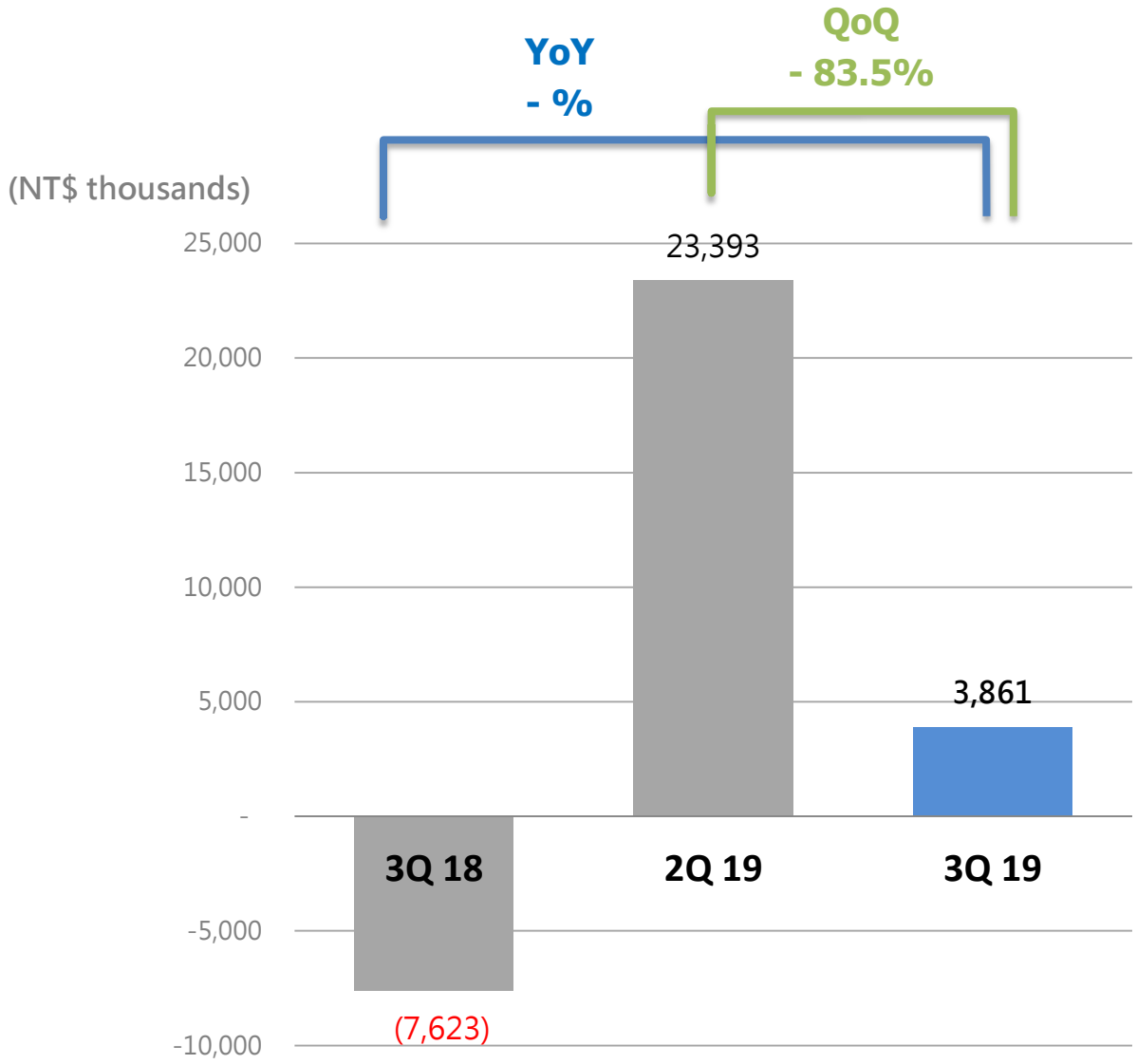


	3Q 18	2Q 19	3Q 19
Gross Profit	56,217	155,311	127,528
Gross Margin	99.74%	99.94%	99.75%

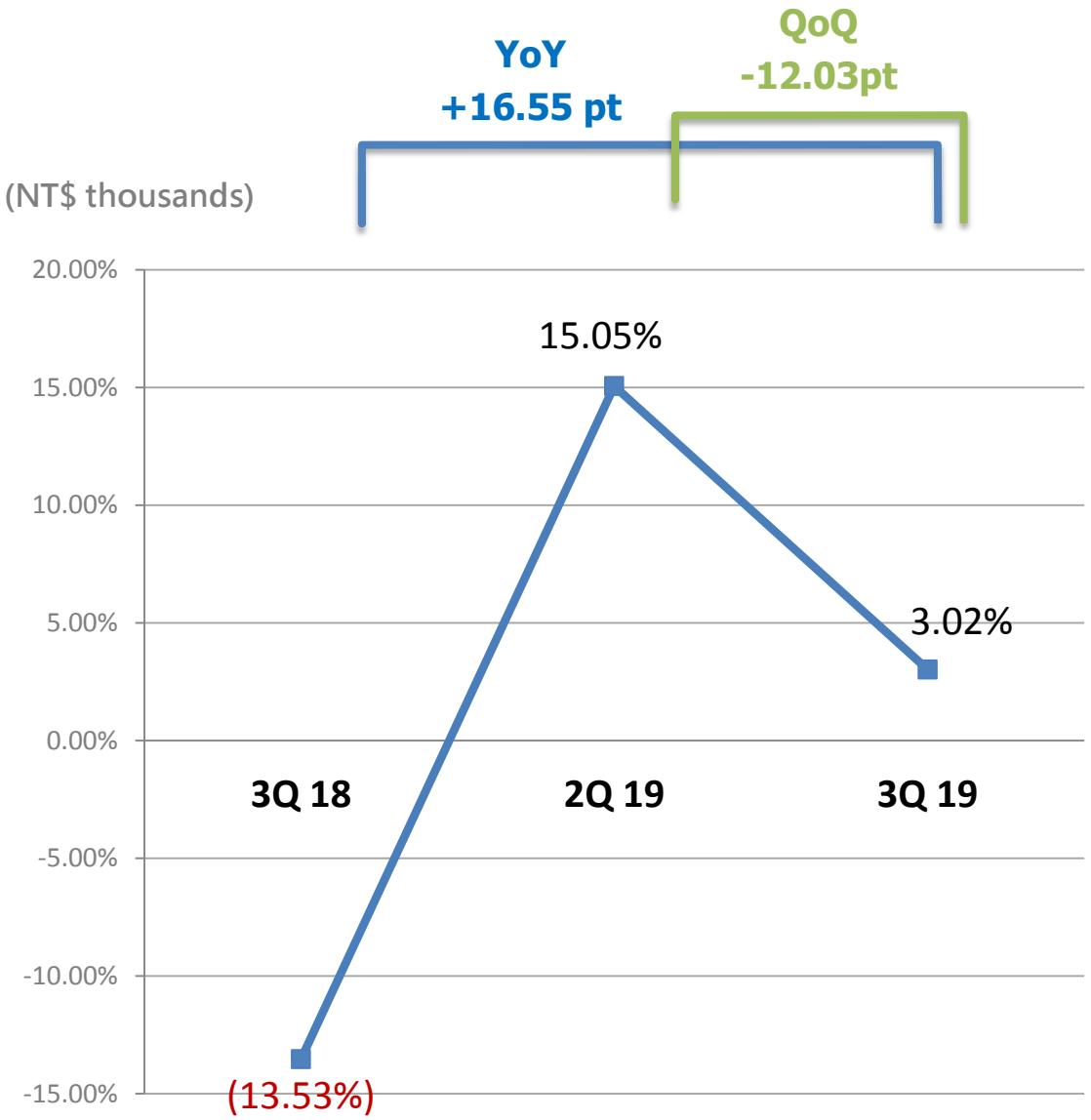
Consolidated Operating Expenses



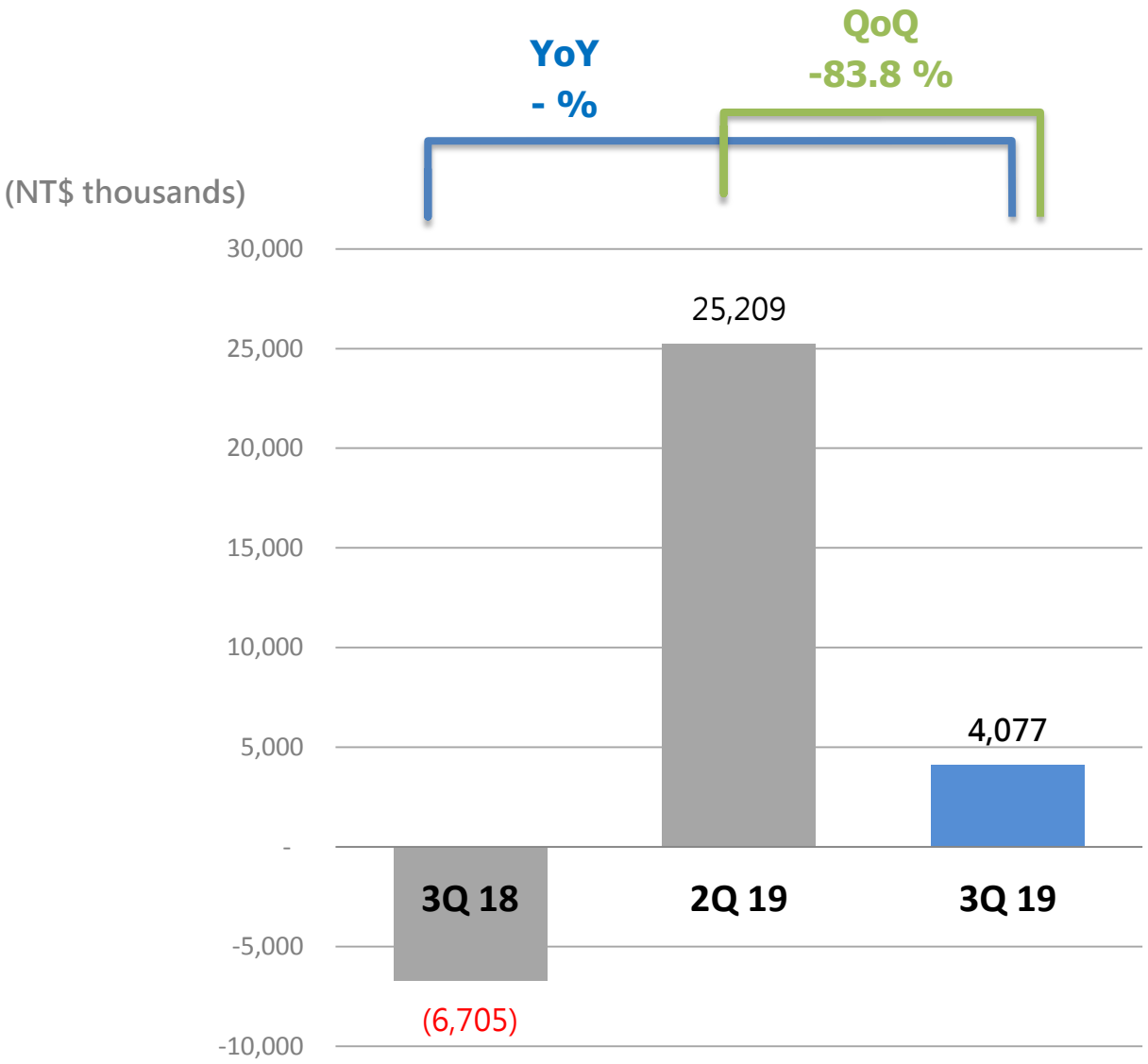
Consolidated Operating Income (Loss)



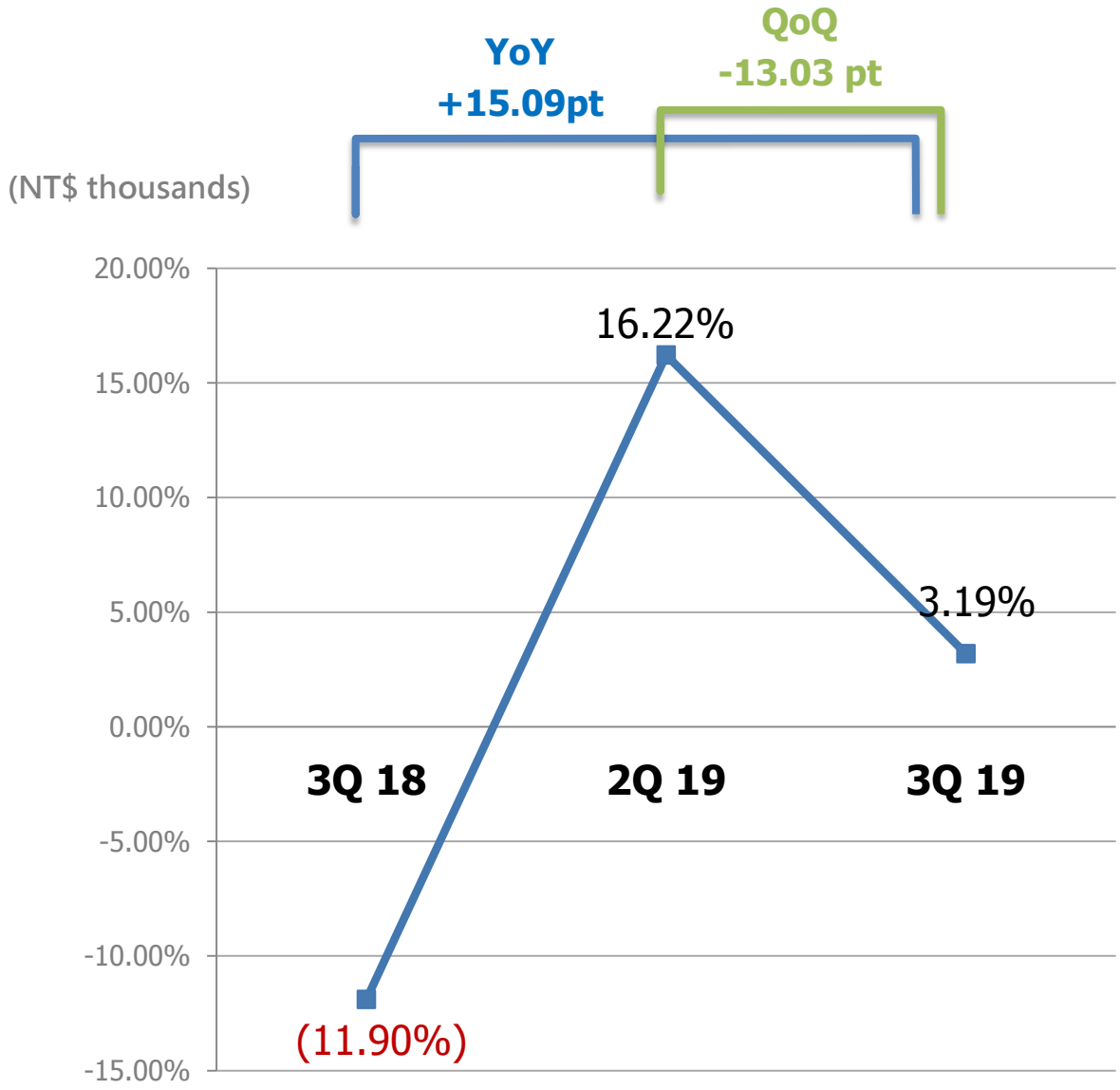
Consolidated Operating Margin



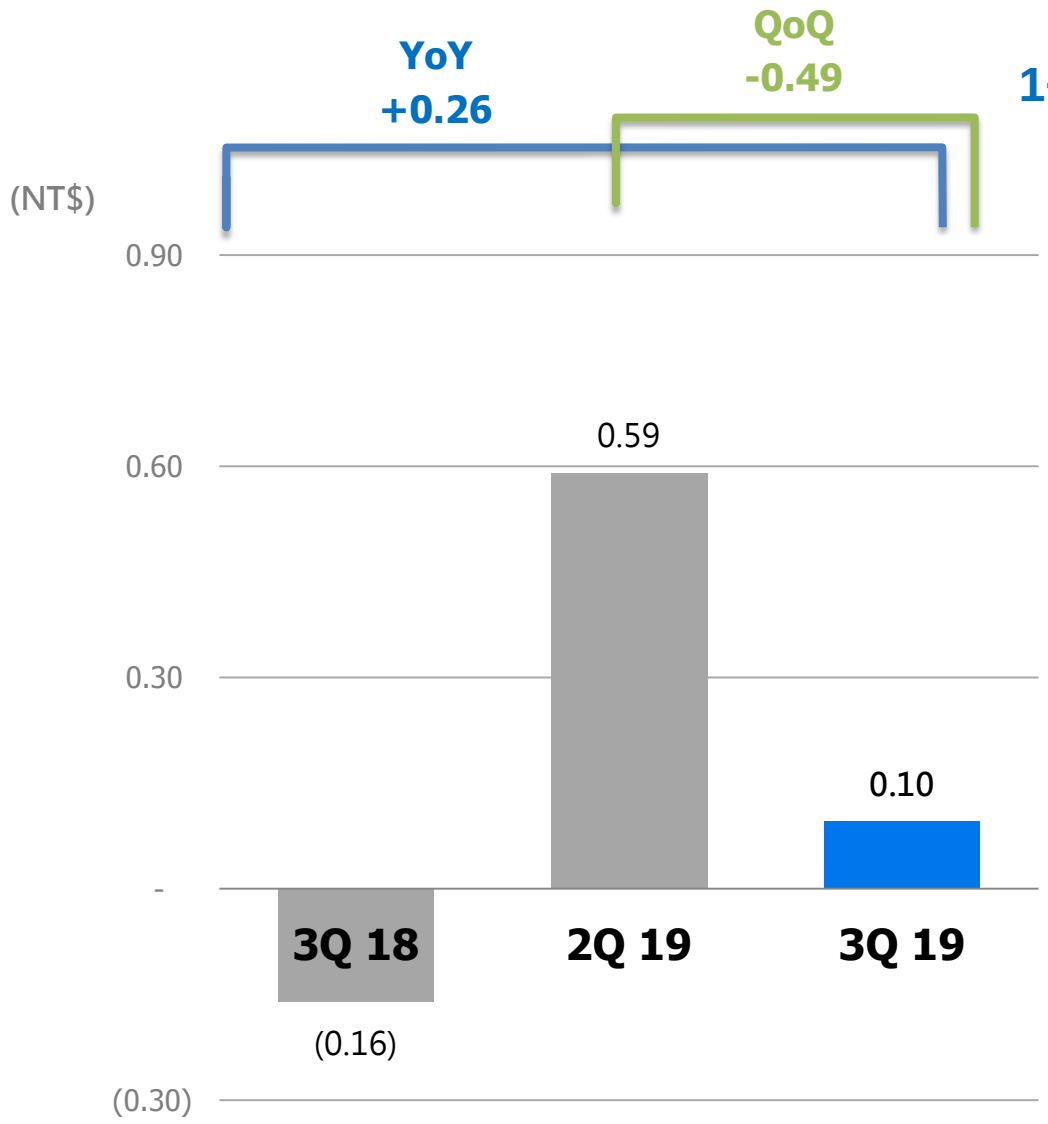
Consolidated Net Income (Loss)



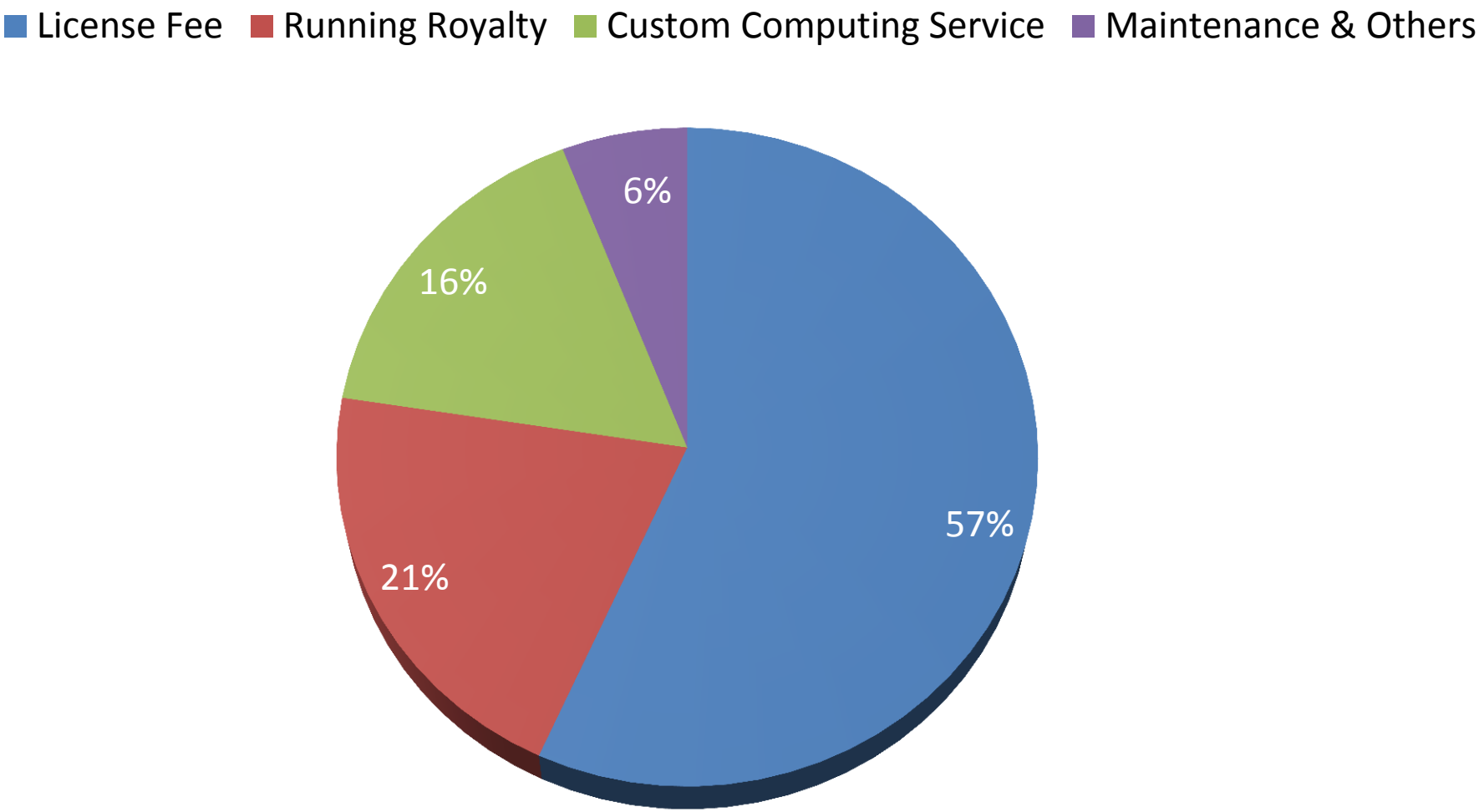
Consolidated Net Profit Margin



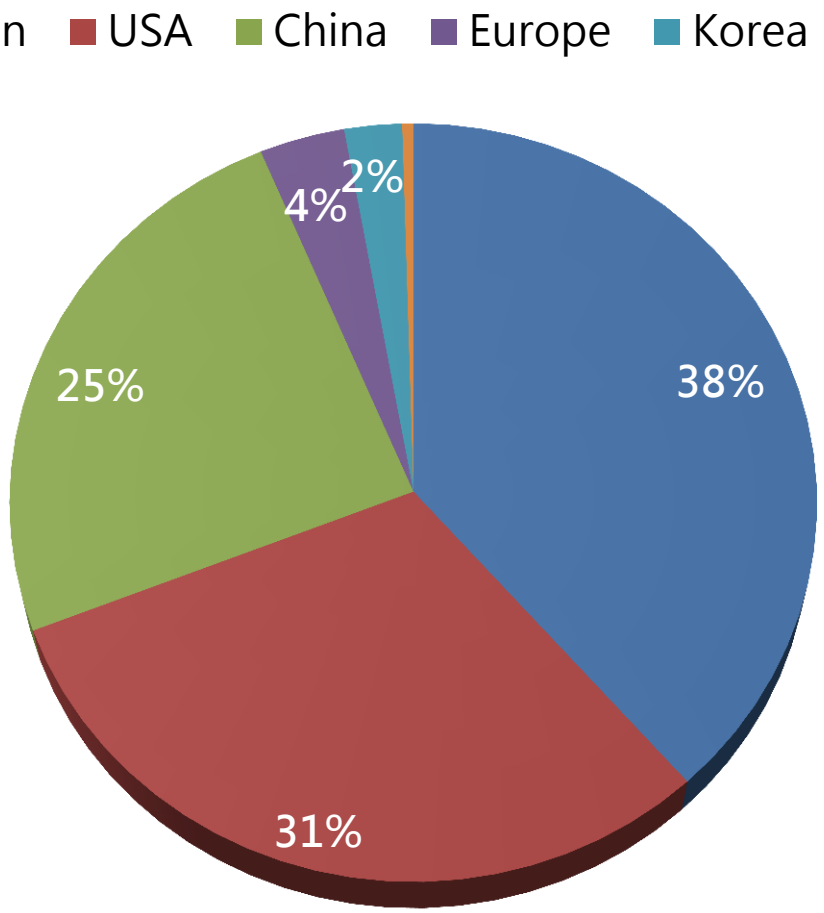
Consolidated Earnings Per Share



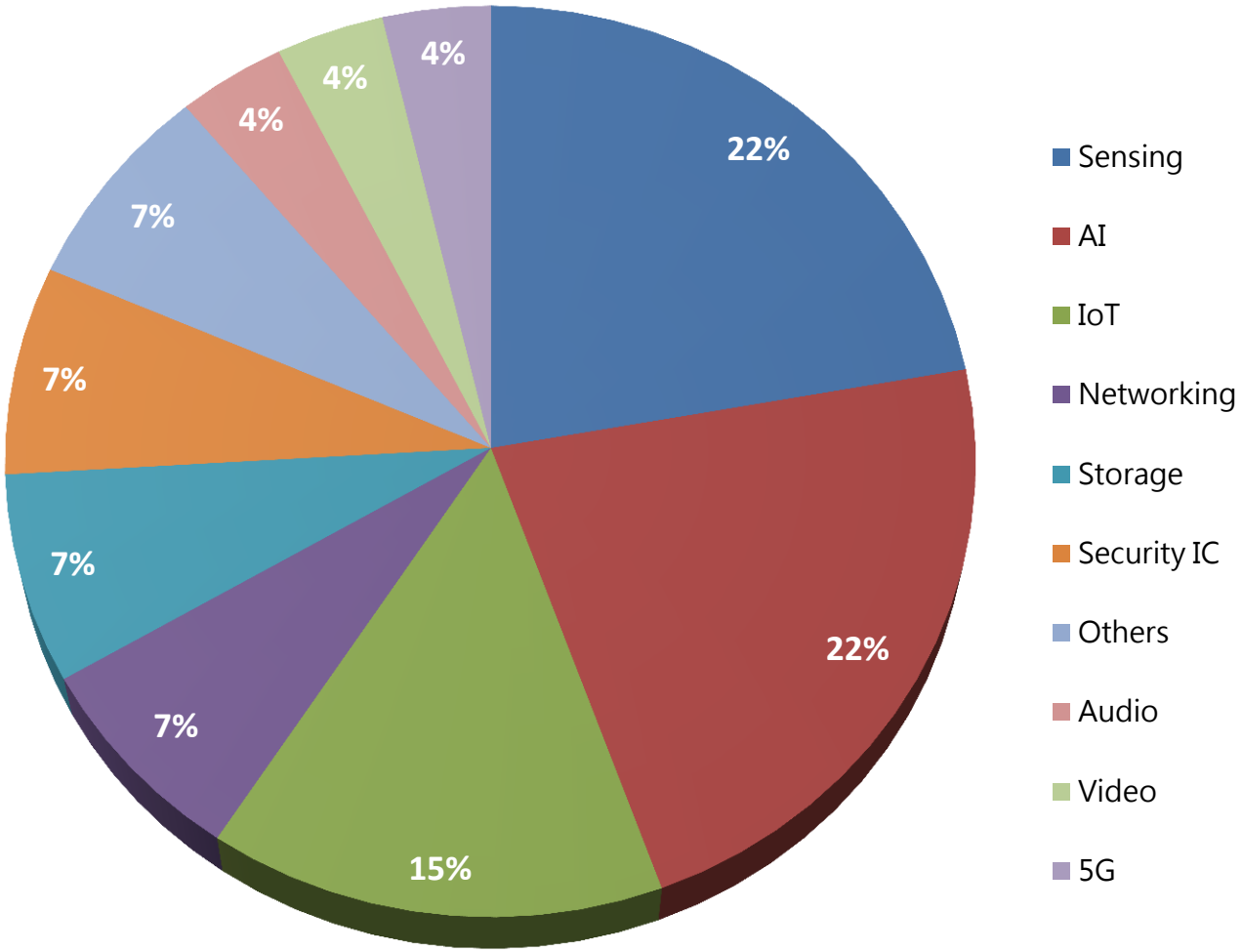
1-3Q 19 Revenue Analysis by Payment Model



1-3Q 19 Revenue Analysis by Region

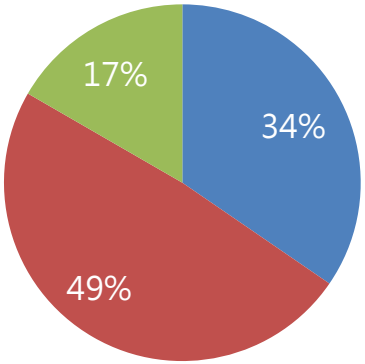


1-3Q19 Customer Application Analysis

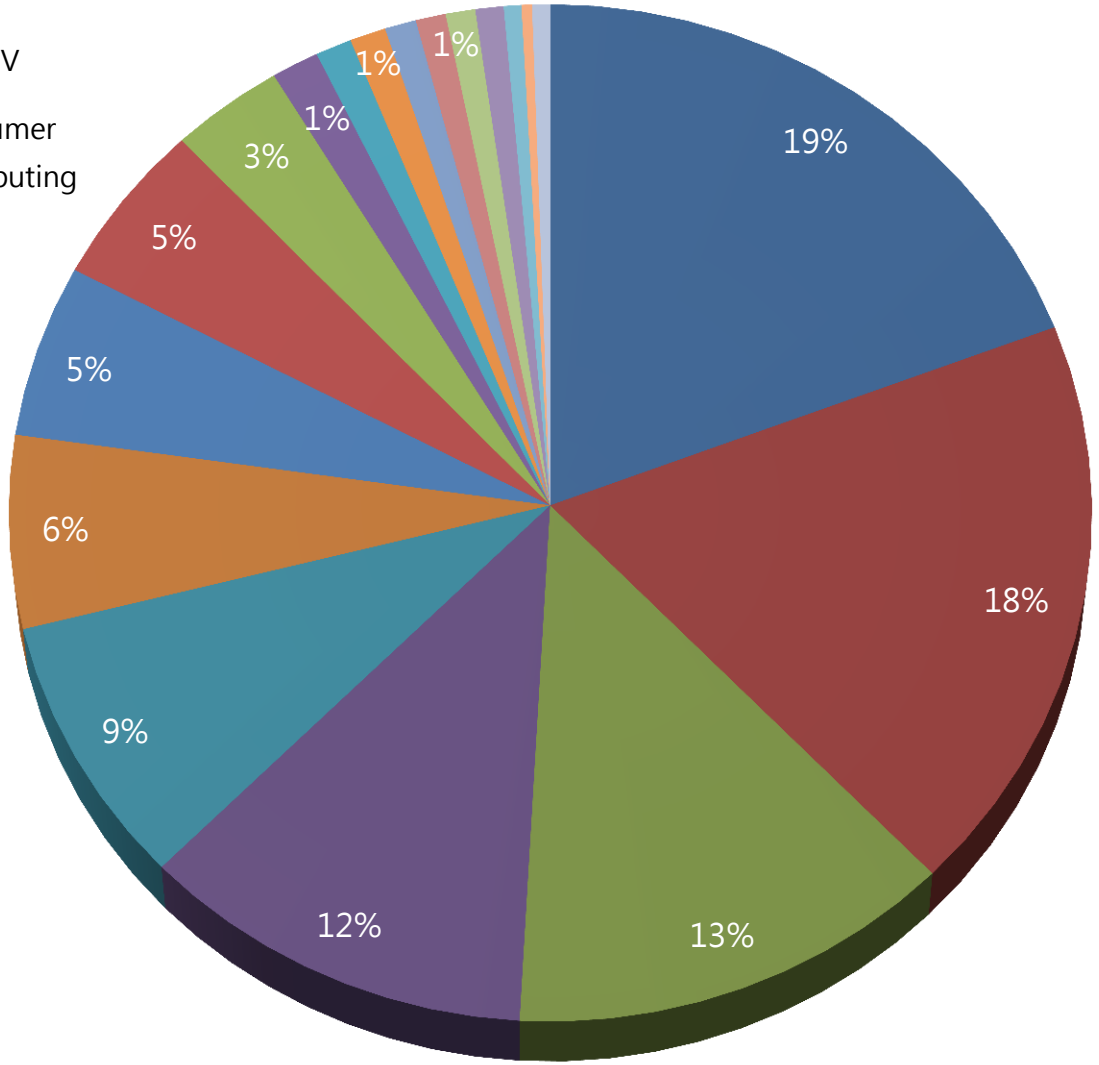


*Based on agreement number

1-3Q19 Revenue Analysis by Product

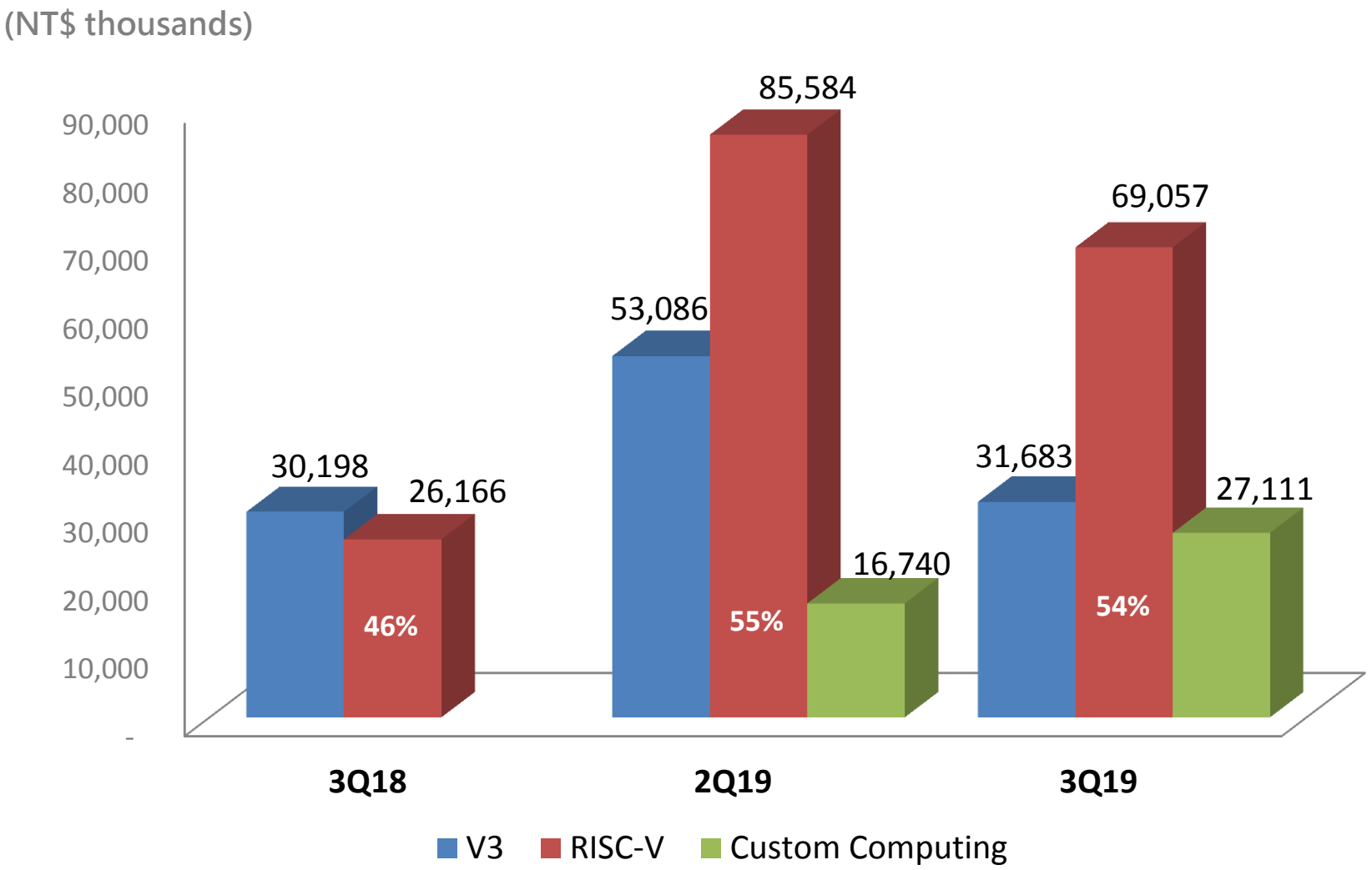


V3
RISC-V
Custumer Computing

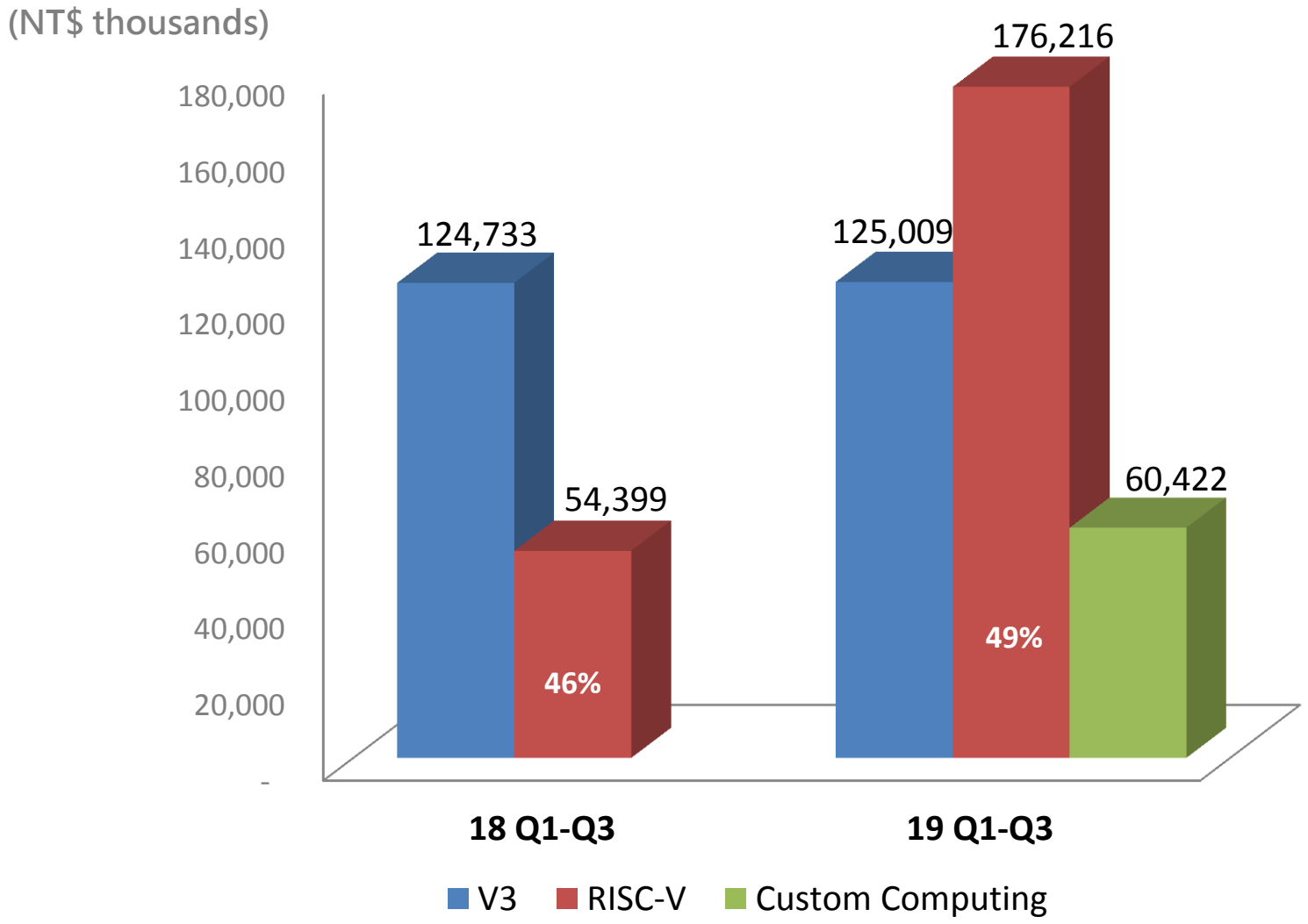


N8
N25
Service
D25
N9
NX25
AX25
ACE
TURBU
D10
S8
N15
N7
N22
N10
N13
EVB
N12
Other

3Q19 Revenue Analysis - RISC-V



1-3Q19 Revenue Analysis - RISC-V

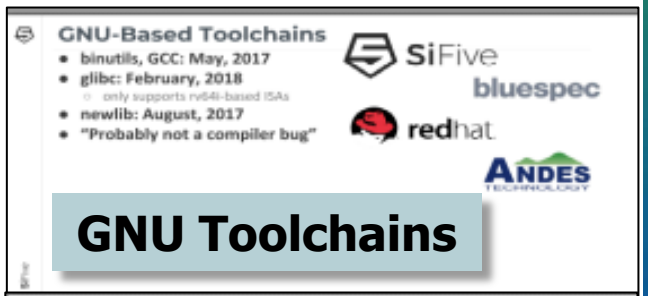


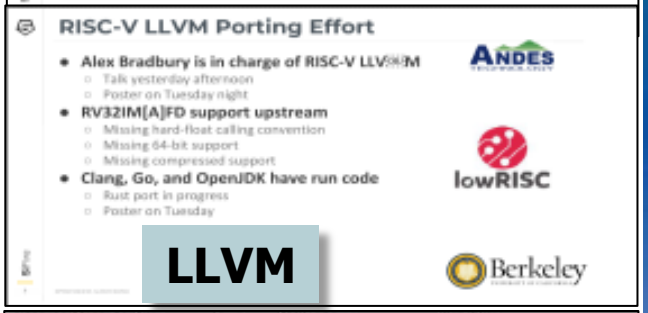
Product Application

Andes Updates

- A 14-year-old public CPU IP company

- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involvement in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group





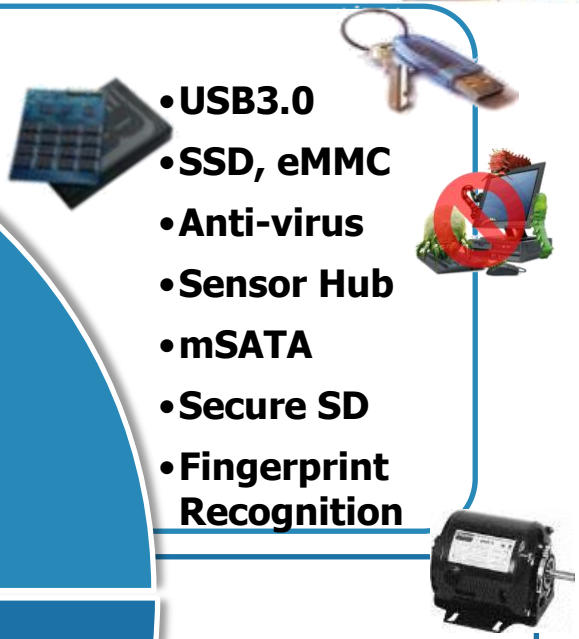
Example Applications of Andes-Embedded™ SoC

Consumer

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

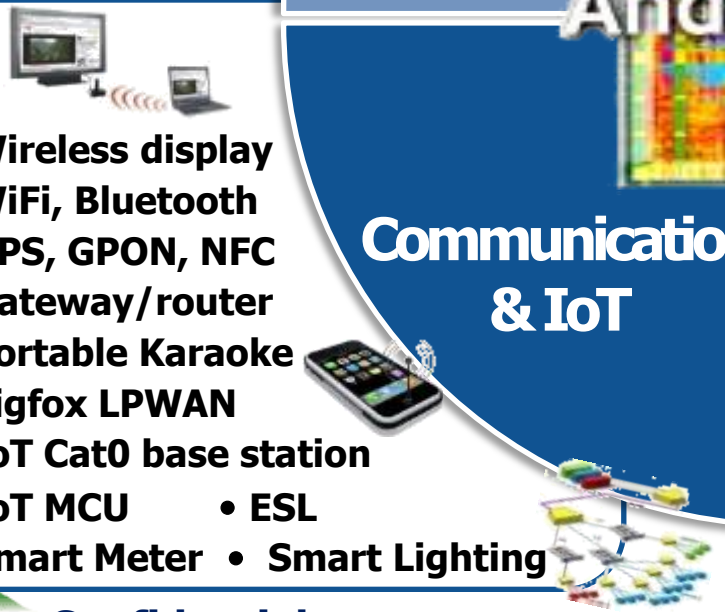
Storage & Sensor

- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition



Communication & IoT

- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU • ESL
- Smart Meter • Smart Lighting



Industrial & Video

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

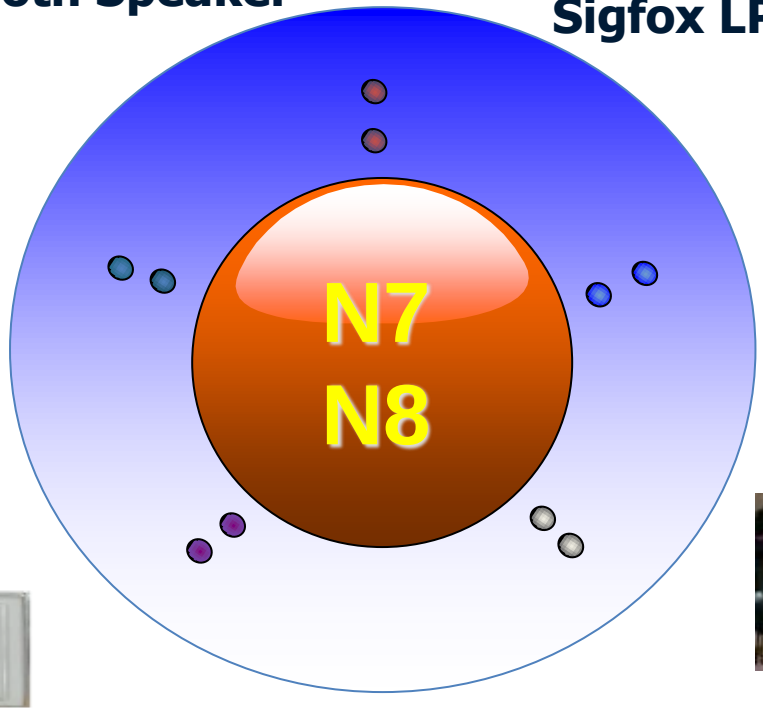
and more…..

IoT Application -1

Bluetooth Speaker

Sigfox LPWAN

Healthcare device



Wearable device

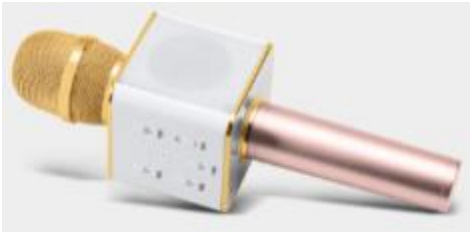
Electronic price tags

Sensor Hub

IoT Application -2

Wearable devices

Drone



Portable Karaoke

N9
D10

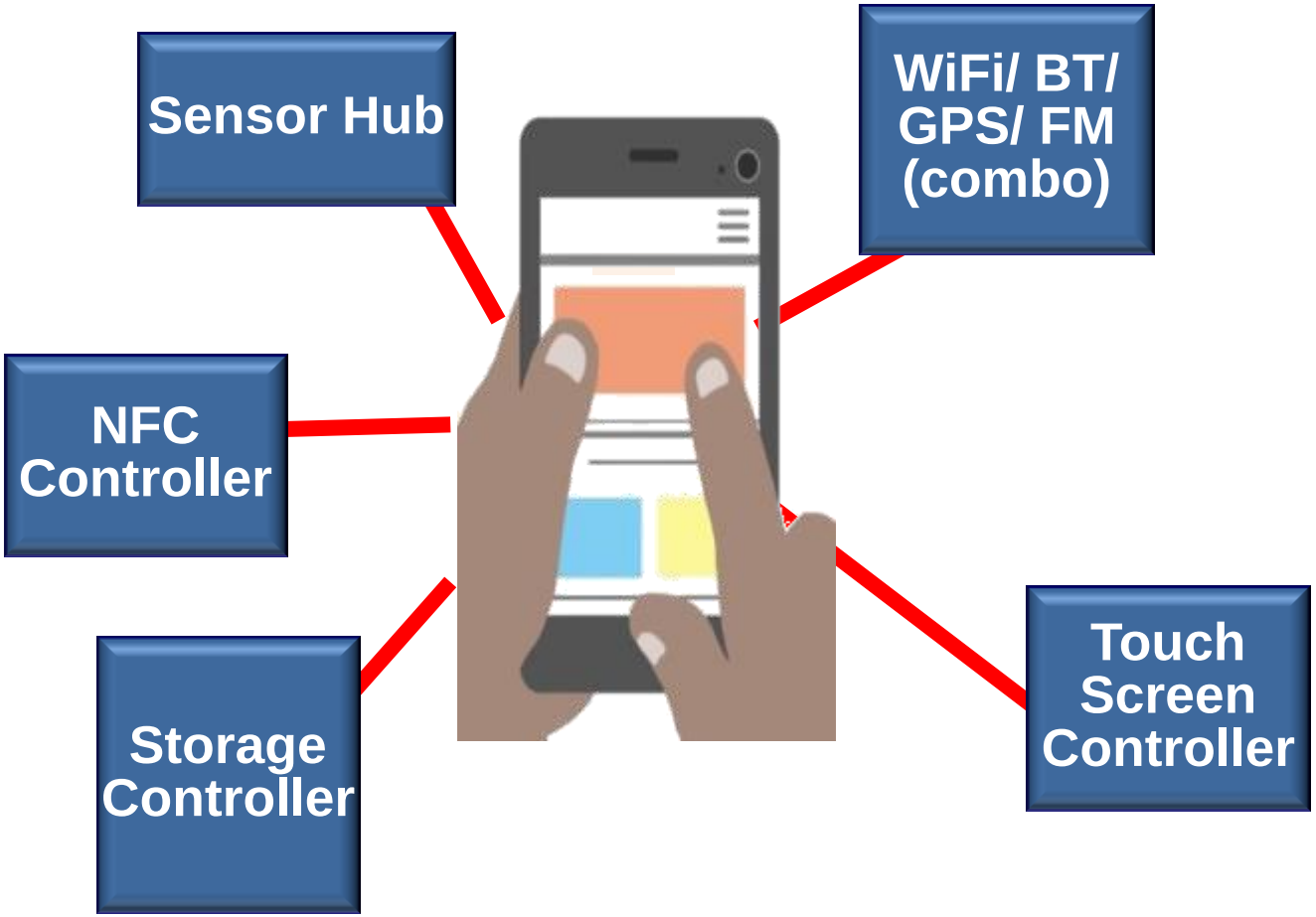
WiFi/GPS/FM/Bluetooth combo

GPS/Beido in shared bikes

Contactless payment (NFC)

Andes Embedded in Smart Phones

1 in 5 Smart Phones are with Andes Embedded



Andes Embedded
in Consumer Devices, Cars and Datacenters

Switch:
MXIC Flash Ctlr

Echo Dot2:
Mediatek WiFi IoT

Bike Sharing:
GPS Ctrl

X-Trail:
ADAS Ctlr

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

New Products and Ecosystems

Product Lines

- New A-series Cores released in Andes Embedded Forum 2018

ANDES

RISC-V

Andes RISC-V Product Overview

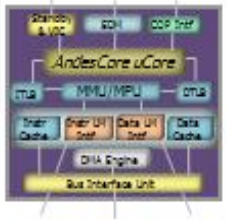
Best extensions to RISC-V

AndeStar™ Architecture V5

RISC-V

Highly optimized design with leading PPA

AndesCore™ Processors



AndeSight™ Tools

Professional IDE with high code quality

Andes Embedded™

Handy peripheral IPs to speed up SoC construction

Extensive SW stacks from bare metal, RTOS to Linux

AndeShape™ Platforms

AndeSoft™ Stacks

V5 AndesCore™ Processors

N22

N25F/NX25F/D25F

A25/AX25

A25MP/AX25MP

AndesCore™ RISC-V Families

Next-Gen

Cores with higher total performance and RISC-V ISA extensions

Higher performance

Cache-Coherent Multicores

A25MP
1/2/4 A25, L2$, L1/IO coherence

AX25MP
1/2/4 AX25, L2$, L1/IO coherence

Linux with FPU/DSP

A25
N25F, MMU, DSP

AX25
NX25F, MMU, DSP

Fast/Compact with FPU/DSP

N25F
V5/32b, FPU, PMP

D25F
N25F, DSP

NX25F
V5/64b, FPU, PMP

5-stage
>1.2GHz
3.58 CoreMark
2.09 DMIPS

Slim and Efficient

N22
V5[e], 32/16 GPR

2-stage
700MHz
3.95 CoreMark
1.80 DMIPS

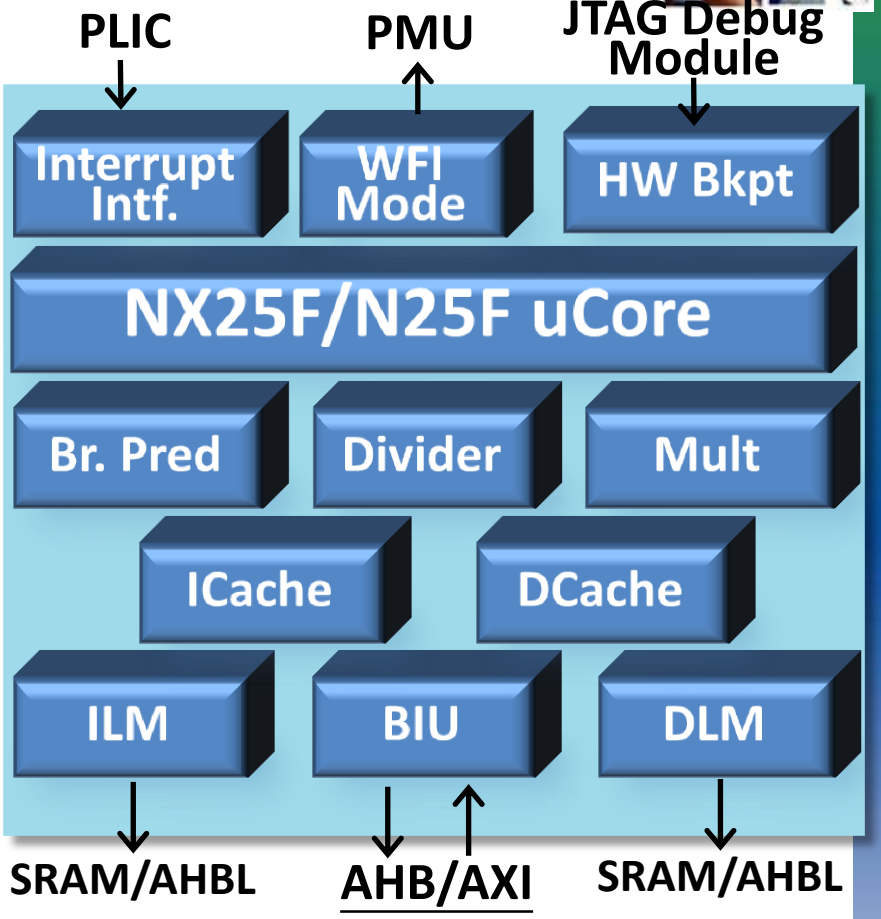
32bit 64bit

Bring Andes Strength to RISC-V Core Family

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure

V5 AndesCores: 25-series

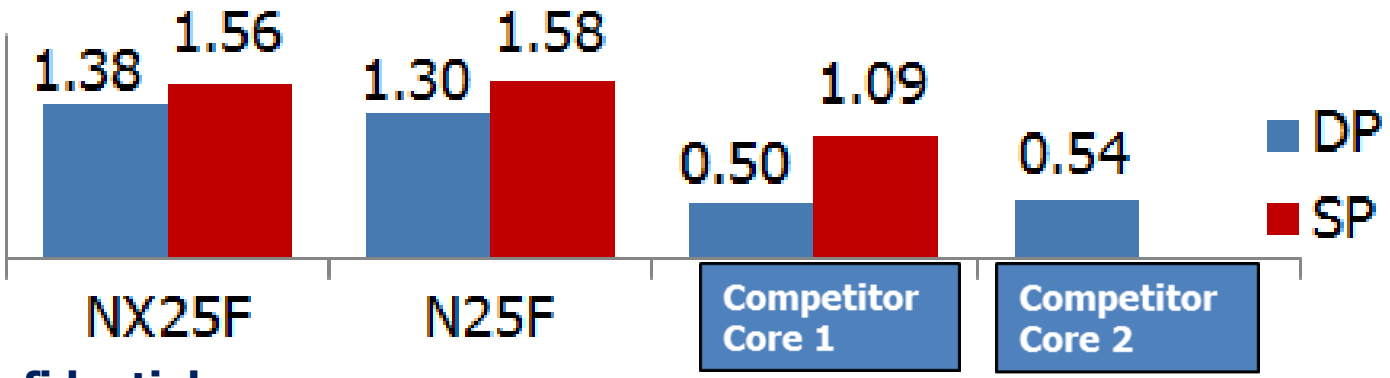
- **N25F: 32-bit, NX25F: 64-bit**
  - From scratch for the best PPA
  - Very configurable
- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses



- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case, w/o caches)
  - Large config: 136K gates, 1.2GHz (worst case, w/ caches)
  - **Best-in-class Coremark: 3.58/MHz**

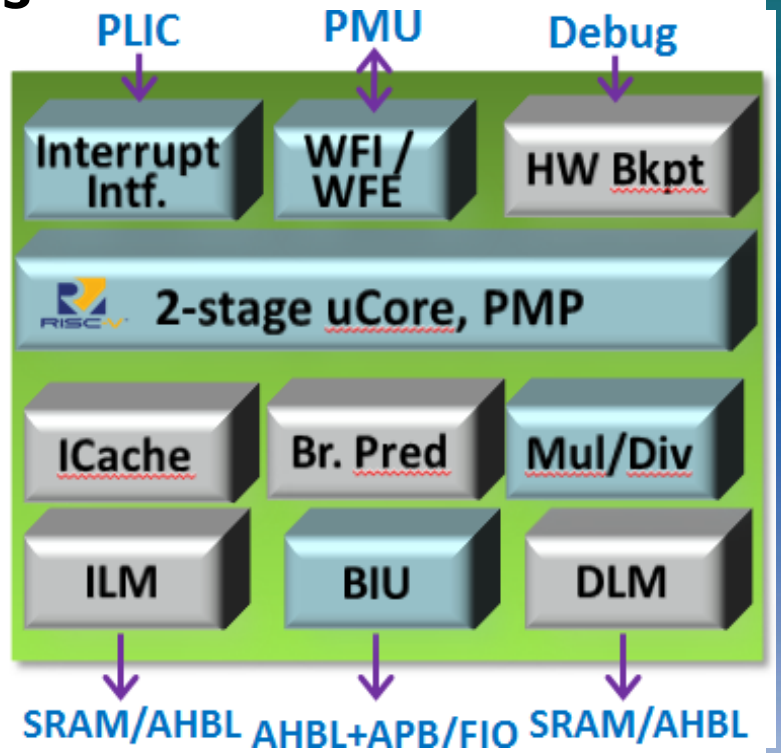
V5 AndesCores: 25-series

- **Fast-n-small for control tasks in AR/VR, networking, storage, AI**
- **N25F/NX25F: +FPU**
  - +, −, x, x+, x−: pipelined 4 cycles
  - ÷, √ : run in the background
    - ◆15 for SP, 29 for DP
- **A25/AX25: +FP +Linux**
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- **Whetstone/MHz**:



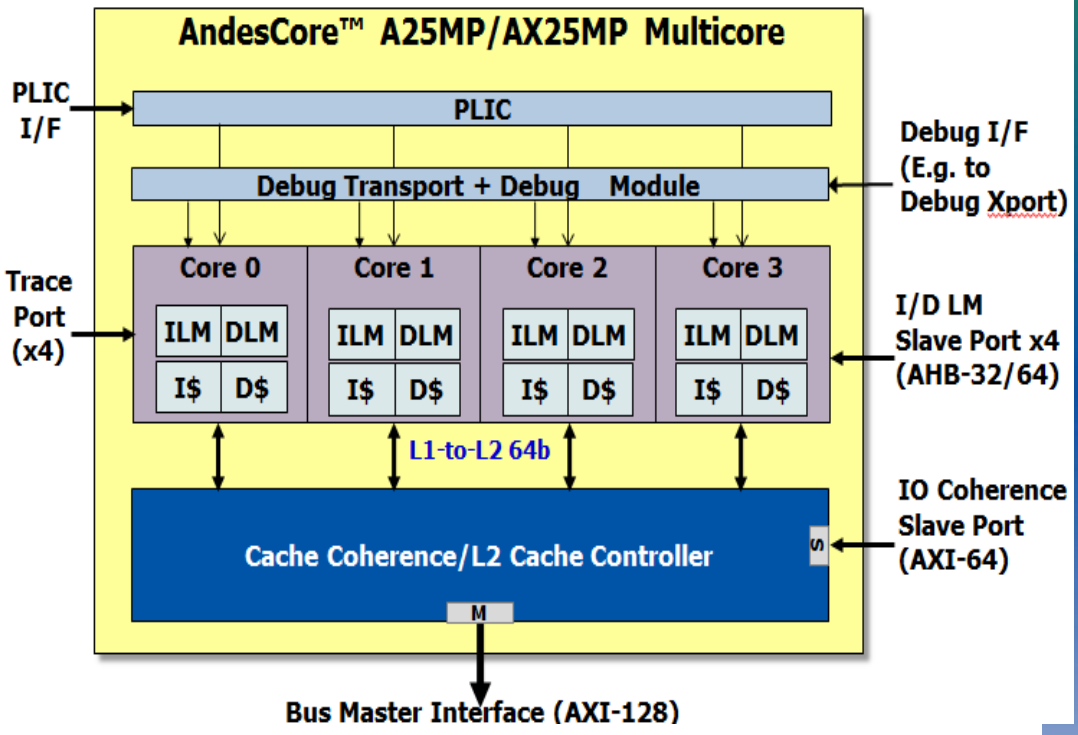
V5 AndesCores: 22-series

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension
- **2-stage pipeline with AHB-lite main bus**
- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller
- **28nm PPA:**
  - **700 MHz** (worst case)
  - **16K gates** (minimal)
- **Best per-MHz performance:**
  - **1.8 DMIPS** (no inline)
  - **3.95 Coremark**



A(X)25MP Cache-Coherent Multicore

- **1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs**
  - RV-GCP ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V
- **Hardware Multicore Cache Coherence**
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches
- **Level-2 Cache Controller**
  - 0/128/256K…2MB, 32-byte line, 16-way
  - ECC, SECDED support
- **Bus Interfaces**
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio
- **Platform Level Interrupt, Debug and Trace Support**



ACE: Andes Custom Extension

Verilog user.v

concise RTL

semantics, operands, test-case spec

script user.ace

COPILOT

Custom-OPtimized Instruction deveLOpment Tools

Automated Env. For Cross Checking

Test Case Generator

Extended RTL

Extended ISS

Extended Tools

Extended ISS

Extended RTL

Compiler Asm/Disasm Debugger IDE

CPU ISS (near-cycle accurate)

CPU RTL

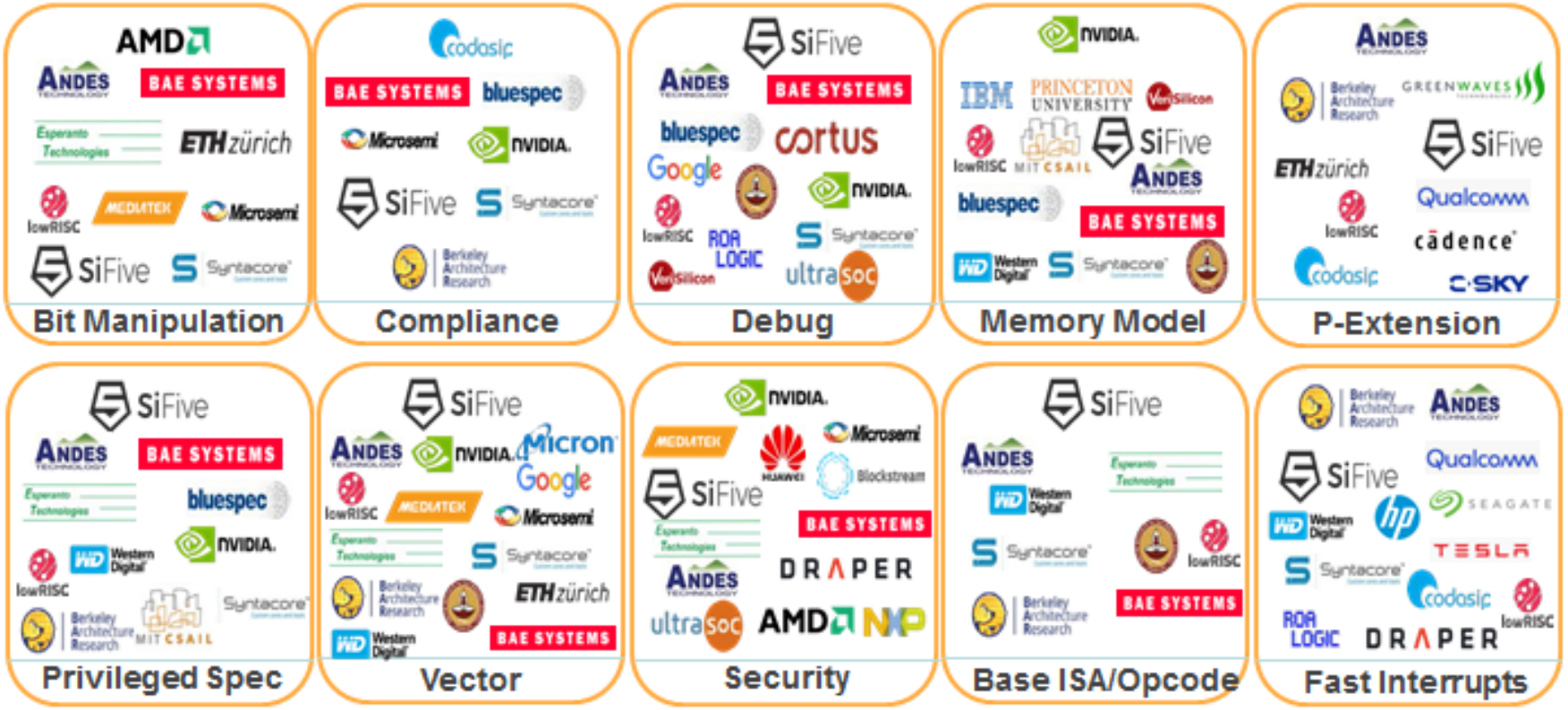
Extensible Baseline Components

Executable or library

Source file

Aggressive in RISC-V Community

Foundation Task Groups (partial list)



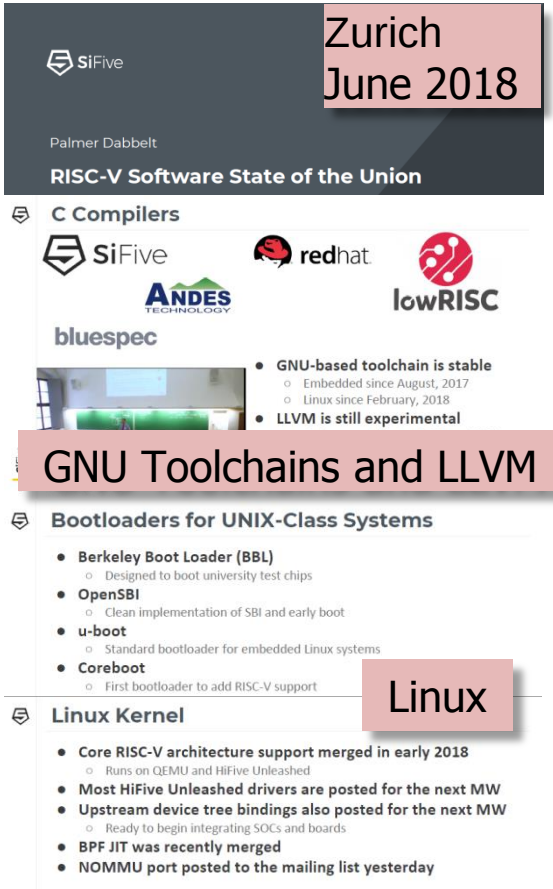
- **Contributing hardware architecture extensions**
  - **Chair of the P-extension (Packed SIMD/DSP) Task Group**
  - **Co-chair of Fast Interrupts Task Group**
  - **Closely reviewing activities of other Task Groups**

Andes Helps Strengthen RISC-V Ecosystem

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem

RISC-V Software Ecosystem: GNU Toolchain

- **GCC, binutils**: May, 2017
- **Newlib**: Aug, 2017
- **Glibc (rv64i)**: Feb, 2018
- **GDB**: Mar, 2018
- **OpenOCD**: July, 2018
- **Glibc (rv32i)**:
  - Submitted in July 2018 (by Andes)
  - Review in progress



ANDES TECHNOLOGY

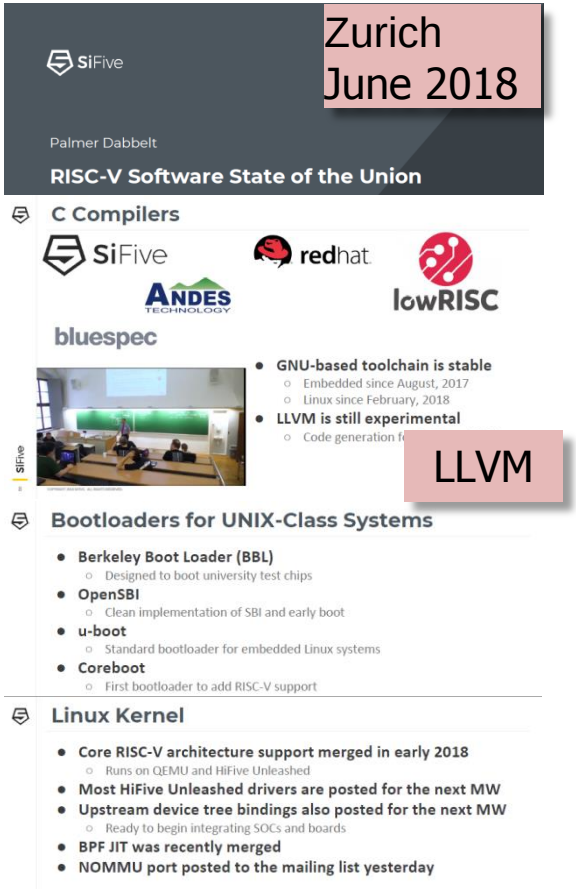
bluespec

redhat

SiFive

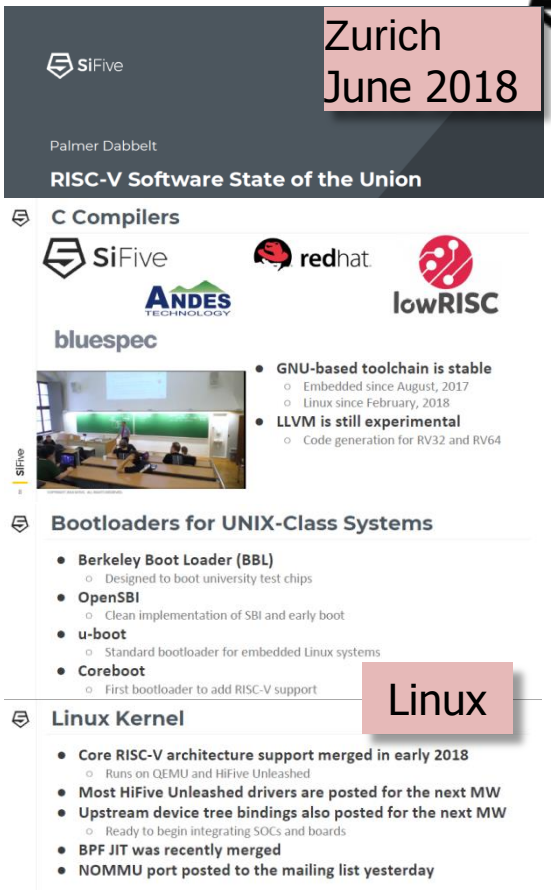
RISC-V Software Ecosystem: LLVM Compilation

- **LLVM**:
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Change status into "official" from LLVM 9: Sep, 2019 (est.)
- **compiler-rt**: Mar, 2018
- **LLD**: Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation



RISC-V System Software Ecosystem: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)



Linux

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WD

Andes Position in RISC-V

Complete product portfolio

Reliable RISC-V core IP provider

Extreme low power consumption, high computing efficiency

World's leading Customer-Extension Capable RISC-V Core

RISC-V

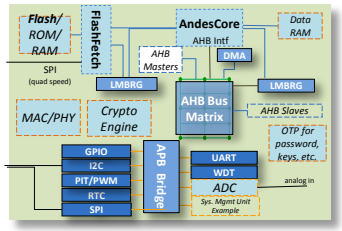
Two Ecosystems: Andes and Knect.me

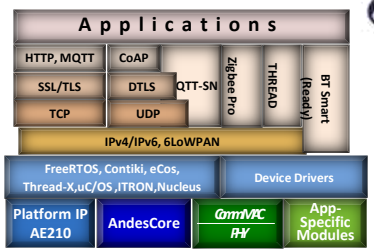
ANDES TECHNOLOGY

knectme™

Knect.me Ecosystem

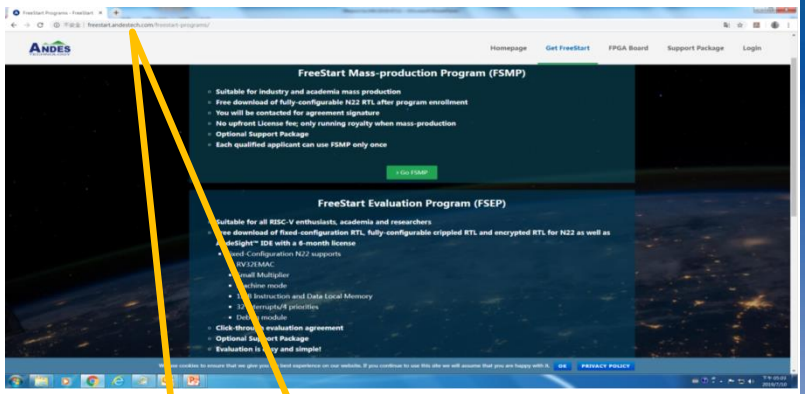
- **Built up Ecosystem *knect.me* to help IoT Developing**
  - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products
- **Includes:**
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools
- **To Form a IoT League**
  - to **knect** chip vendors, partners, application developers, system vendors





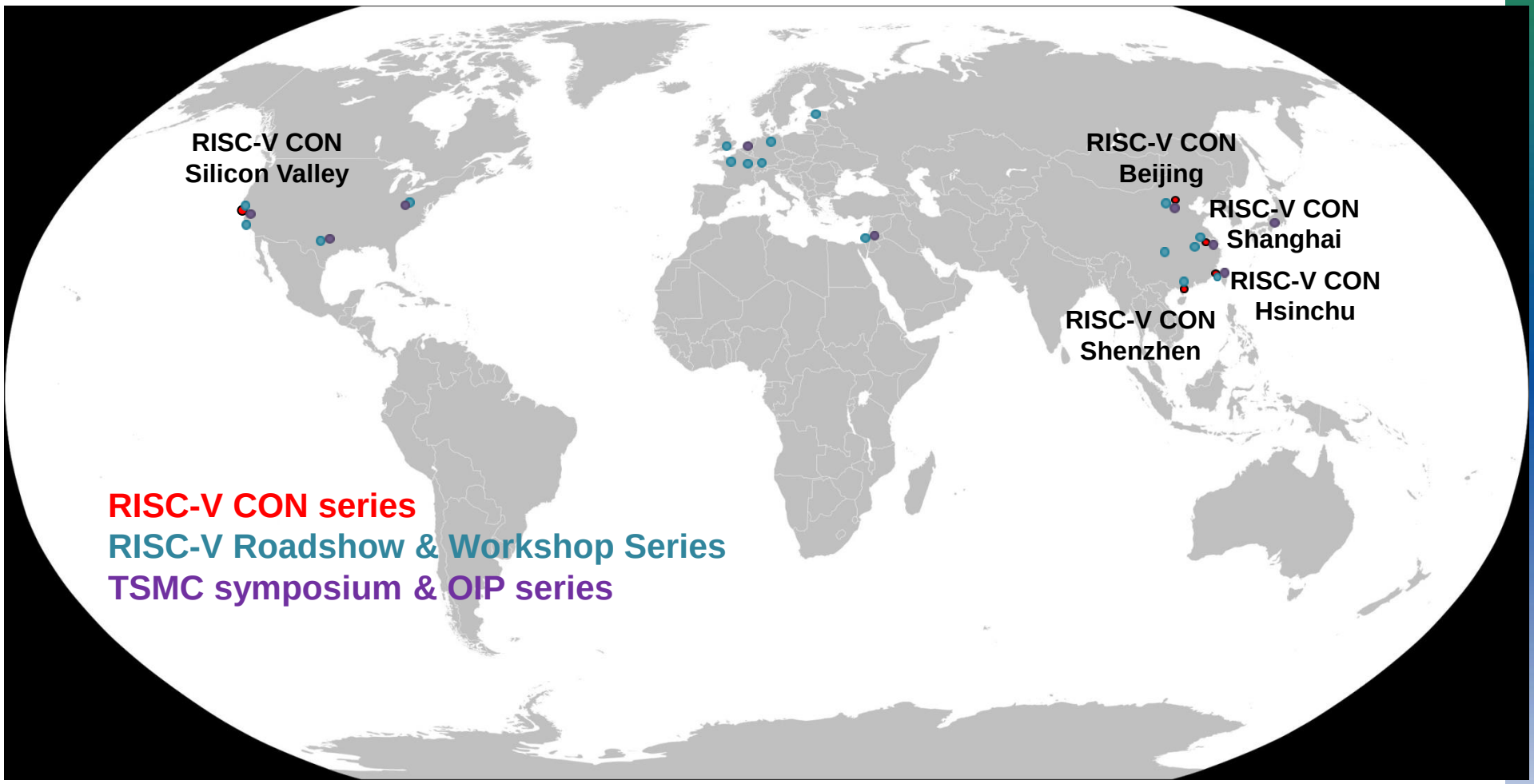
FreeStart Program

- **FreeStart Evaluation Program (FSEP)**
  - For all RISC-V enthusiasms and educator/researcher
  - Good for N22 evaluation and research project
  - Fixed-Configuration N22 RTL
  - Sign simple evaluation agreement directly on website
- **FreeStart Mass-production Program (FSMP)**
  - For industrial and academy mass production
  - Full-configuration N22
  - License fee: $0; only running royalty is required when mass production
- **Support Package (FSSP)**
  - For all
  - $20K for 1st year, including
    - 1 year e-service
    - FreeStart AE250 RTL
    - Corvette F1 FPGA board



For more info., please visit www.andestech.com

2019 Event Promotion



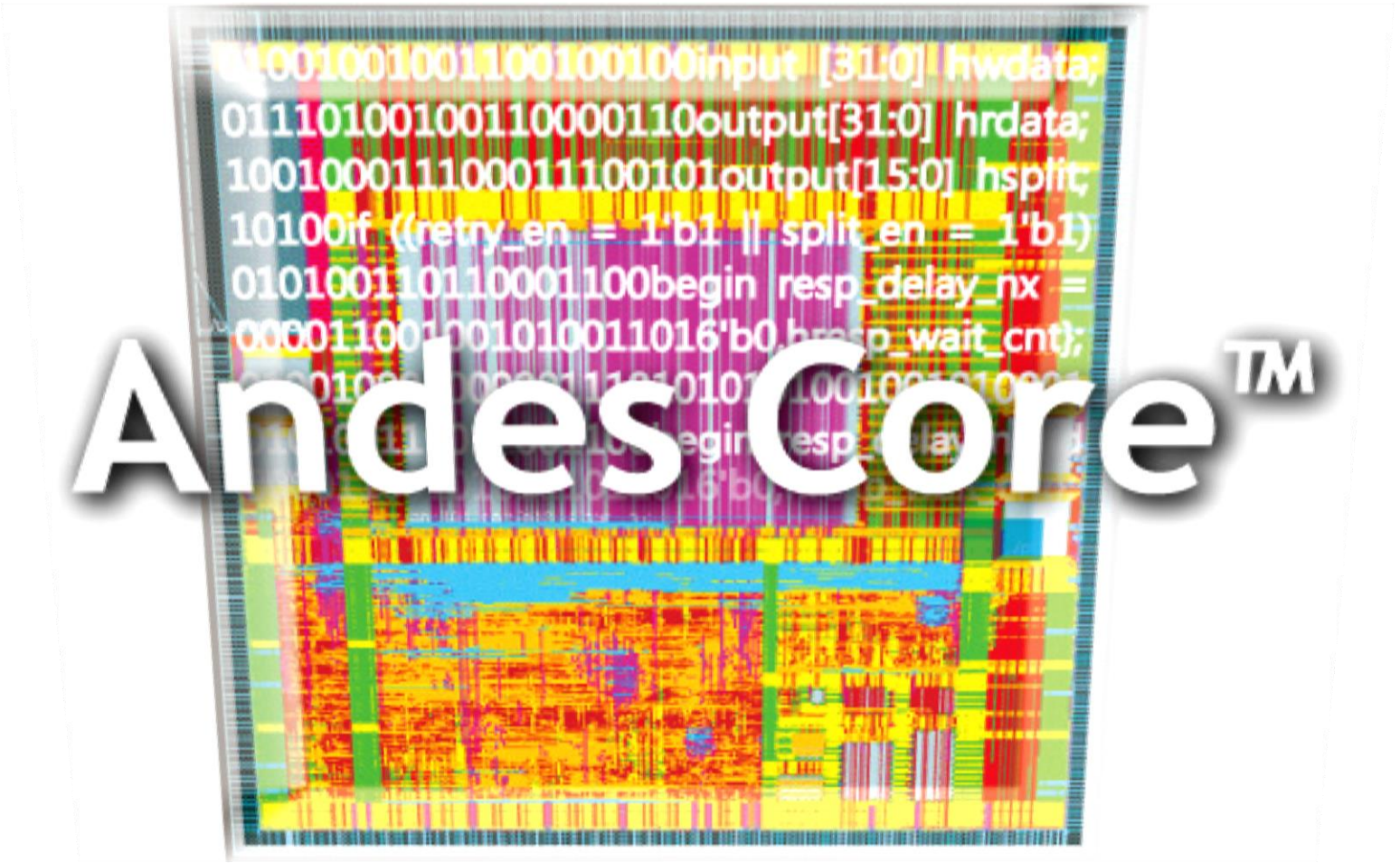
Concluding Remarks

ANDES TECHNOLOGY

Andes: Trusted Computing Expert

- Andes stretched out for more opportunities in Q1~Q3'19 thru the launch of x6 new RISC-V cores, custom design service and FreeStart program.
- Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.
- Andes has successively signed >15 contracts with design service houses to authorize ASIC design to embed RISC-V core (i.e. Andes RISC-V EasyStart Program) for creating a "win-win" situation.
- Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry

Thank You!



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Q&A