晶心科技股份有限公司
2019年第三季法人說明會

Driving Innovations™

股票代號: 6533
2019/12/06

投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

- 公司簡介
- 營運成果
- 產品應用
- 新產品及生態系統
- 近期獲獎
- 總結

公司簡介

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數達190人；80%為工程師。
- **EETimes**評為全球60家最具潛力半導體新創公司。**(2012)**
- **獲得TSMC 2015年新的 IP OIP Award** 。
- **RISC-V基金會創始成員。 (2016)**
- **中國電子報 2018 MCU 設計創新獎**。

晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

晶心利基

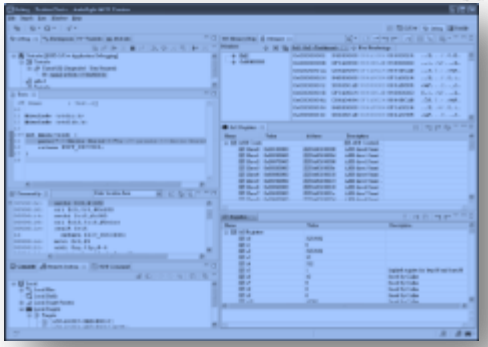
- **智能及環保之電子設備**
- **雲端應用,人工智慧及物聯網**

營運成果

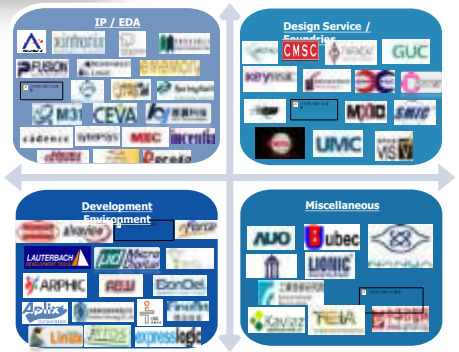
重要里程碑

- 全球授權客戶超過 **160**家
  - 台灣, 大陸, 韓國, 日本, 歐洲, 及美國
  - 授權合約超過**300**份

- **AndeSight™ IDE:**
  - 安裝次數超過 **17,000** 次

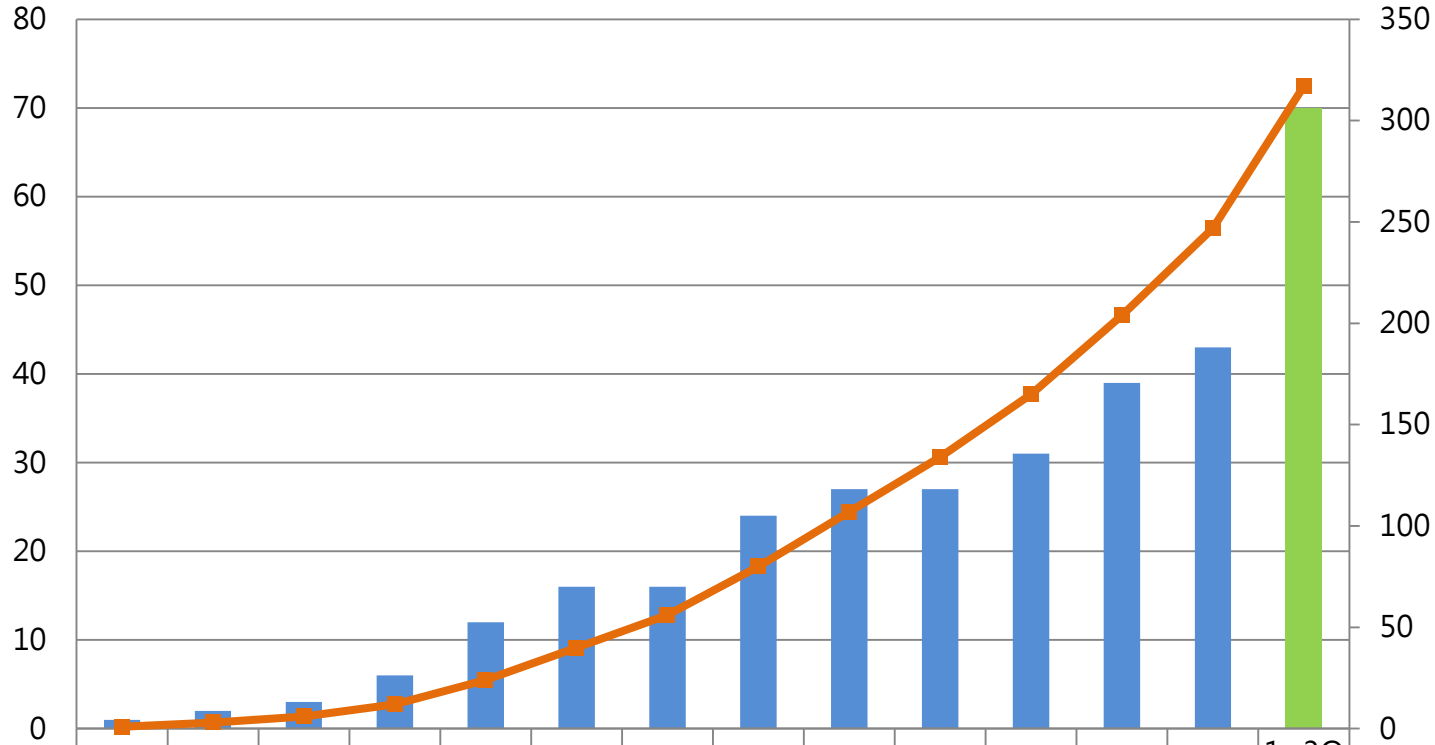


- 生態系統:
  - 合作夥伴超過 **145** 家



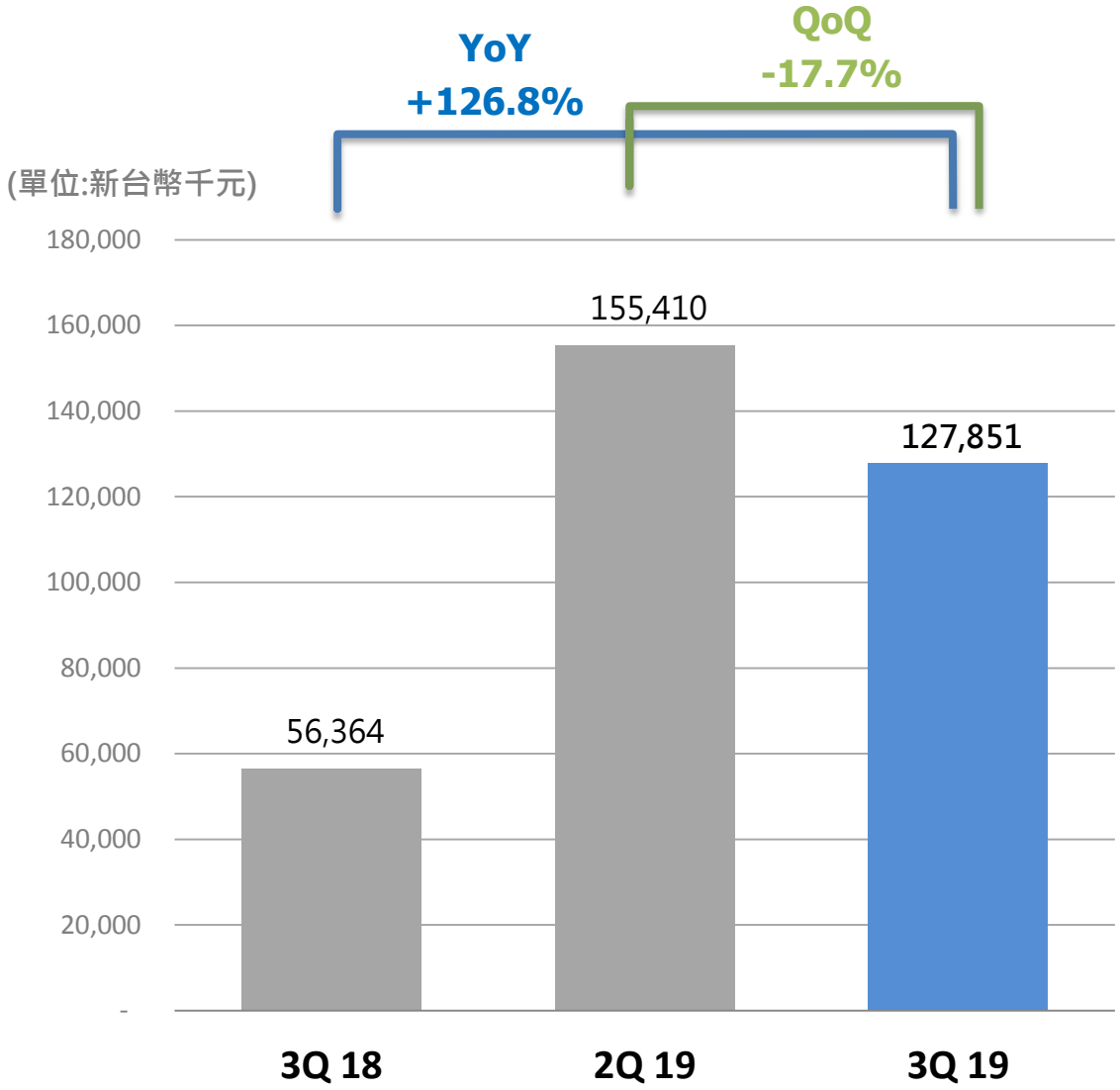
- 嵌入晶心處理器之系統晶片累計出貨量
  - 超過**45**億顆

IP 授權合約數穩健成長

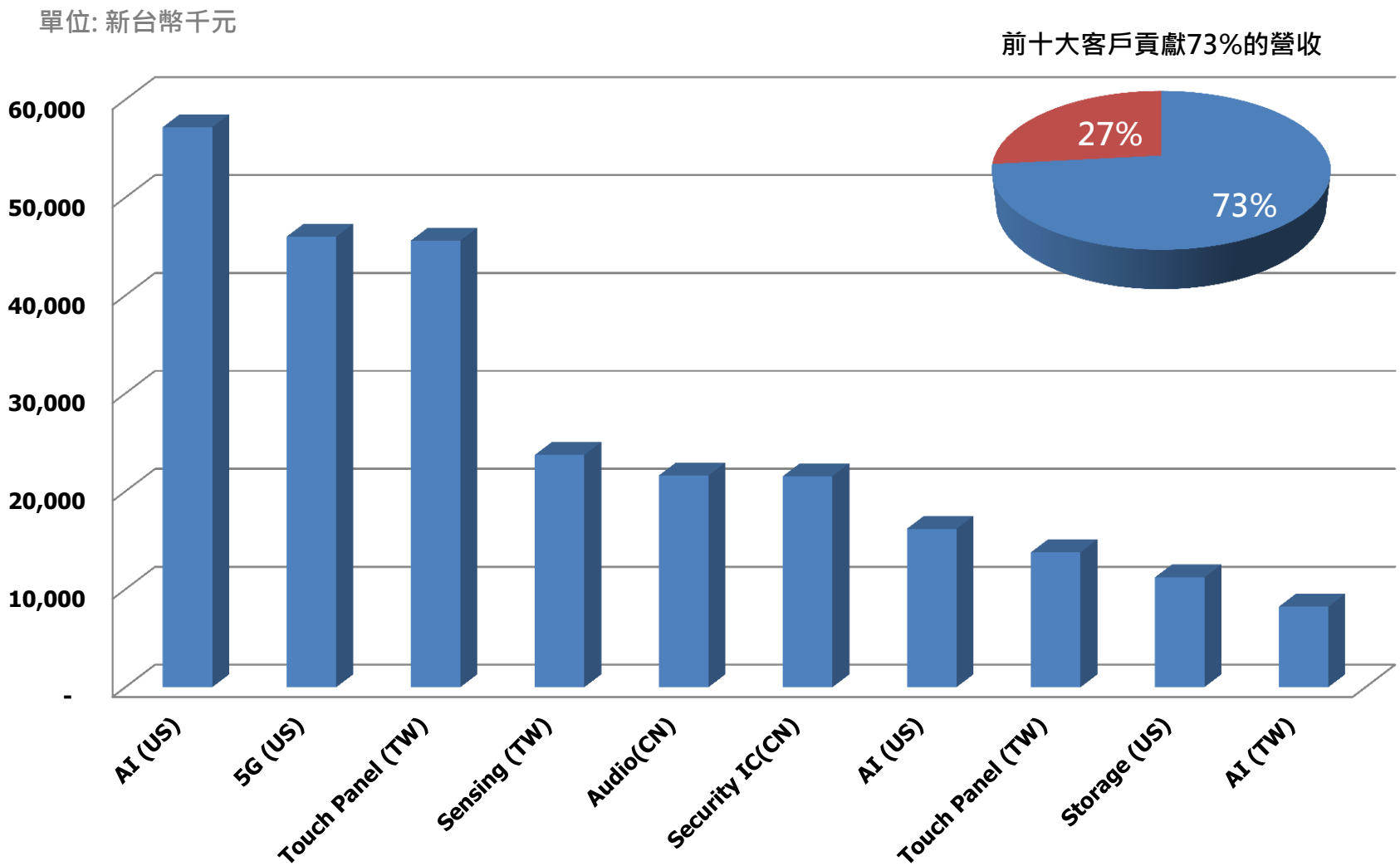


	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	1~3Q 2019
IP授權合約數	1	2	3	6	12	16	16	24	27	27	31	39	43	70
累計IP授權合約數	1	3	6	12	24	40	56	80	107	134	165	204	247	317

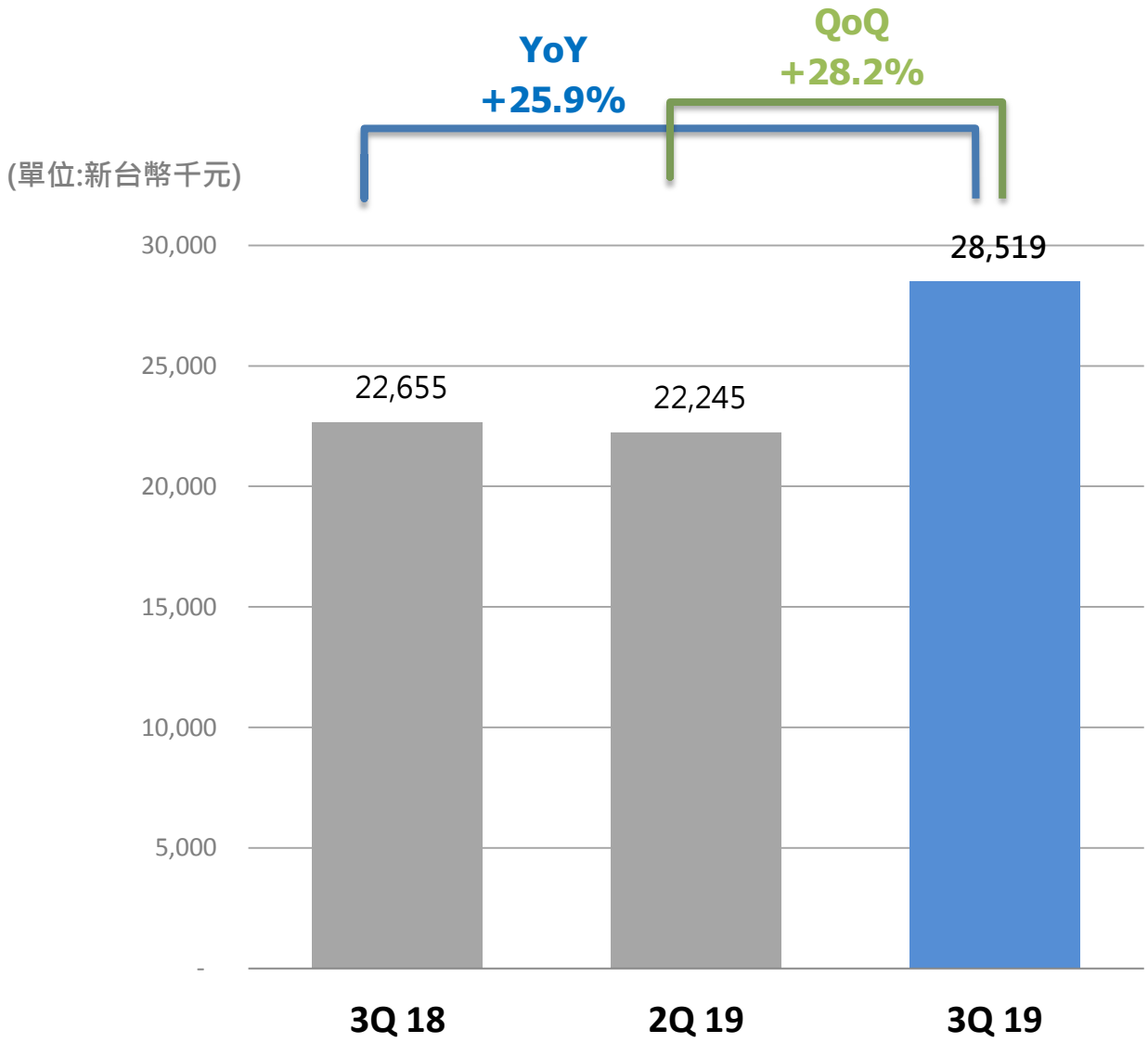
2019年第三季營業收入



2019前三季前十大客戶之應用分析

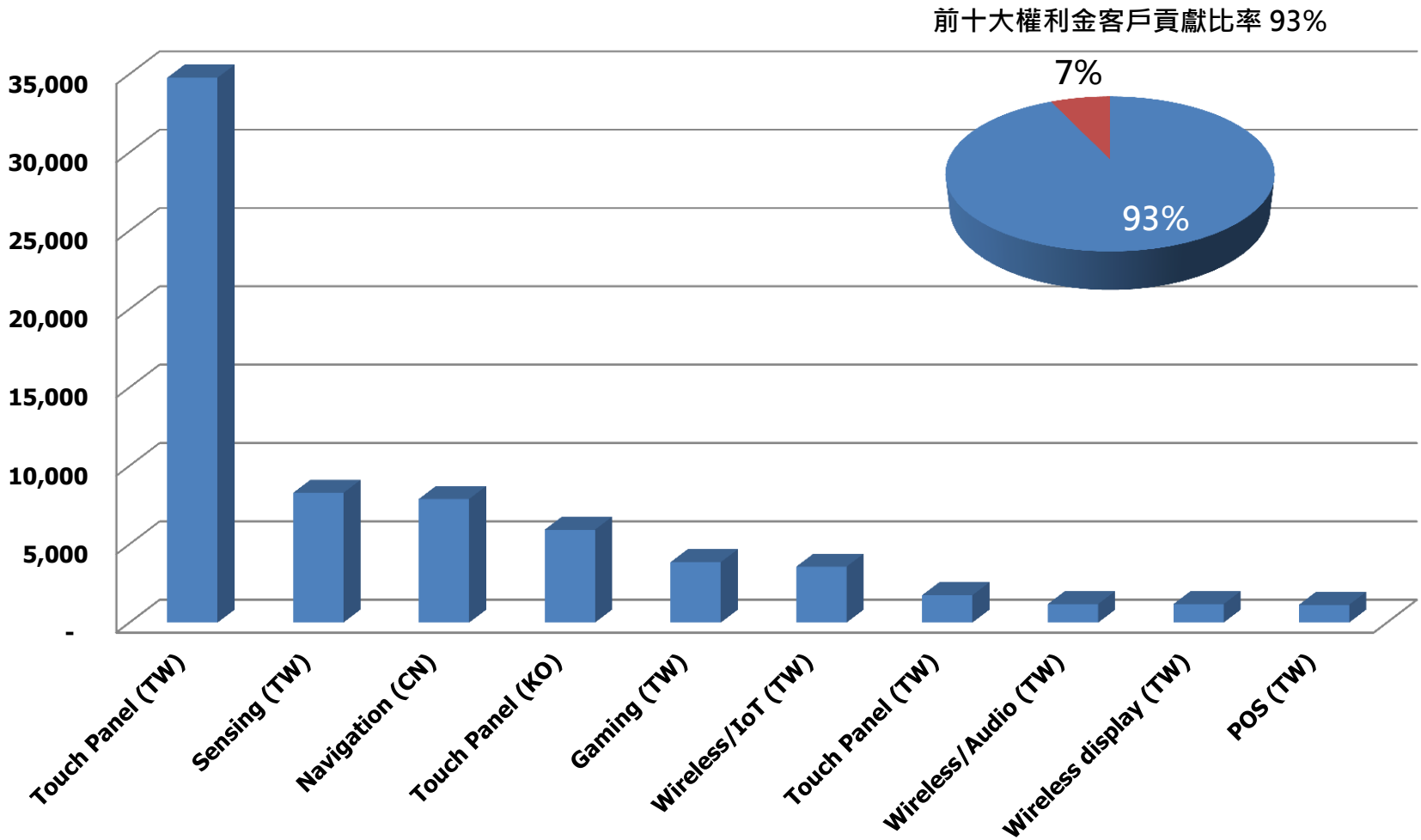


2019年第三季權利金收入



2019年前三季權利金應用分析

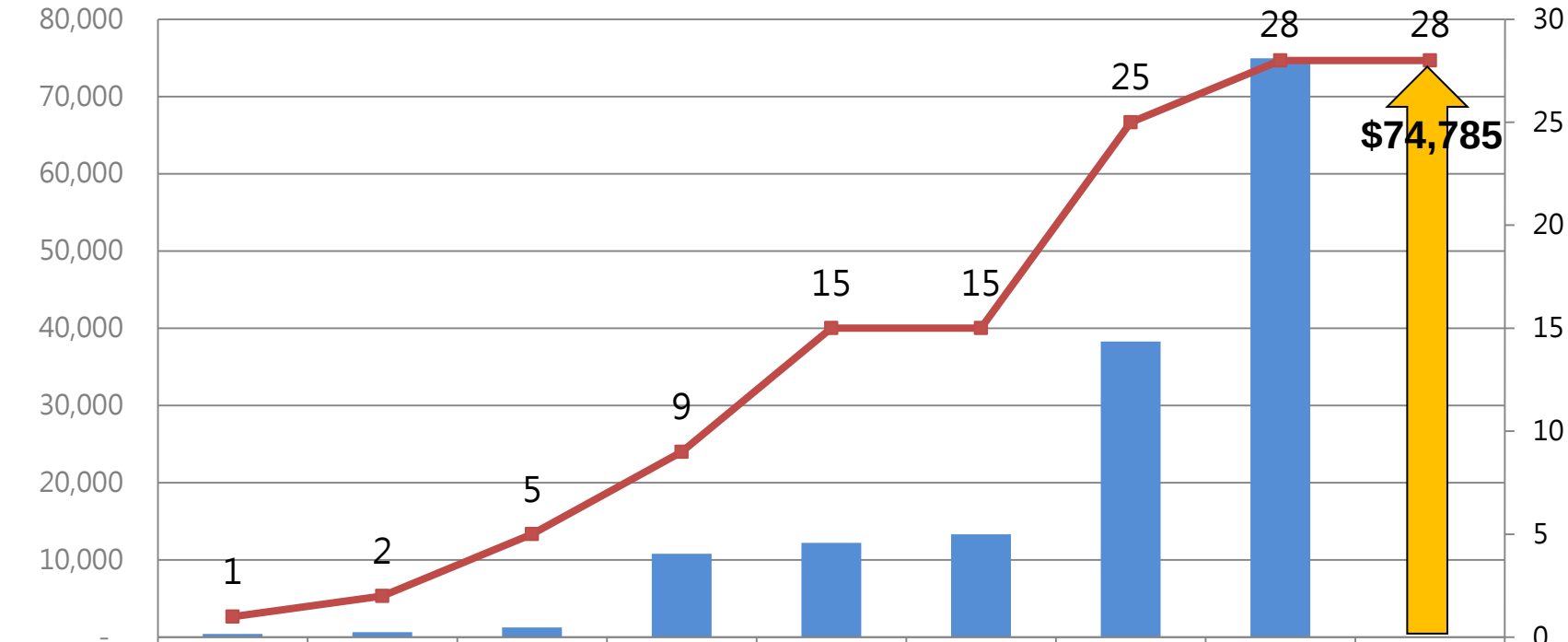
(單位:新台幣千元)



權利金貢獻分析

(單位:新台幣千元)

: 2019 till Q3 royalty collected

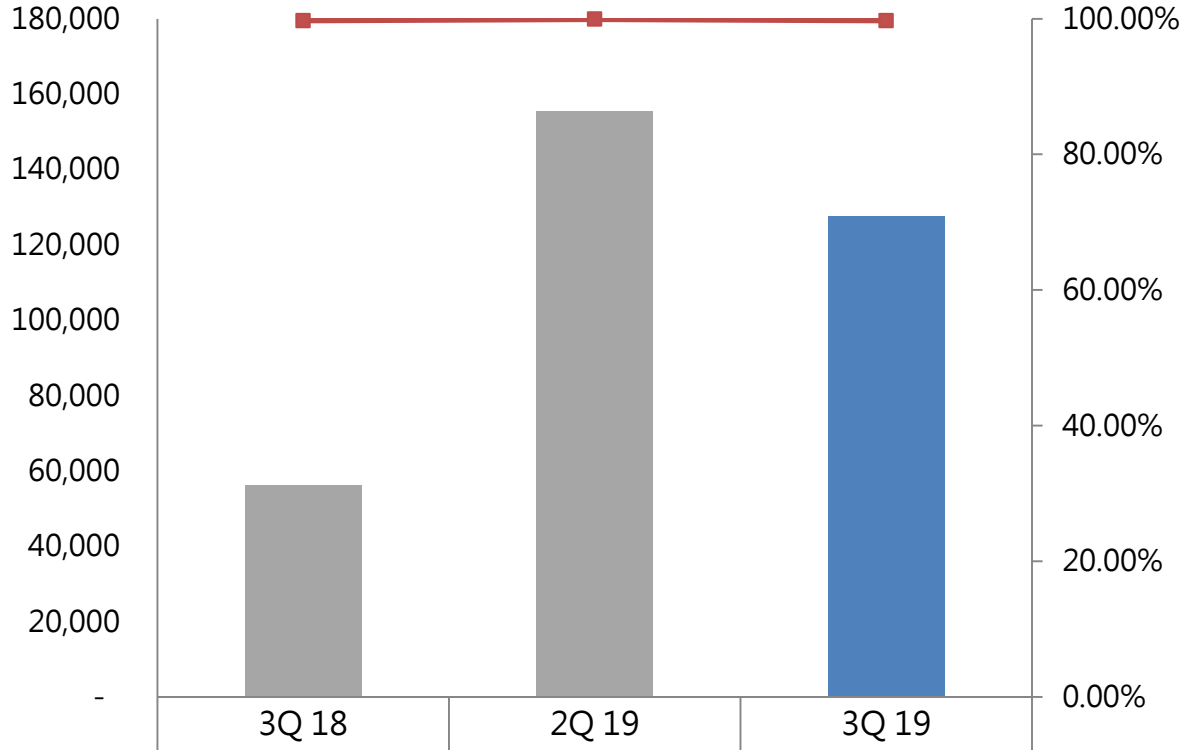


	2011	2012	2013	2014	2015	2016	2017	2018	1-3Q 2019
權利金	445	660	1,285	10,819	12,232	13,320	38,287	74,953	74,785
客戶數	1	2	5	9	15	15	25	28	28

(單位:家數)

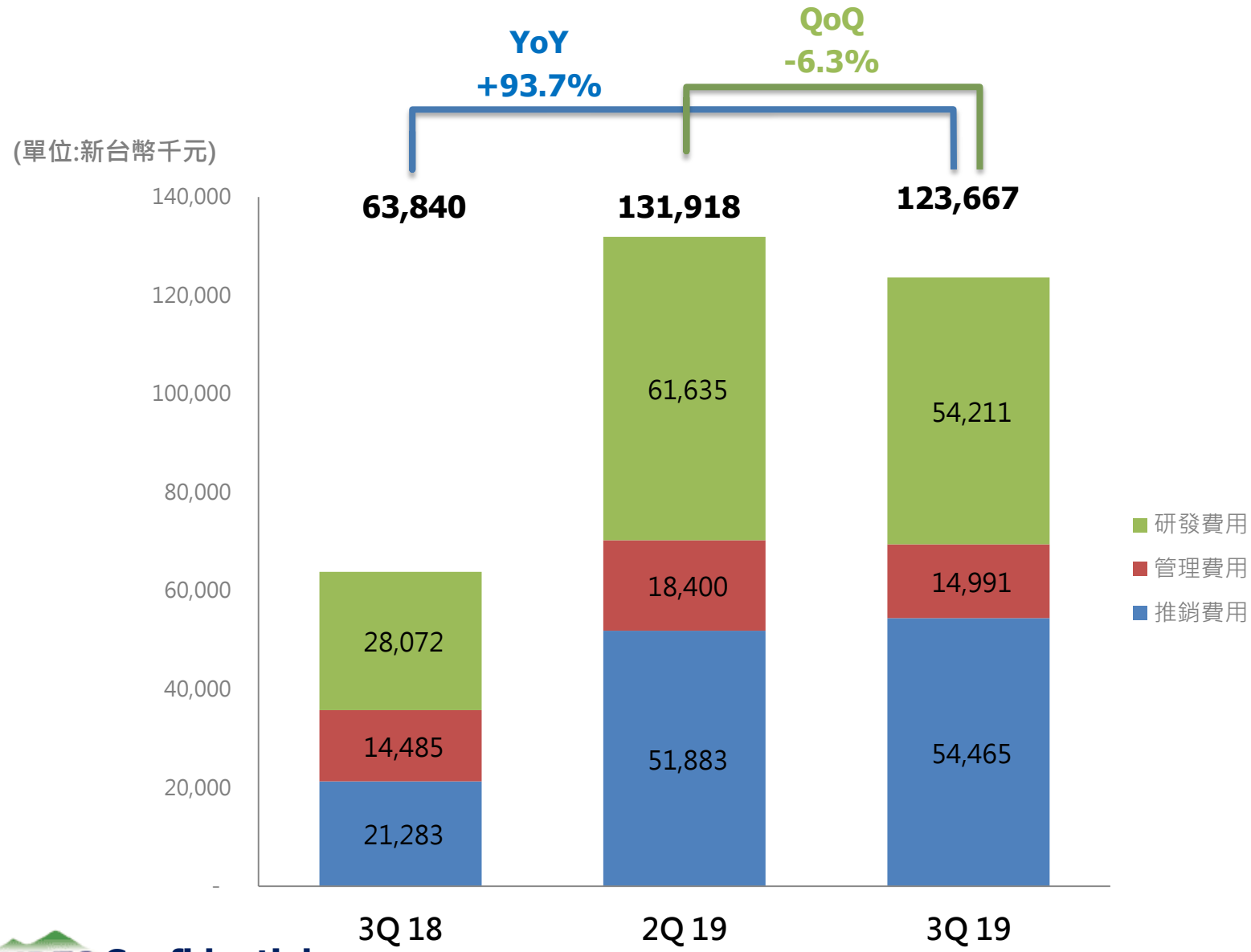
營業毛利與毛利率

(單位:新台幣千元)

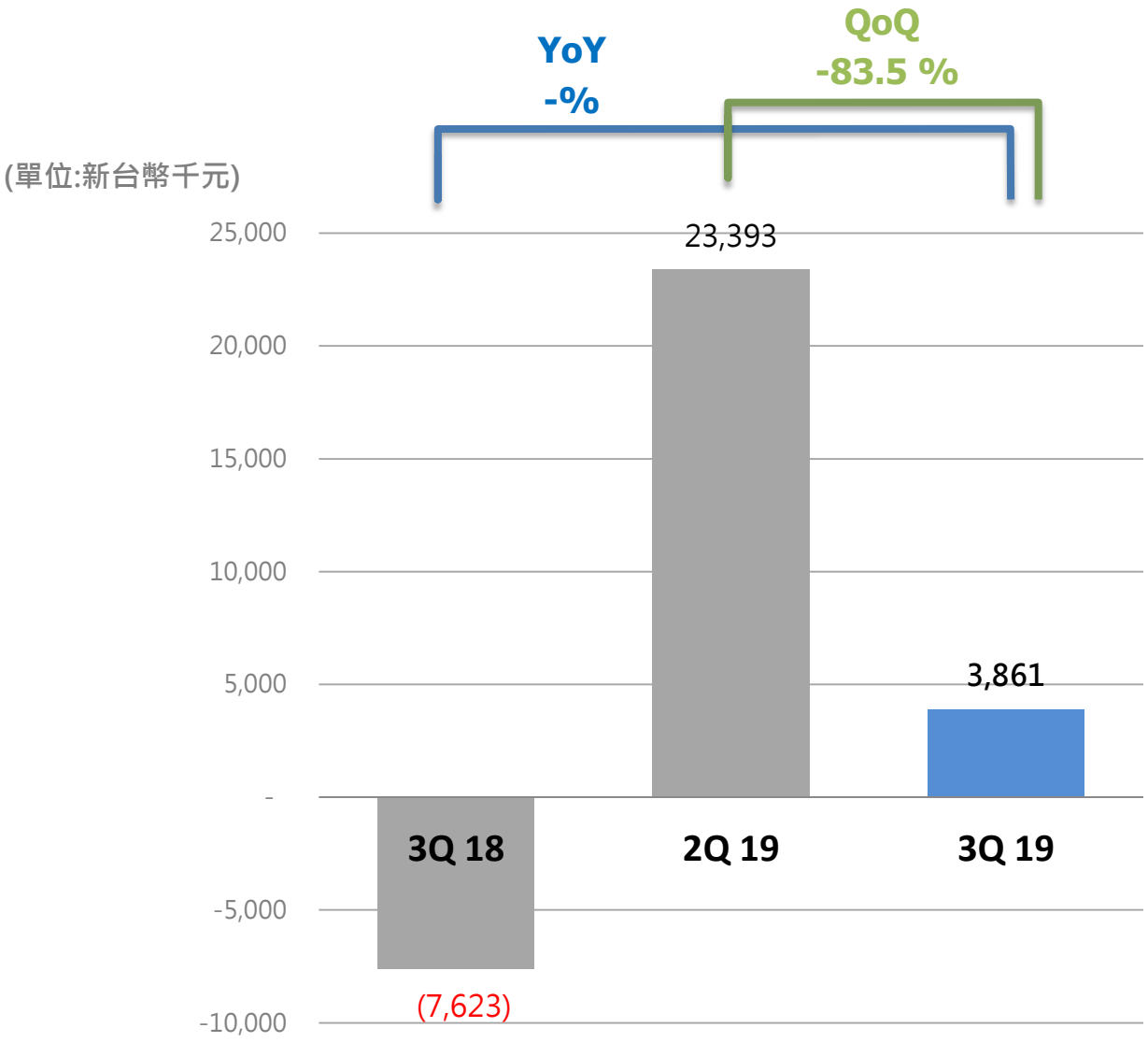


	3Q 18	2Q 19	3Q 19
營業毛利	56,217	155,311	127,528
毛利率	99.74%	99.94%	99.75%

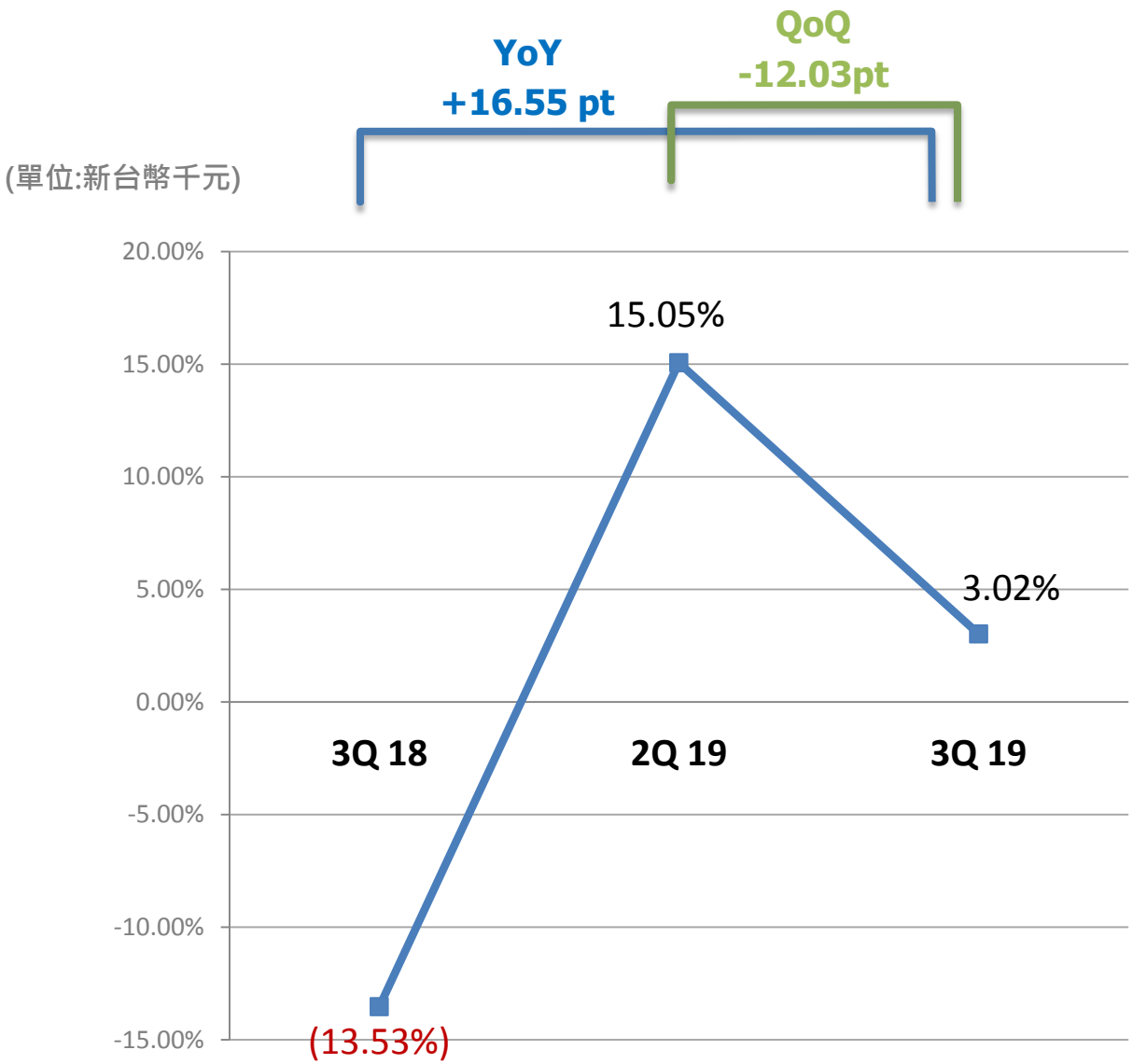
營業費用


YoY
+93.7%
QoQ
-6.3%
(單位:新台幣千元)
140,000
120,000
100,000
80,000
60,000
40,000
20,000
-
63,840
131,918
123,667
28,072
14,485
21,283
61,635
18,400
51,883
54,211
14,991
54,465
3Q 18
2Q 19
3Q 19
研發費用
管理費用
推銷費用

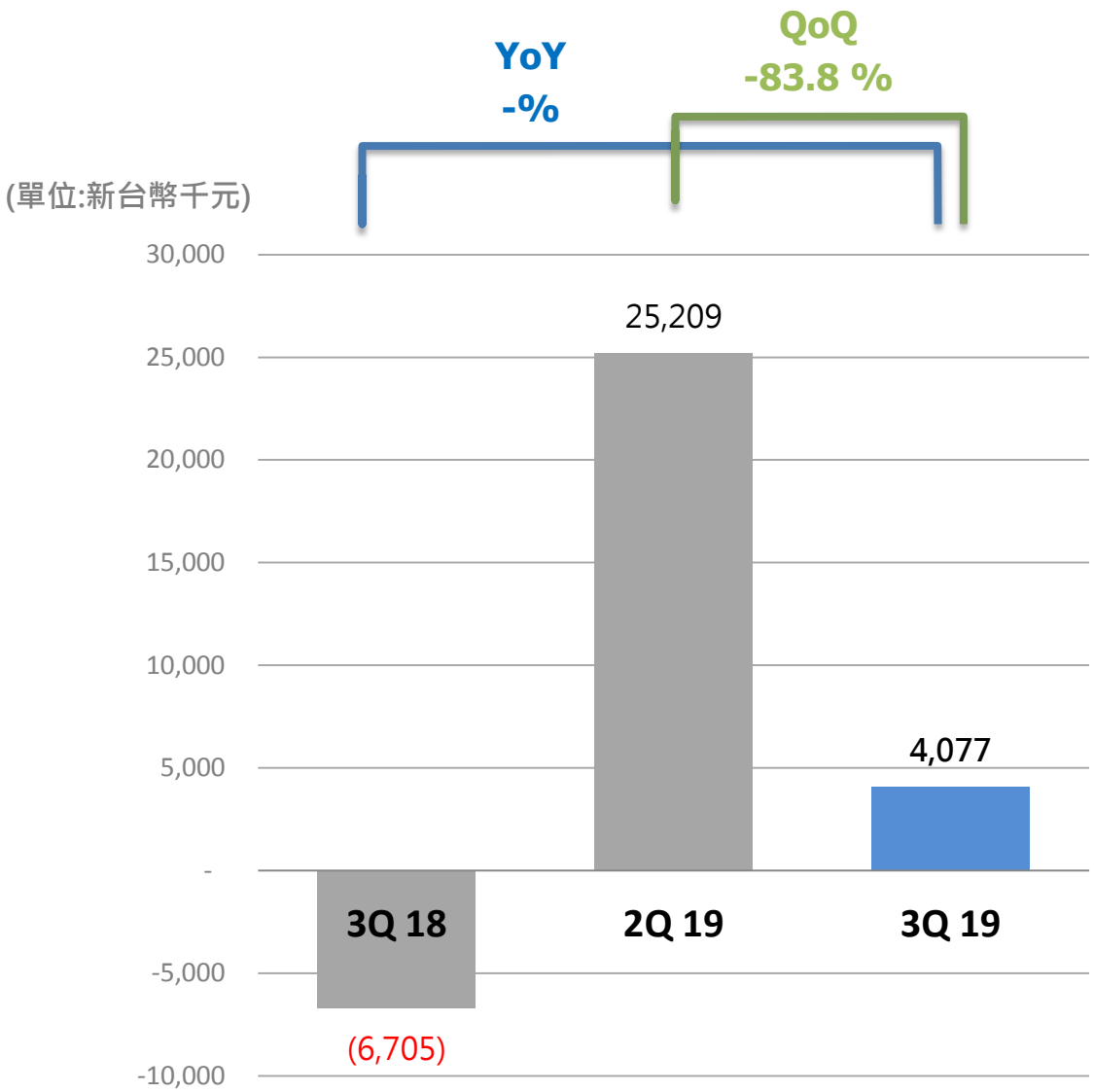
營業利益(損失)


YoY
-%
QoQ
-83.5 %
(單位:新台幣千元)
25,000
20,000
15,000
10,000
5,000
-
-5,000
-10,000
23,393
3,861
(7,623)
3Q 18
2Q 19
3Q 19

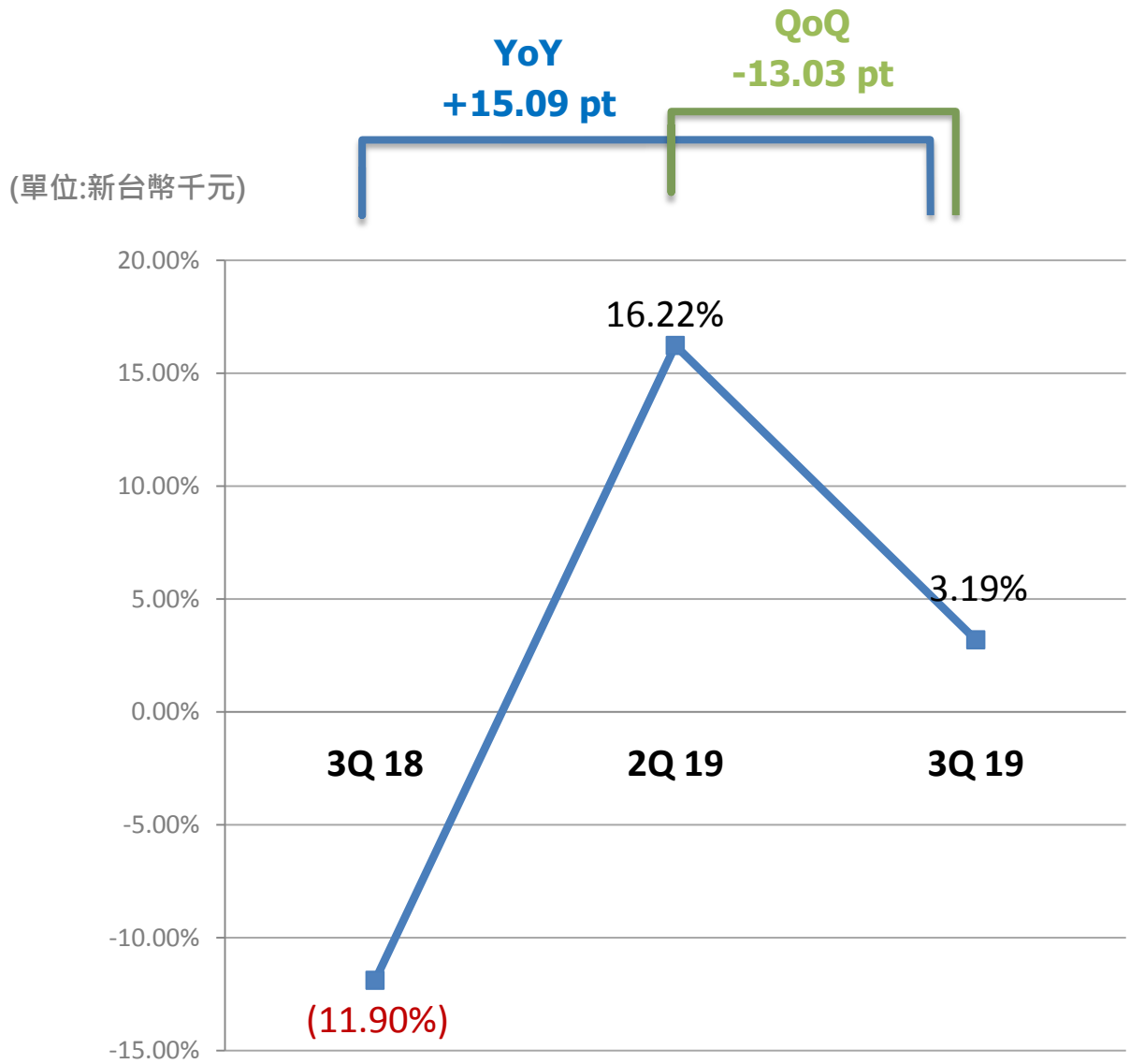
營業利益率


YoY
+16.55 pt
QoQ
-12.03pt
(單位:新台幣千元)
20.00%
15.00%
10.00%
5.00%
0.00%
-5.00%
-10.00%
-15.00%
15.05%
3.02%
(13.53%)
3Q 18
2Q 19
3Q 19

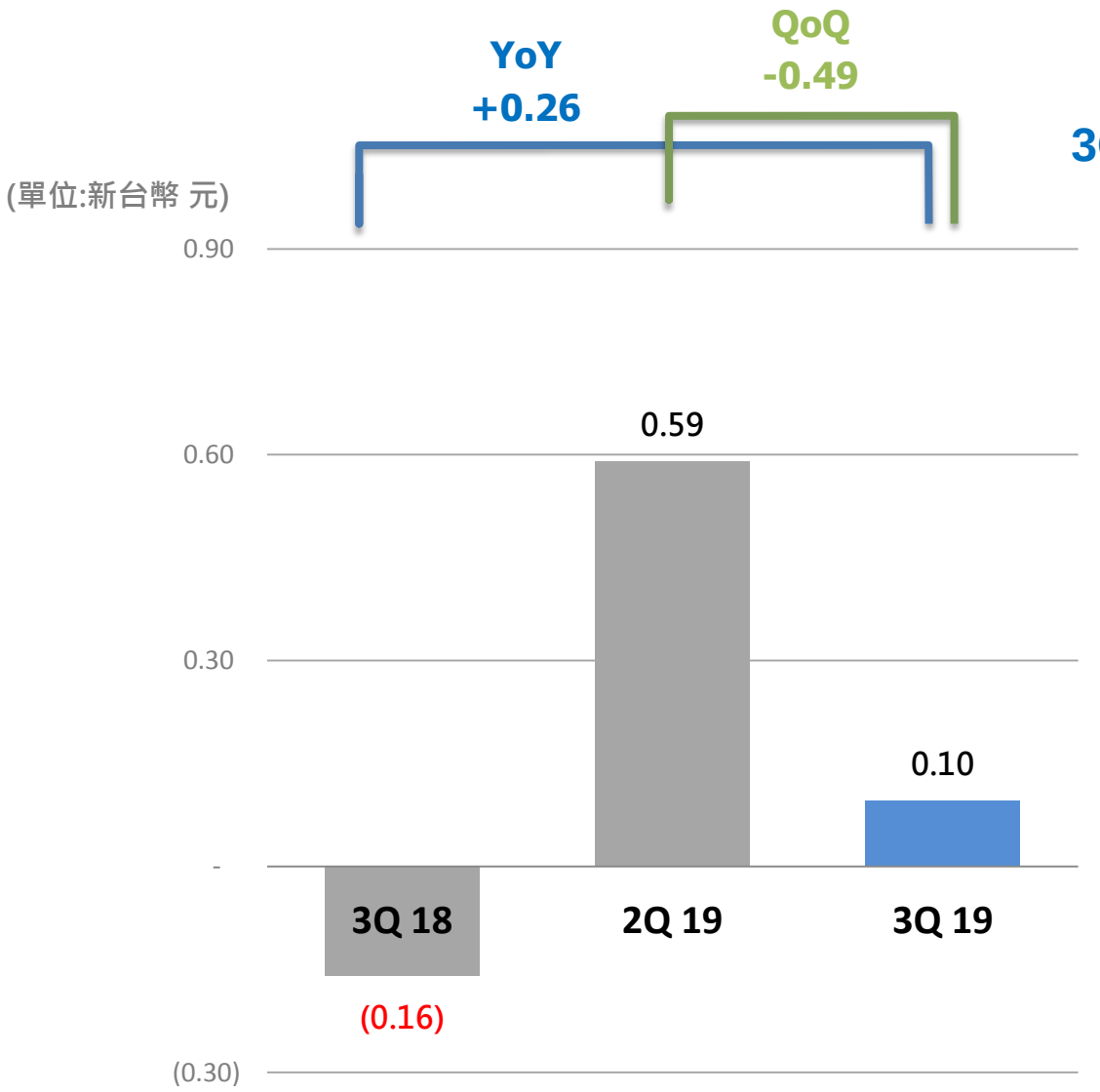
合併淨利(損)


YoY
-%
QoQ
-83.8 %
(單位:新台幣千元)
30,000
25,000
20,000
15,000
10,000
5,000
-
-5,000
-10,000
25,209
4,077
(6,705)
3Q 18
2Q 19
3Q 19

合併淨利率

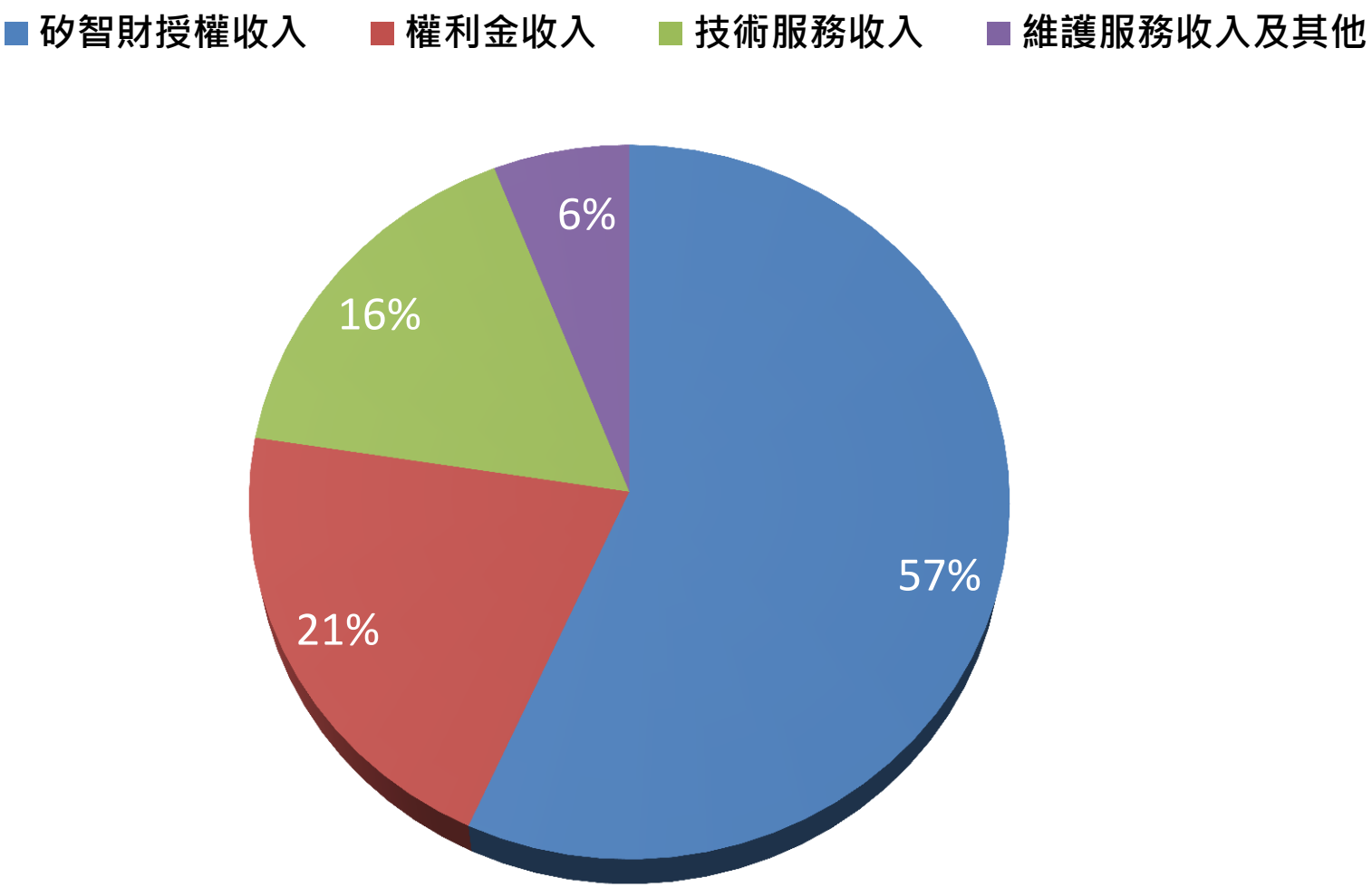

YoY
+15.09 pt
QoQ
-13.03 pt
(單位:新台幣千元)
20.00%
15.00%
10.00%
5.00%
0.00%
-5.00%
-10.00%
-15.00%
16.22%
3.19%
(11.90%)
3Q 18
2Q 19
3Q 19

每股盈餘

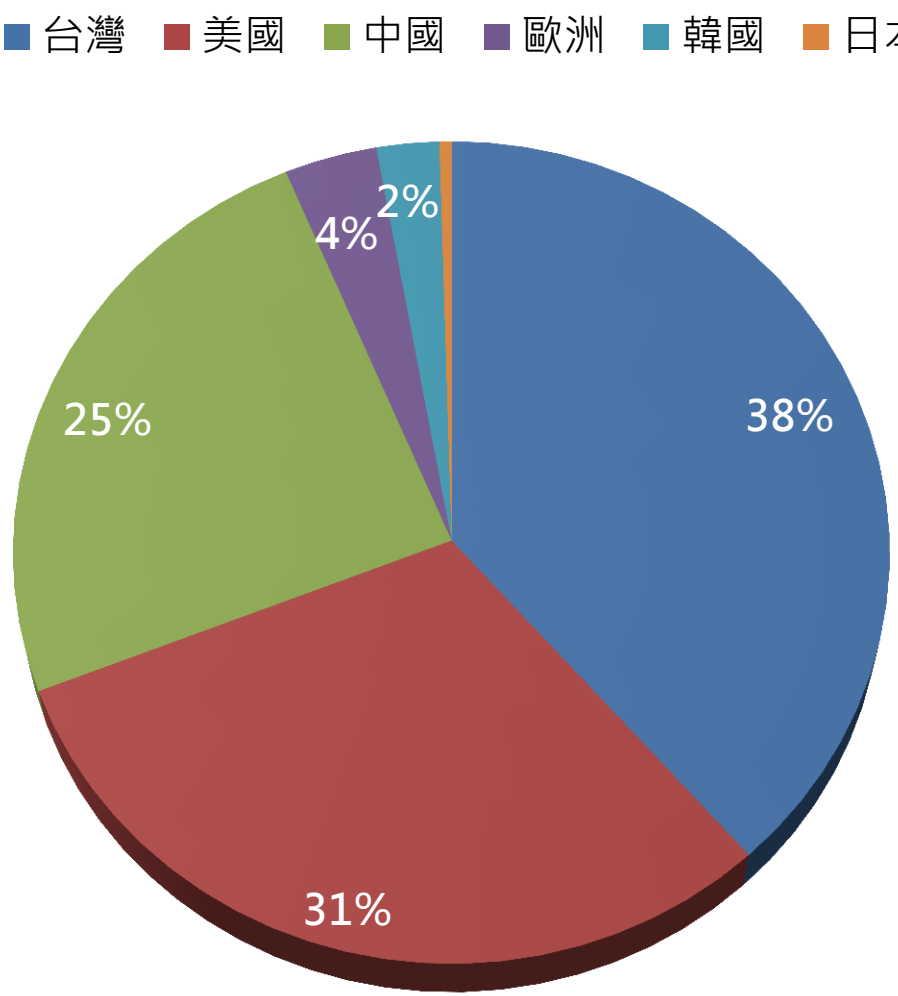


3Q19 EPS: 0.13

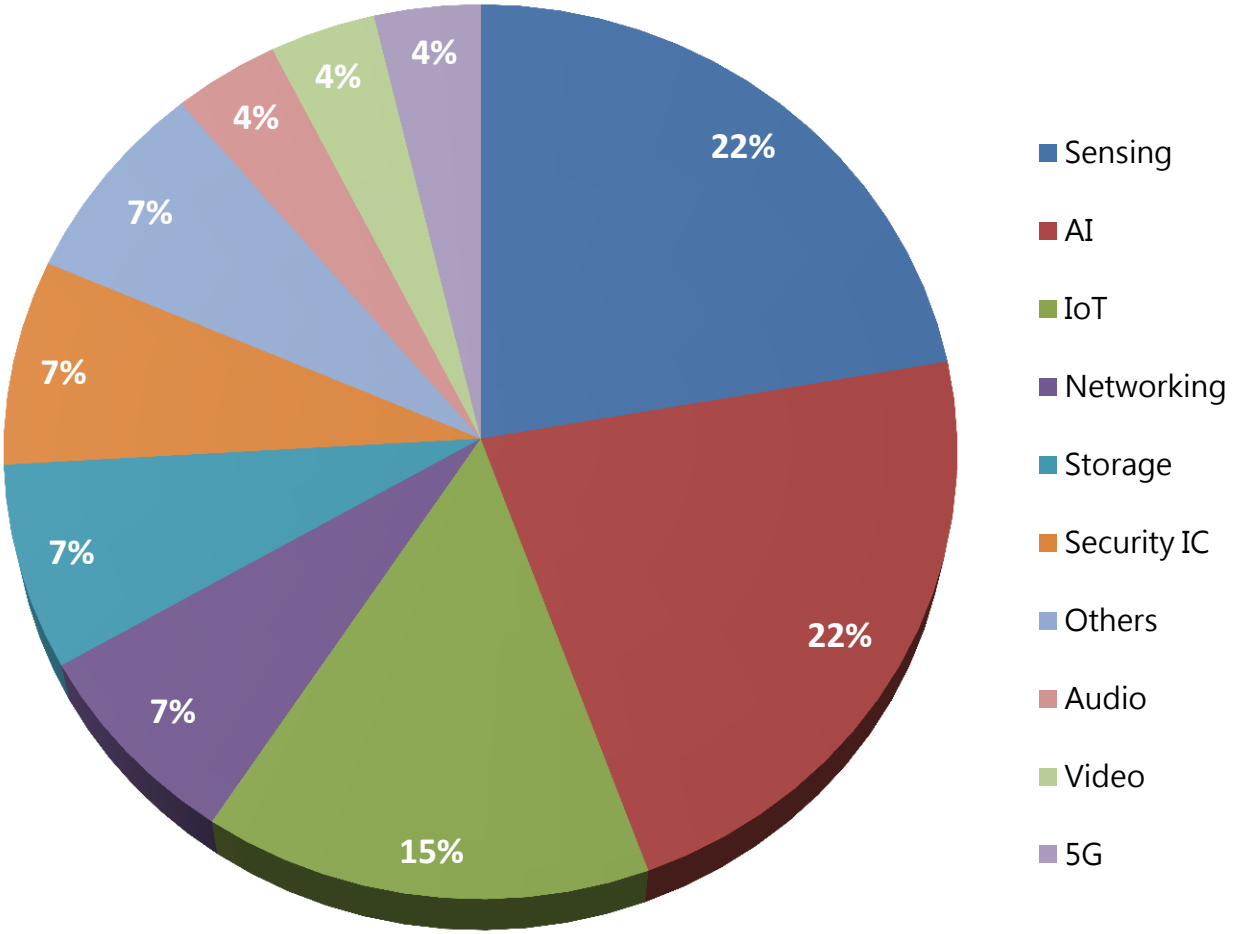
2019年前三季銷售分析-收入模式



2019年前三季銷售分析-地區別

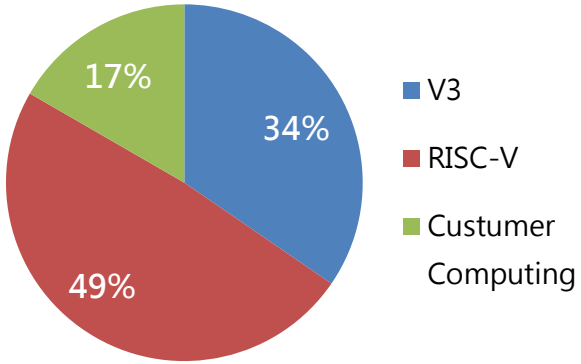


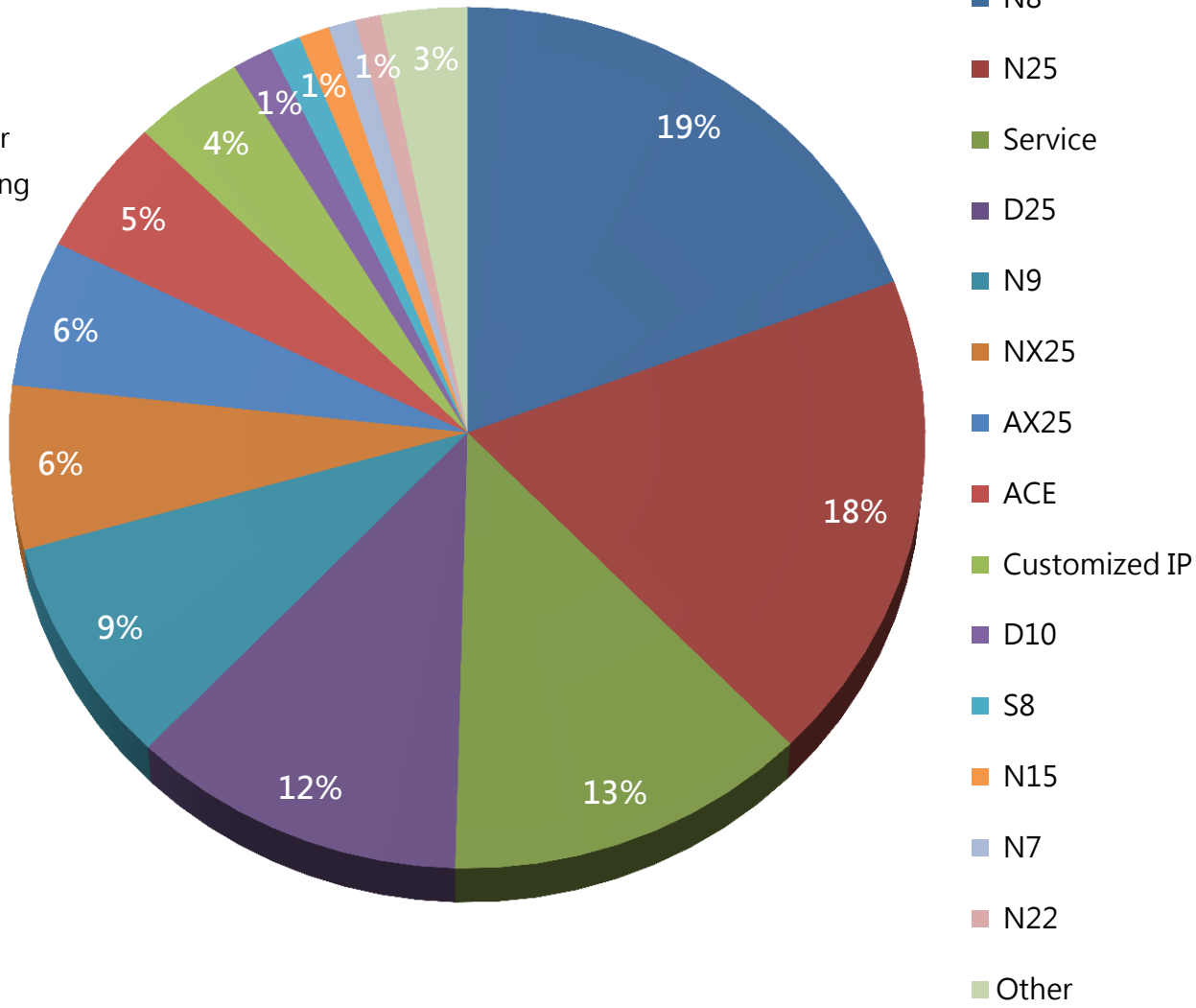
2019年前三季銷售分析-客戶應用



*Based on agreement number

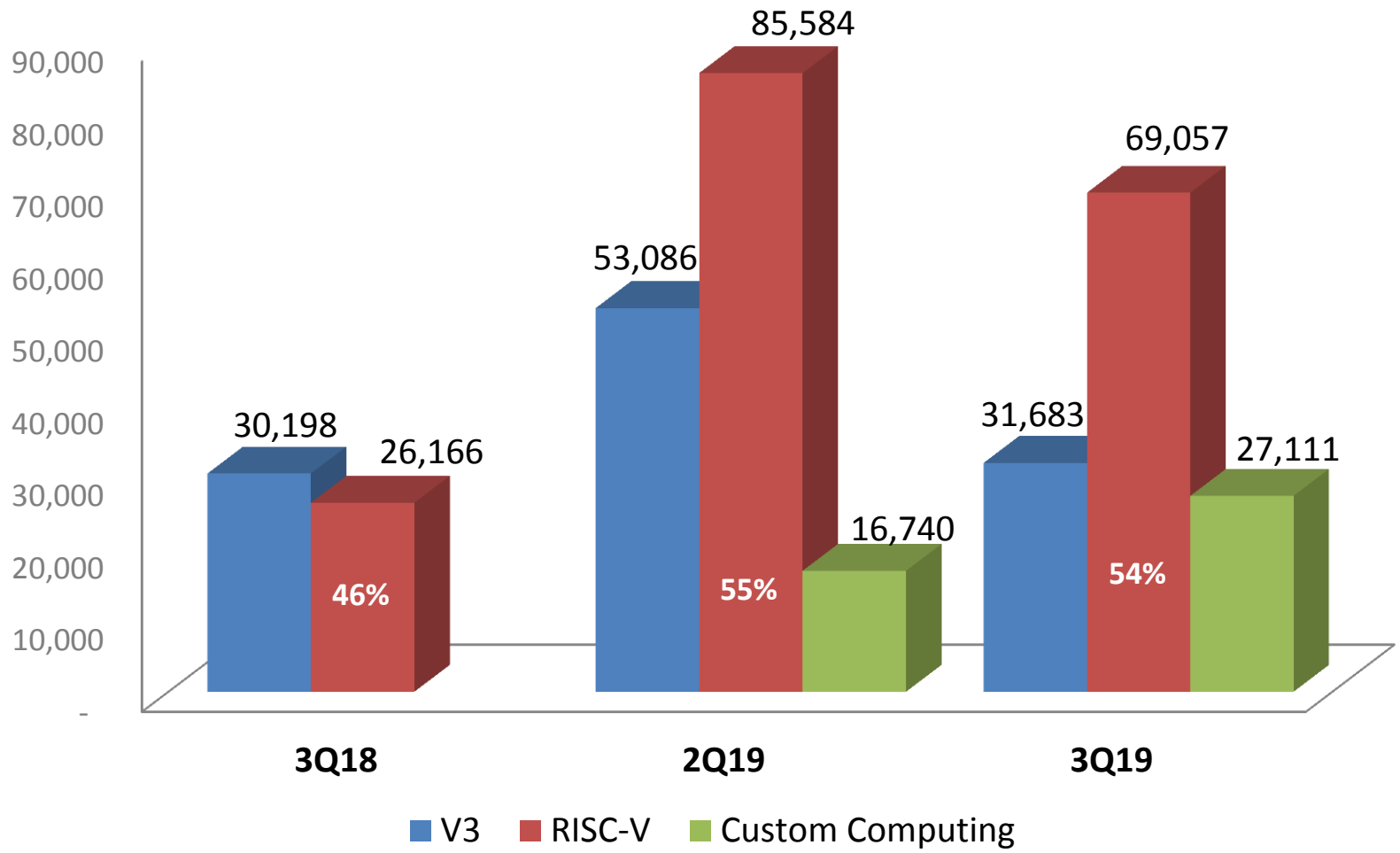
2019年前三季銷售分析-產品別



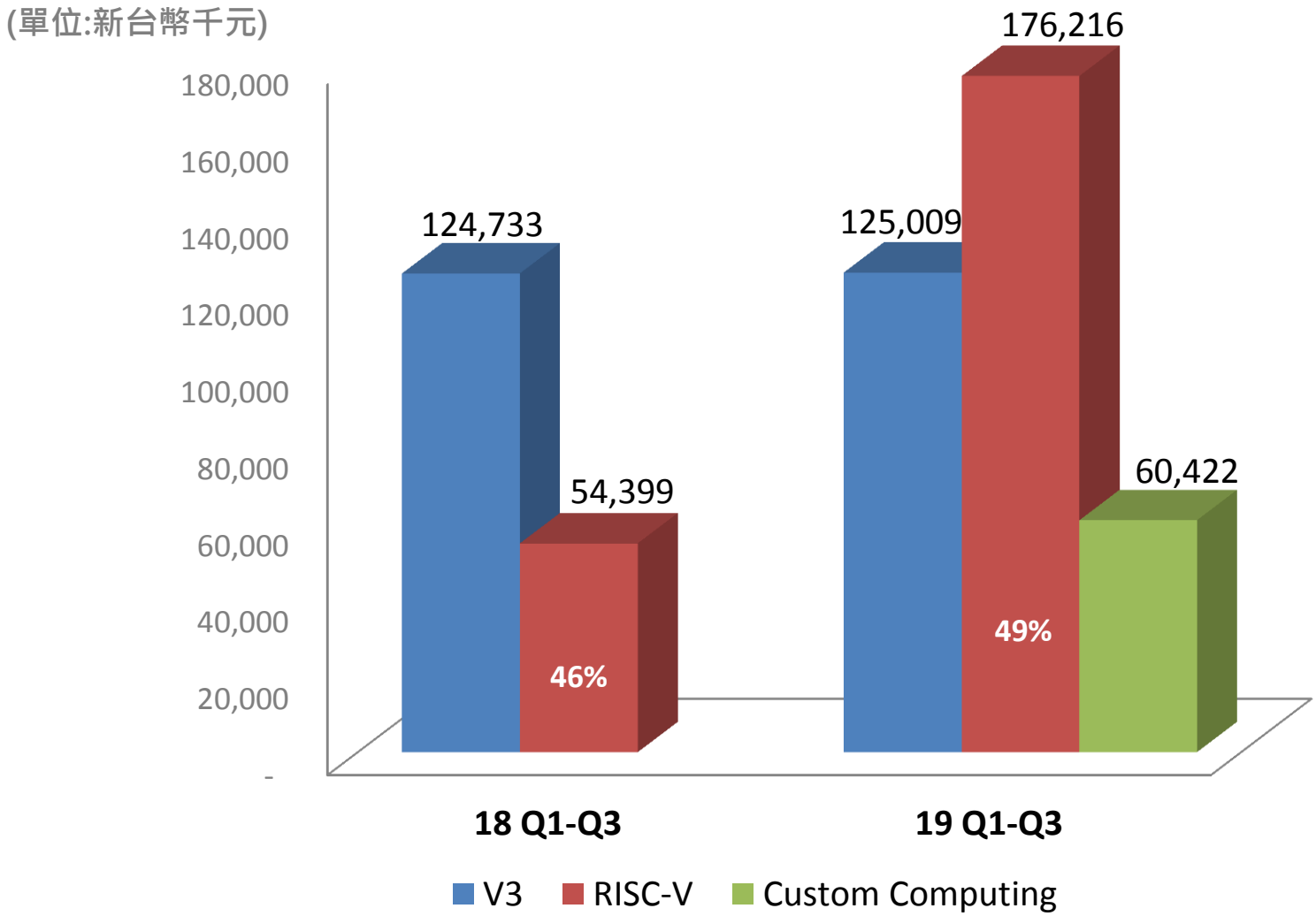


2019年第三季銷售分析 - RISC-V

(單位:新台幣千元)



2019年前三季銷售分析 - RISC-V

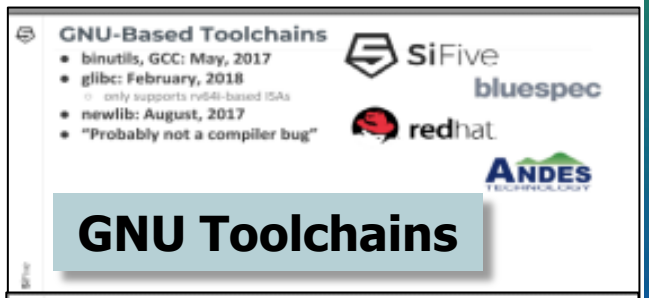


產品應用

晶心概況

- A 14-year-old public CPU IP company

- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involvement in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group



豐富多樣的客戶應用

Consumer

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

Storage & Sensor

- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition

Communication & IoT

- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
- ESL
- Smart Meter
- Smart Lighting

Industrial & Video

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

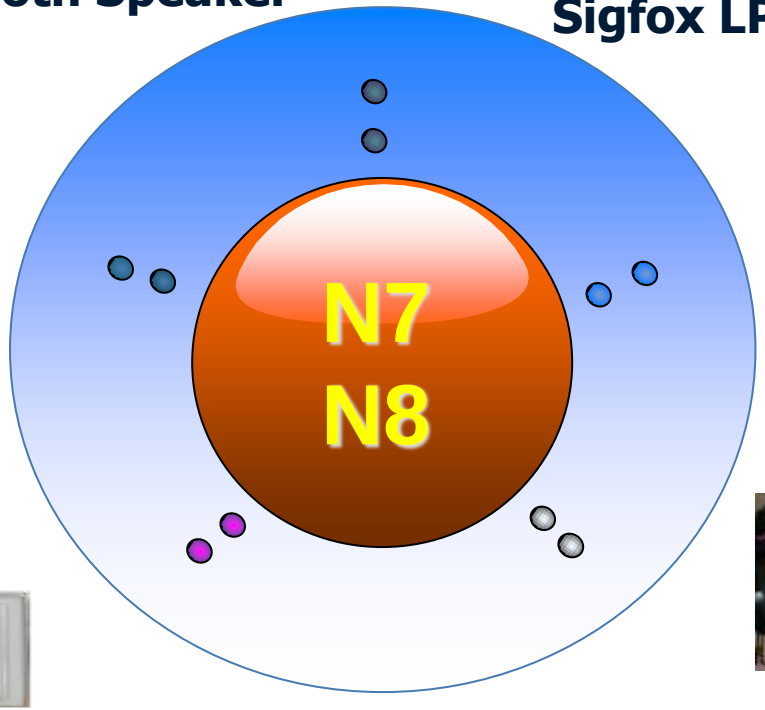
and more…..

物聯網應用 - 1

Bluetooth Speaker

Sigfox LPWAN

Healthcare device



Wearable device

Electronic price tags

Sensor Hub

物聯網應用 - 2

Wearable devices

Drone

Portable Karaoke

N9
D10

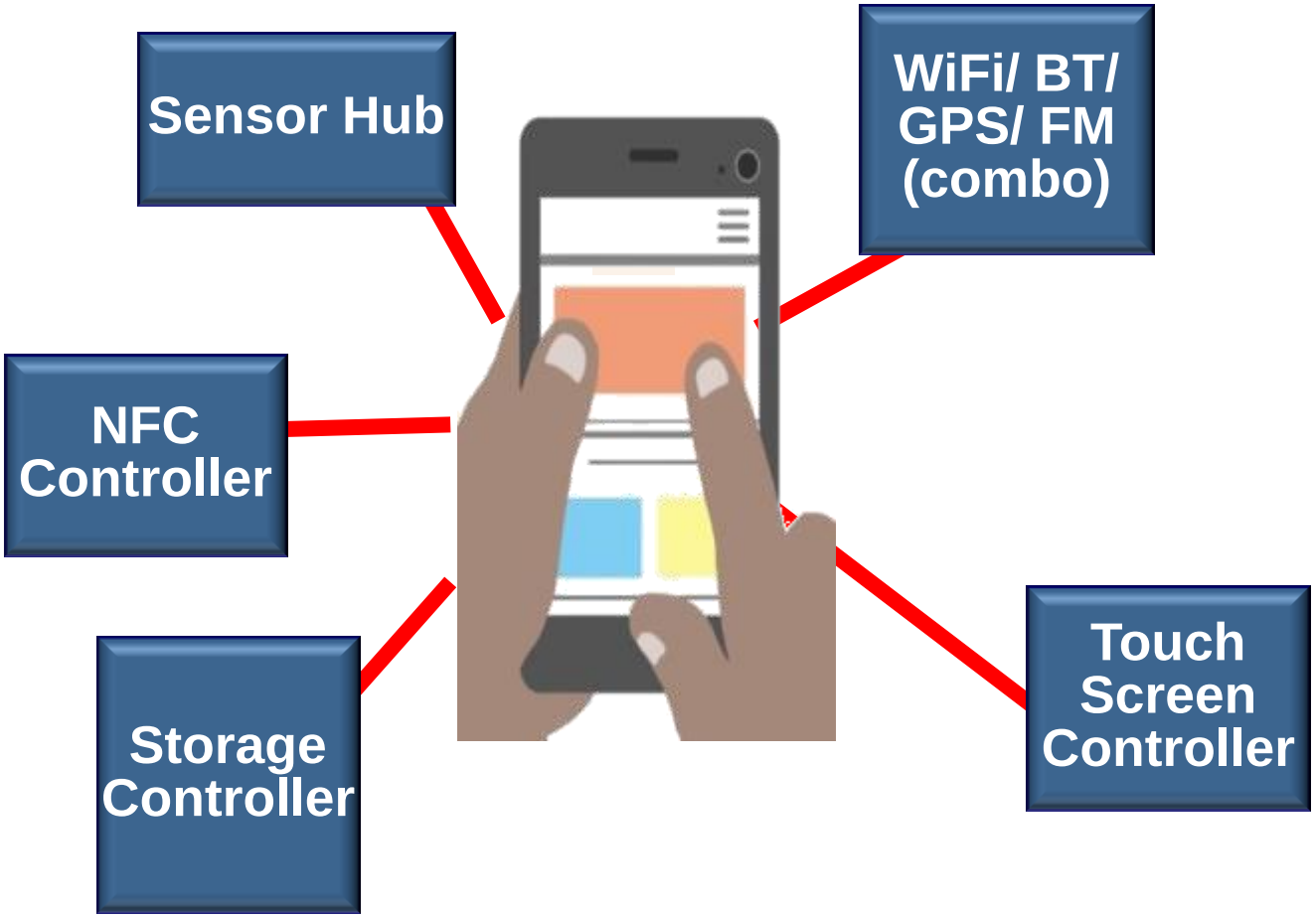
WiFi/GPS/FM/Bluetooth combo

GPS/Beido in shared bikes

Contactless payment (NFC)

晶心嵌入智能手機

1 in 5 Smart Phones are with Andes Embedded



晶心嵌入消費性裝置、車用電子及資料處理中心

Switch:
MXIC Flash Ctlr

Echo Dot2:
Mediatek WiFi IoT

Bike Sharing:
GPS Ctrl

X-Trail:
ADAS Ctlr

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

新產品及生態系統

完整產品線

- New A-series Cores released in Andes Embedded Forum 2018

ANDES

RISC-V

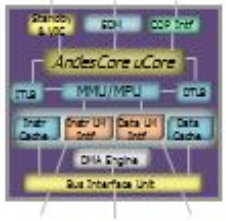
晶心 RISC-V 產品概述

Best extensions to RISC-V

AndeStar™ Architecture V5

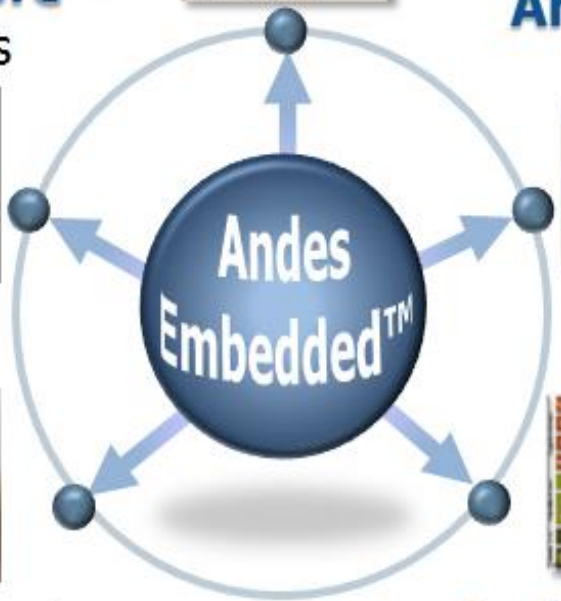
Highly optimized design with leading PPA

AndesCore™ Processors



AndeSight™ Tools

Professional IDE with high code quality



Handy peripheral IPs to speed up SoC construction

Extensive SW stacks from bare metal, RTOS to Linux

AndeShape™ Platforms

AndeSoft™ Stacks

V5 AndesCore™ 處理器核心

N22

N25F/NX25F

A25/AX25

A25MP/AX25MP

最新產品路線圖

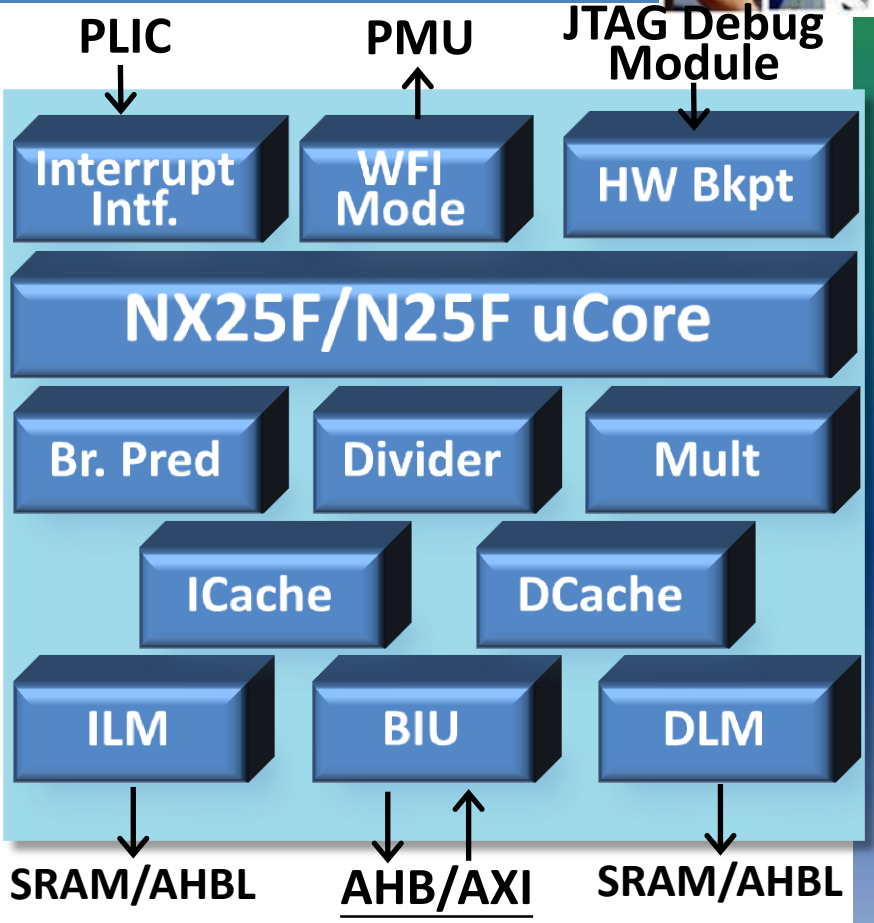
Next-Gen	Cores with higher total performance and RISC-V ISA extensions		Higher performance
Cache-Coherent Multicores	**A25MP** 1/2/4 A25, L2$, L1/IO coherence	**AX25MP** 1/2/4 AX25, L2$, L1/IO coherence	5-stage >1.2GHz 3.58 CoreMark 2.09 DMIPS
Linux with FPU/DSP	**A25** N25F, MMU, DSP	**AX25** NX25F, MMU, DSP	
Fast/Compact with FPU/DSP	**N25F** V5/32b, FPU, PMP **D25F** N25F, DSP	**NX25F** V5/64b, FPU, PMP	
Slim and Efficient	**N22** V5[e], 32/16 GPR		2-stage 700MHz 3.95 CoreMark 1.80 DMIPS
	32bit	64bit	

將晶心的優勢帶進 RISC-V 處理器

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure

V5 AndesCores: 25-系列

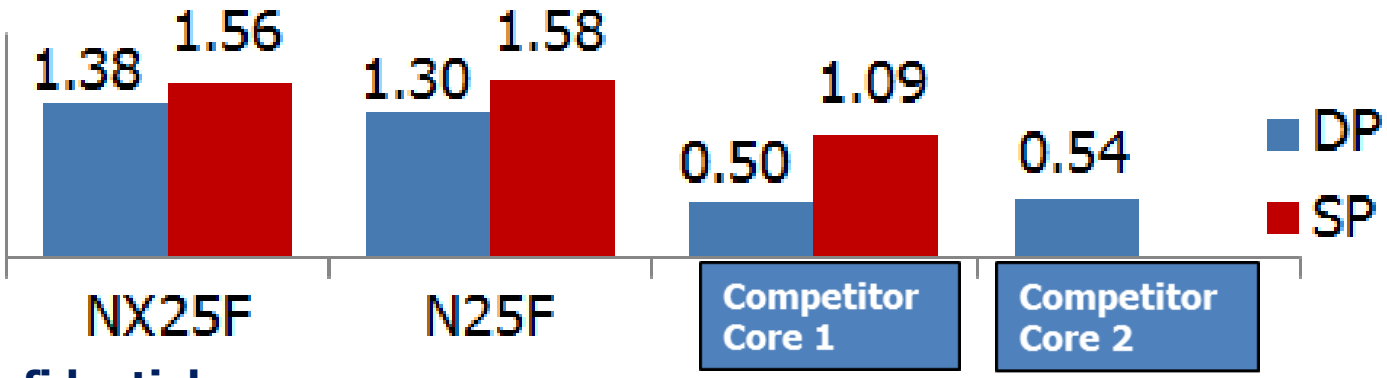
- **N25F: 32-bit, NX25F: 64-bit**
  - From scratch for the best PPA
  - Very configurable
- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses



- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case, w/o caches)
  - Large config: 136K gates, 1.2GHz (worst case, w/ caches)
  - **Best-in-class Coremark: 3.58/MHz**

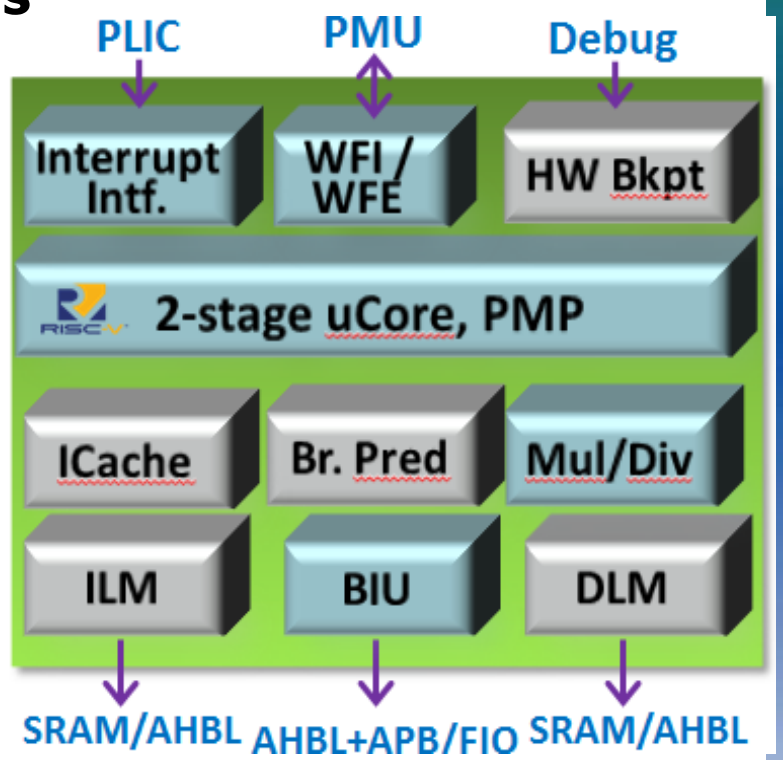
V5 AndesCores: 25-系列

- **Fast-n-small for control tasks in AR/VR, networking, storage, AI**
- **N25F/NX25F: +FPU**
  - +, –, x, x+, x–: pipelined 4 cycles
  - ÷, √ : run in the background
    - 15 for SP, 29 for DP
- **A25/AX25: +FP +Linux**
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- **Whetstone/MHz**:



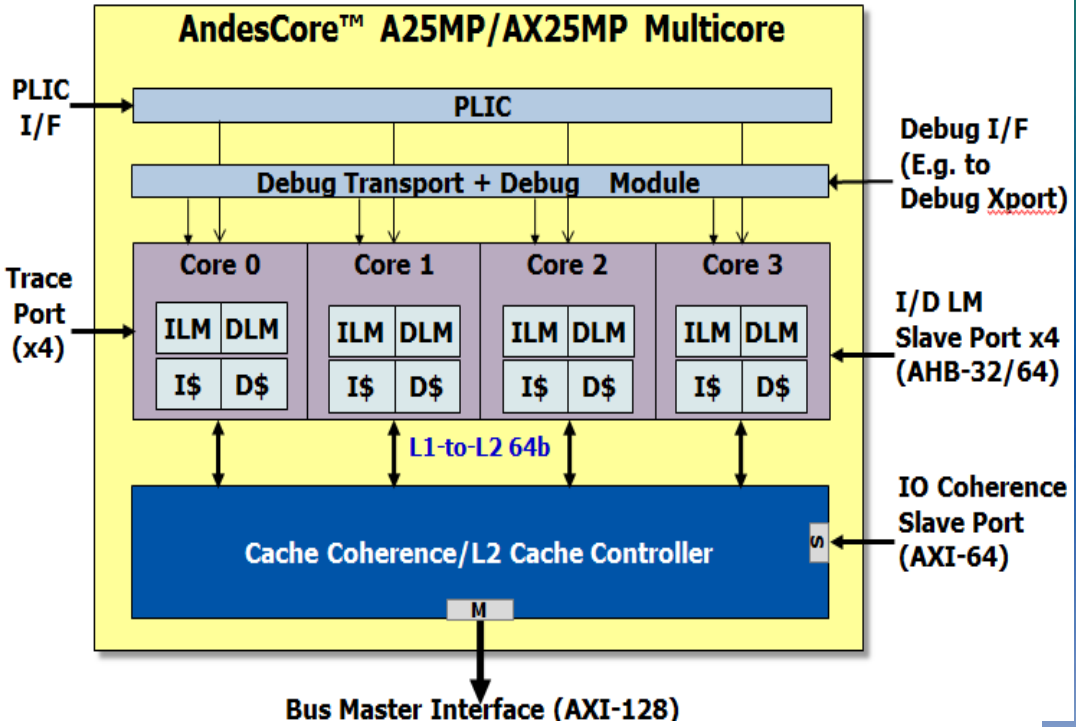
V5 AndesCores: 22-系列

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension
- **2-stage pipeline with AHB-lite main bus**
- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller
- **28nm PPA:**
  - **700 MHz** (worst case)
  - **16K gates** (minimal)
- **Best per-MHz performance:**
  - **1.8 DMIPS** (no inline)
  - **3.95 Coremark**



A(X)25MP Cache-Coherent Multicore

- **1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs**
  - RV-GCP ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V
- **Hardware Multicore Cache Coherence**
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches
- **Level-2 Cache Controller**
  - 0/128/256K…2MB, 32-byte line, 16-way
  - ECC, SECDED support
- **Bus Interfaces**
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio
- **Platform Level Interrupt, Debug and Trace Support**



ACE: Andes Custom Extension

Verilog user.v

concise RTL

semantics, operands, test-case spec

script user.ace

COPILOT

Custom-OPtimized Instruction deveLOpment Tools

Automated Env. For Cross Checking

Test Case Generator

Extended RTL

Extended ISS

Extended Tools + Compiler Asm/Disasm Debugger IDE

Extended ISS + CPU ISS (near-cycle accurate)

Extended RTL + CPU RTL

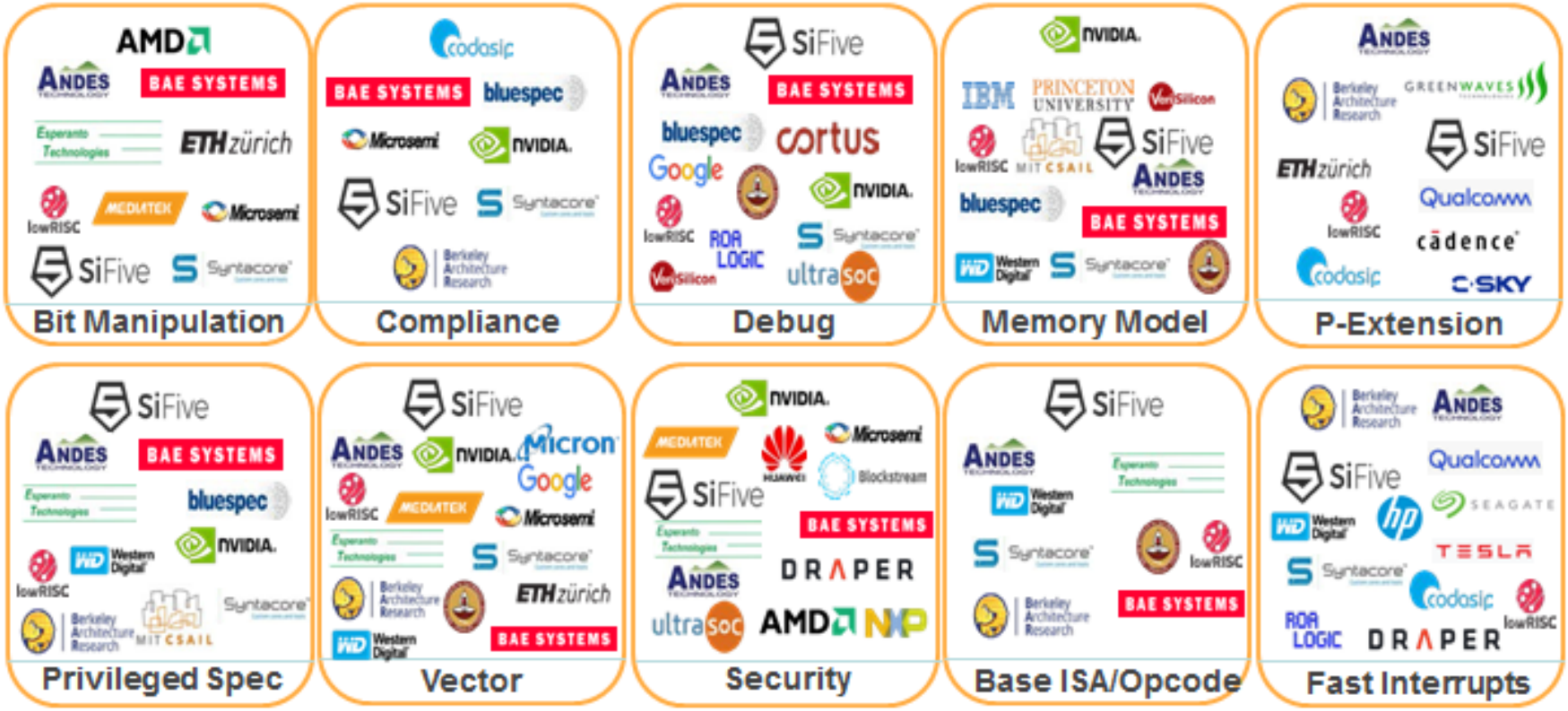
Extensible Baseline Components

Executable or library

Source file

積極參與RISC-V社群活動

Foundation Task Groups (partial list)



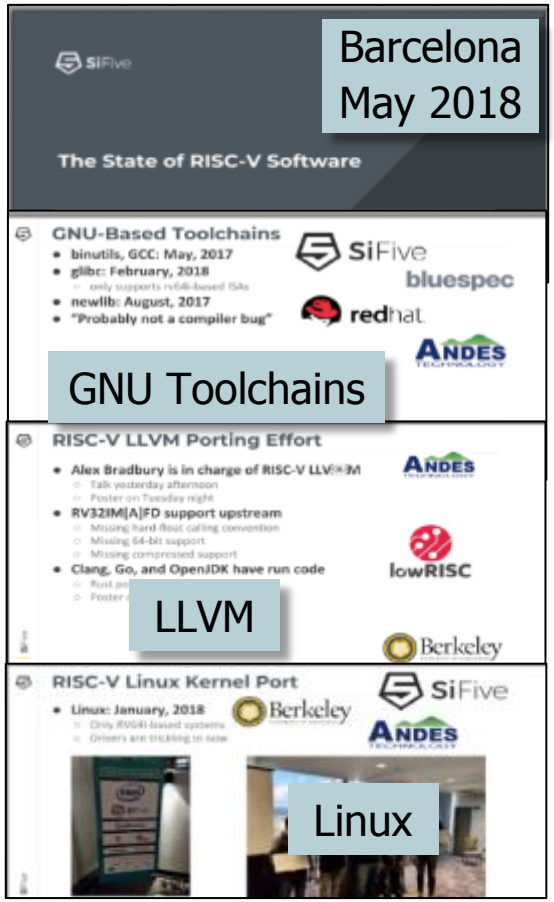
- **Contributing hardware architecture extensions**
  - **Chair of the P-extension (Packed SIMD/DSP) Task Group**
  - **Co-chair of Fast Interrupts Task Group**
  - **Closely reviewing activities of other Task Groups**

晶心協助強化RISC-V生態系統

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem

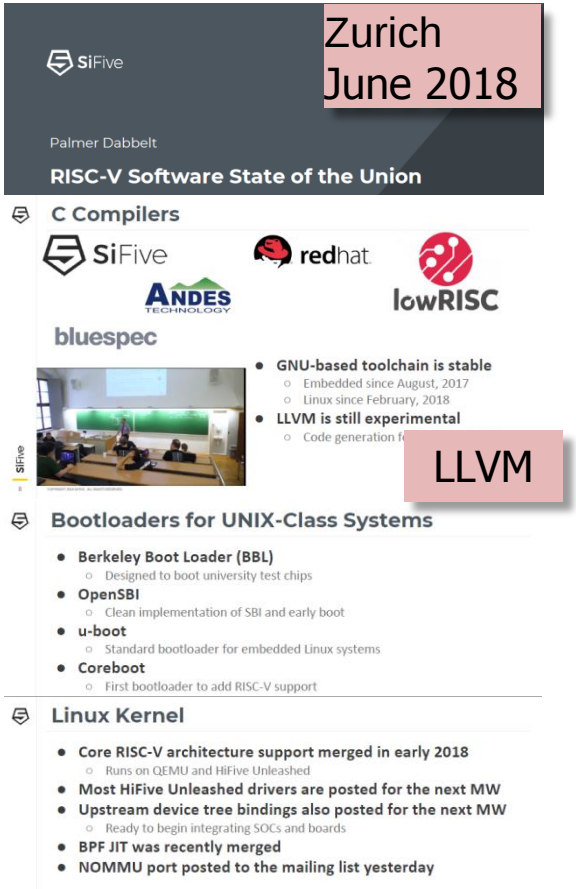
RISC-V 軟體生態系統: GNU Toolchain

- **GCC, binutils**: May, 2017
- **Newlib**: Aug, 2017
- **Glibc (rv64i)**: Feb, 2018
- **GDB**: Mar, 2018
- **OpenOCD**: July, 2018
- **Glibc (rv32i)**:
  - Submitted in July 2018 (by Andes)
  - Review in progress



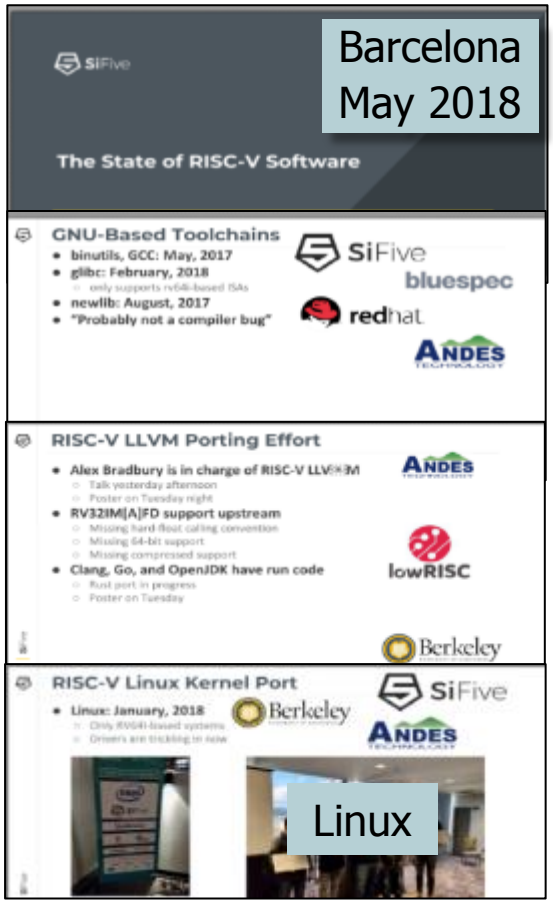
RISC-V 軟體生態系統: LLVM Compilation

- **LLVM**:
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Change status into "official" from LLVM 9: Sep, 2019 (est.)
- **compiler-rt**: Mar, 2018
- **LLD**: Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation



RISC-V 軟體生態系統: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)



晶心在 RISC-V 上的定位

完整的產品組合

可靠的 RISC-V 核心 IP 供應商

超低功耗、高運算效能的處理器核心

領先世界推出具有客戶可自訂指令的 RISC-V處理器核心

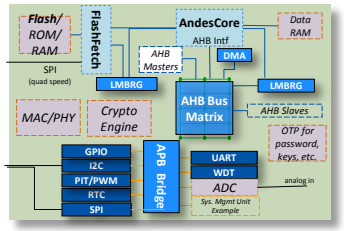
生態系統: Andes 與 Knect.me

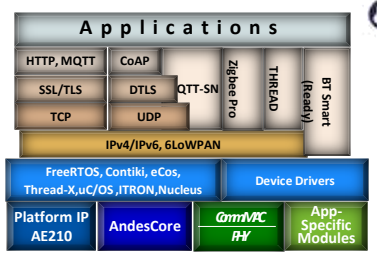
ANDES TECHNOLOGY

knectme™

Knect.me 生態系統

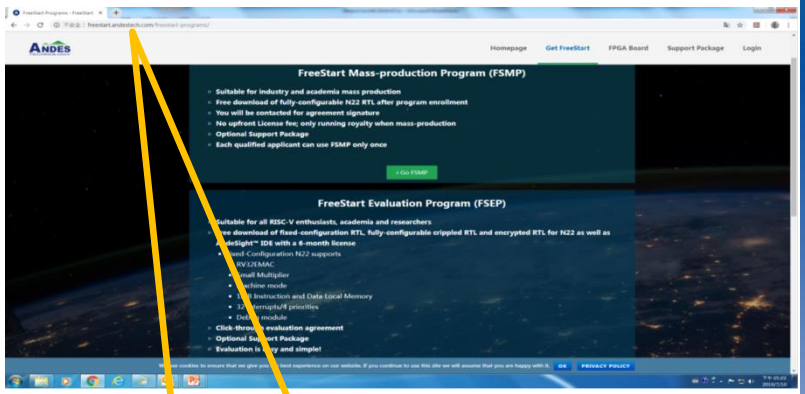
- **Built up Ecosystem *knect.me* to help IoT Developing**
  - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products
- **Includes:**
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools
- **To Form a IoT League**
  - to **knect** chip vendors, partners, application developers, system vendors





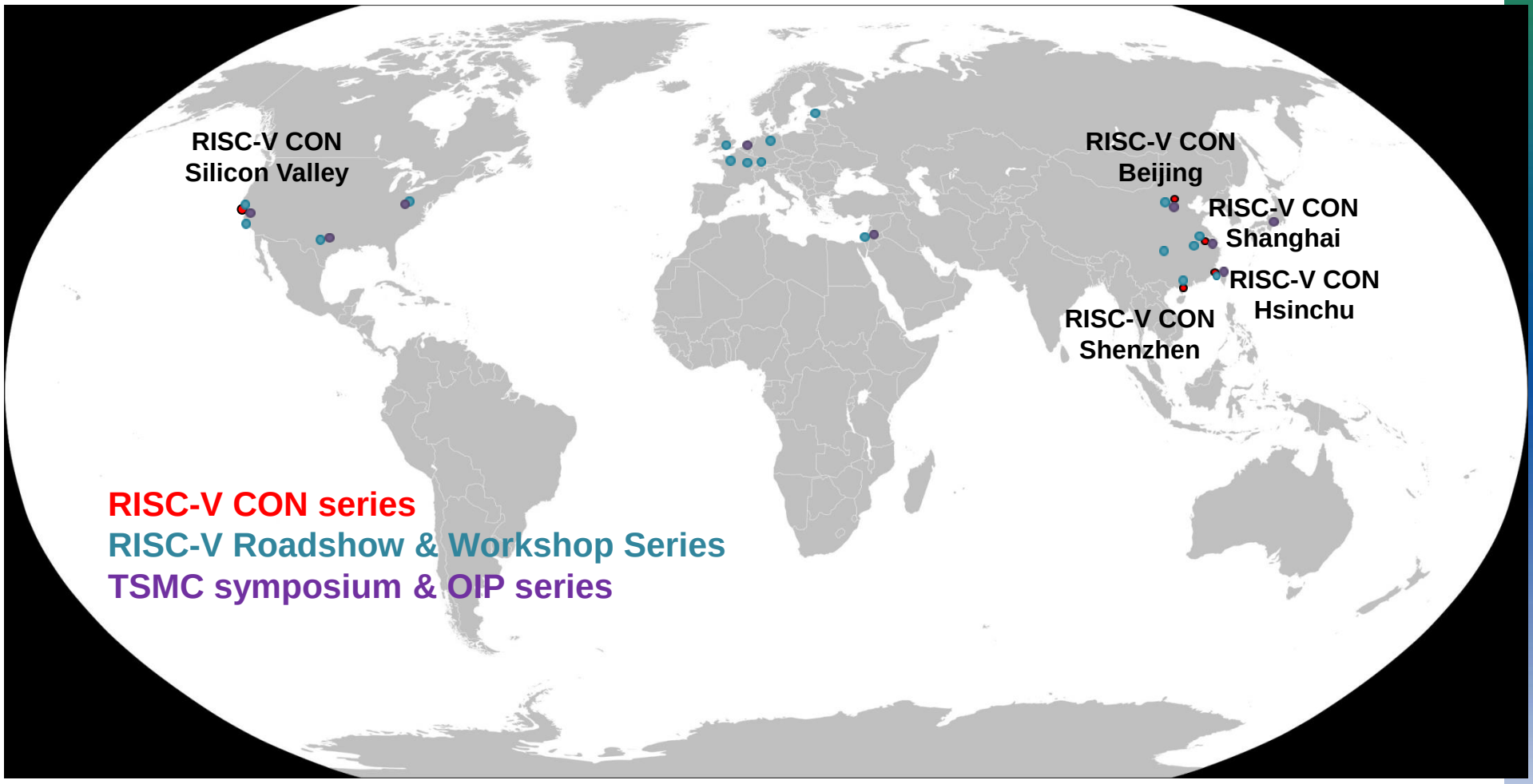
FreeStart Program

- **FreeStart Evaluation Program (FSEP)**
  - For all RISC-V enthusiasms and educator/researcher
  - Good for N22 evaluation and research project
  - Fixed-Configuration N22 RTL
  - Sign simple evaluation agreement directly on website
- **FreeStart Mass-production Program (FSMP)**
  - For industrial and academy mass production
  - Full-configuration N22
  - License fee: $0; only running royalty is required when mass production
- **Support Package (FSSP)**
  - For all
  - $20K for 1st year, including
    - 1 year e-service
    - FreeStart AE250 RTL
    - Corvette F1 FPGA board



For more info., please visit www.andestech.com

2019 Event Promotion

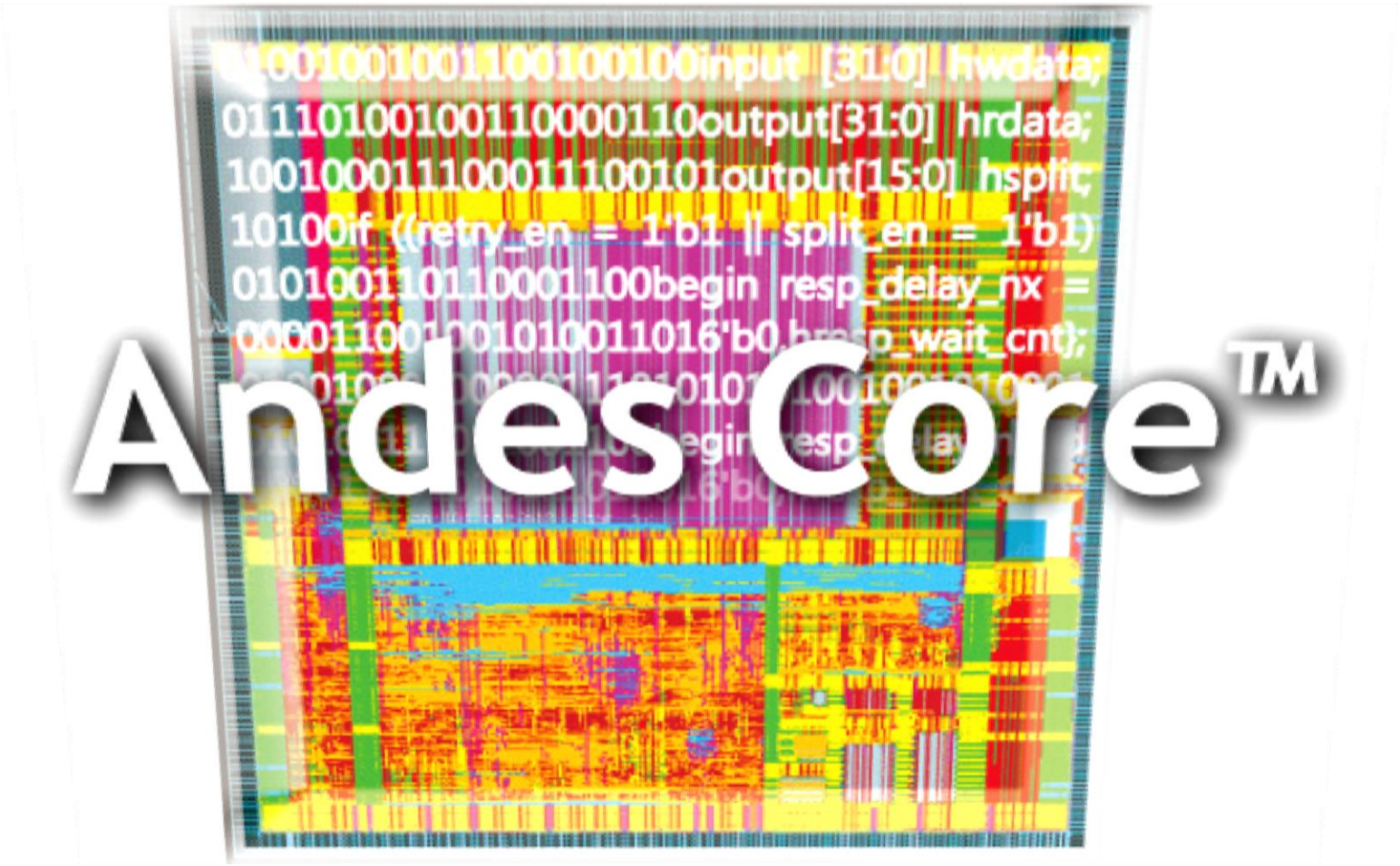


總結

晶心科技: Trusted Computing Expert

- 晶心科技今年已陸續推出了6個新的RISC-V cores、客制化CPU技術服務以及FreeStart Program來拓展更多的客戶應用與商機。
- 晶心科技積極參與 RISC-V 基金會科技與社群發展，並與RISC-V 生態系統互助。
- 晶心科技持續與全球超過15家Design service houses簽訂合約，授權其協助客戶開發內嵌 Andes RISC-V core的ASIC (稱為Andes RISC-V Easy Start Program)，創造晶心、Design service house與客戶共贏的局面。
- 成為RISC-V產業中之技術貢獻者、市場推廣者、銷售領導者

謝謝指教



www.andestech.com

問與答