Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
Agenda

- Overview of Andes Technology Corporation
- Operating Results
- Product Applications
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks
Overview of Andes Technology Corporation

Andes Highlights

• Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
• Well-established high technology IPO company
• Just over 180 people; 80% are engineers.
• EETimes' Silicon 60 Hot Startups to Watch (2012)
• TSMC OIP Award “Partner of the Year” for New IP (2015)
• A founding member of RISC-V Foundation (2016)
• MCU innovation award by China online press (2018)

Andes Mission

• Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

• Smart and Green electronic devices
• Cloud Computing and Internet of Things and Machine Learning
Operating Results
Business Status Overview

- >160 commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
  - >300 license agreements signed

- AndeSight™ IDE:
  - >14,000 installations

- Eco-system:
  - >140 partners

- >3.9B Accumulative SoC Shipped
  (by 2019 Q1)
Agreement Growth Analysis

<table>
<thead>
<tr>
<th>Year</th>
<th>IP agreements</th>
<th>Accumulated IP agreements</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2007</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>2008</td>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td>2009</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>2010</td>
<td>12</td>
<td>24</td>
</tr>
<tr>
<td>2011</td>
<td>16</td>
<td>40</td>
</tr>
<tr>
<td>2012</td>
<td>16</td>
<td>56</td>
</tr>
<tr>
<td>2013</td>
<td>24</td>
<td>80</td>
</tr>
<tr>
<td>2014</td>
<td>27</td>
<td>107</td>
</tr>
<tr>
<td>2015</td>
<td>27</td>
<td>134</td>
</tr>
<tr>
<td>2016</td>
<td>31</td>
<td>165</td>
</tr>
<tr>
<td>2017</td>
<td>39</td>
<td>204</td>
</tr>
<tr>
<td>2018</td>
<td>43</td>
<td>247</td>
</tr>
<tr>
<td>1H19</td>
<td>58</td>
<td>305</td>
</tr>
</tbody>
</table>
2Q19 Revenue Analysis

QoQ: +98.3%

Year-over-Year: +76.4%

(NT$ thousands)

2Q18: 88,087
1Q19: 78,386
2Q19: 155,410
2Q19 Top 10 Customers Analysis by Revenue

Top 10 Customer Contributed 77% Revenue

(NT$ thousands)

AI (US) 5G (US) Touch Panel (TW) Sensing (TW) Touch Panel (TW) Storage (US) AI (TW) AI (TW) TDDI (EU) AI (CN)

AI (US) 5G (US) Touch Panel (TW) Sensing (TW) Touch Panel (TW) Storage (US) AI (TW) AI (TW) TDDI (EU) AI (CN)
2Q19 Royalty Analysis

- **YoY**: +58.3%
- **QoQ**: -7.4%

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Royalty (NT$ thousands)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Q18</td>
<td>14,053</td>
</tr>
<tr>
<td>1Q19</td>
<td>24,021</td>
</tr>
<tr>
<td>2Q19</td>
<td>22,245</td>
</tr>
</tbody>
</table>
2Q19 Top Ten Royalty Contributors Analysis by Application

Top 10 Royalty Customers Contribution Analysis: 94%

(NT$ thousands)
## Royalty Analysis

(NT$ thousands)

<table>
<thead>
<tr>
<th>Year</th>
<th>Royalty (NT$ thousands)</th>
<th>Customers</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>445</td>
<td>1</td>
</tr>
<tr>
<td>2012</td>
<td>660</td>
<td>2</td>
</tr>
<tr>
<td>2013</td>
<td>1,285</td>
<td>5</td>
</tr>
<tr>
<td>2014</td>
<td>10,819</td>
<td>9</td>
</tr>
<tr>
<td>2015</td>
<td>12,232</td>
<td>15</td>
</tr>
<tr>
<td>2016</td>
<td>13,320</td>
<td>15</td>
</tr>
<tr>
<td>2017</td>
<td>38,287</td>
<td>25</td>
</tr>
<tr>
<td>2018</td>
<td>74,953</td>
<td>28</td>
</tr>
<tr>
<td>1H19</td>
<td>$46,266</td>
<td>26</td>
</tr>
</tbody>
</table>

- **Royalty Analysis**: 1H19 royalty collected
- **Unit**: 家數 (Customers)
- **Note**: The royalties and customer numbers are presented in NT$ thousands and customers respectively.
### Consolidated Gross Margin

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>2Q18</th>
<th>1Q19</th>
<th>2Q19</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross Profit</td>
<td>88,001</td>
<td>78,098</td>
<td>155,311</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>99.90%</td>
<td>99.63%</td>
<td>99.94%</td>
</tr>
</tbody>
</table>
Consolidated Operating Expenses

- **YoY** +106.2%
- **QoQ** +28.8%

<table>
<thead>
<tr>
<th></th>
<th>2Q18</th>
<th>1Q19</th>
<th>2Q19</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&amp;D expenses</td>
<td>25,270</td>
<td>54,110</td>
<td>61,635</td>
</tr>
<tr>
<td>Administration expenses</td>
<td>17,567</td>
<td>18,088</td>
<td>18,400</td>
</tr>
<tr>
<td>Selling expenses</td>
<td>21,129</td>
<td>30,226</td>
<td>51,883</td>
</tr>
</tbody>
</table>

(NT$ thousands)

- 2Q18: 63,966
- 1Q19: 102,424
- 2Q19: 131,918

*Driving Innovations™*
Consolidated Operating Income (Loss)

- YoY: -2.7%
- QoQ: - %

2Q18: 24,035
1Q19: (24,326)
2Q19: 23,393

(NT$ thousands)
Consolidated Operating Margin

- Year-over-year (YoY) change: -12.22 pt
- Quarter-over-quarter (QoQ) change: +46.08 pt

2Q18: 27.28%
1Q19: (31.03%)
2Q19: 15.05%
Consolidated Net Income (Loss)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Net Income (Loss) (NT$ thousands)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Q18</td>
<td>29,582</td>
</tr>
<tr>
<td>1Q19</td>
<td>(23,599)</td>
</tr>
<tr>
<td>2Q19</td>
<td>25,209</td>
</tr>
</tbody>
</table>

YoY -14.8%  
QoQ - %
Consolidated Net Profit Margin

- QoQ: +46.33 pt
- YoY: -17.36 pt

(NT$ thousands)

- 2Q18: 33.58%
- 1Q19: (30.11%)
- 2Q19: 16.22%

-10.00% to +40.00% range
Consolidated Earnings Per Share

1H19 EPS: 0.04

<table>
<thead>
<tr>
<th>Q</th>
<th>EPS (NT$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Q18</td>
<td>0.69</td>
</tr>
<tr>
<td>1Q19</td>
<td>-0.30</td>
</tr>
<tr>
<td>2Q19</td>
<td>0.59</td>
</tr>
</tbody>
</table>
1H19 Revenue Analysis by Payment Model

- License Fee: 61%
- Running Royalty: 20%
- Custom Computing Service: 14%
- Maintenance & Others: 5%
1H19 Revenue Analysis by Region

- Taiwan: 42%
- USA: 33%
- China: 17%
- Europe: 5%
- Korea: 2%
- Japan: 1%
1H19 Customer Application Analysis

*Based on agreement number
1H19 Revenue Analysis by Product
2Q19 Revenue Analysis - RISC-V

<table>
<thead>
<tr>
<th></th>
<th>V3</th>
<th>RISC-V</th>
<th>Custom Computing</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Q18</td>
<td>64,230</td>
<td>23,857</td>
<td>27.1%</td>
</tr>
<tr>
<td>1Q19</td>
<td>40,240</td>
<td>21,575</td>
<td>27.5%</td>
</tr>
<tr>
<td>2Q19</td>
<td>53,086</td>
<td>85,584</td>
<td>55.1%</td>
</tr>
</tbody>
</table>

(NT$ thousands)
1H19 Revenue Analysis - RISC-V

(NT$ thousands)

1H18

- V3: 94,535 (23.0%)
- RISC-V: 28,233
- Custom Computing: 6,362

1H19

- V3: 93,325
- RISC-V: 107,159 (45.8%)
- Custom Computing: 33,312

Revenue Analysis
Product Application
Andes Updates

- A 14-year-old public CPU IP company
- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involvement in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group

GNU Toolchains
LLVM
Linux
Example Applications of Andes-Embedded™ SoC

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
- ESL
- Smart Meter
- Smart Lighting

- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

- Communication & IoT
- Industrial & Video
- Consumer & Storage & Sensor

and more.....
IoT Application -1

- Bluetooth Speaker
- Sigfox LPWAN
- Healthcare device
- Wearable device
- Electronic price tags
- Sensor Hub
IoT Application -2

**Wearable devices**

**Portable Karaoke**

**GPS/Beido in shared bikes**

**Drone**

**WiFi/GPS/FM/Bluetooth combo**

**Contactless payment (NFC)**
Andes Embedded in Smart Phones

1 in 5 Smart Phones are with Andes Embedded

- Sensor Hub
- NFC Controller
- Storage Controller
- WiFi/ BT/ GPS/ FM (combo)
- Touch Screen Controller
Andes Embedded in Consumer Devices, Cars and Datacenters

- Switch: MXIC Flash Ctrl
- Echo Dot2: Mediatek WiFi IoT
- Bike Sharing: GPS Ctrl
- X-Trail: ADAS Ctrl

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)
New Products and Ecosystems
Product Lines

- New A-series Cores released in Andes Embedded Forum 2018

ANDES

RISC-V
Andes RISC-V Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

Highly optimized design with leading PPA

AndesCore™ Processors

AndeSight™ Tools

Professional IDE with high code quality

Handy peripheral IPs to speed up SoC construction

AndeShape™ Platforms

Extensive SW stacks from bare metal, RTOS to Linux

AndeSoft™ Stacks
V5 AndesCore™ Processors

N22
N25F/NX25F/D25F
A25/AX25
A25MP/AX25MP
## AndesCore™ RISC-V Families

<table>
<thead>
<tr>
<th>Cache-Coherent Multicores</th>
<th>A25MP</th>
<th>AX25MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2/4 A25, L2$, L1/IO coherence</td>
<td>1/2/4 AX25, L2$, L1/IO Coherence</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Linux with FPU/DSP</th>
<th>A25</th>
<th>AX25</th>
</tr>
</thead>
<tbody>
<tr>
<td>N25F, MMU, DSP</td>
<td>NX25F, MMU, DSP</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fast/Compact with FPU/DSP</th>
<th>N25F/D25F</th>
<th>NX25F</th>
</tr>
</thead>
<tbody>
<tr>
<td>V5/32b, FPU, PMP, DSP (D25F)</td>
<td>V5/64b, FPU, PMP</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Slim and Efficient</th>
<th>N22</th>
</tr>
</thead>
<tbody>
<tr>
<td>V5[e]/32b, 32/16 GPR</td>
<td></td>
</tr>
</tbody>
</table>

#### Specifications
- **A25MP**: 1/2/4 A25, L2\$, L1/IO coherence
- **AX25MP**: 1/2/4 AX25, L2\$, L1/IO Coherence
- **A25**: N25F, MMU, DSP
- **AX25**: NX25F, MMU, DSP
- **N25F/D25F**: V5/32b, FPU, PMP, DSP (D25F)
- **NX25F**: V5/64b, FPU, PMP
- **N22**: V5[e]/32b, 32/16 GPR

* 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

---

* 5-stage, ACE, > 1.2 GHz*
* 2-stage, 700 MHz*
Bring Andes Strength to RISC-V Core Family

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure
**V5 AndesCores: 25-series**

- **N25F**: 32-bit, **NX25F**: 64-bit
  - From scratch for the best PPA
  - Very configurable

- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses

- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case, w/o caches)
  - Large config: 136K gates, 1.2GHz (worst case, w/ caches)
  - Best-in-class Coremark: 3.58/MHz
V5 AndesCores: 25-series

- Fast-n-small for control tasks in AR/VR, networking, storage, AI
- N25F/NX25F: +FPU
  - +, −, x, x+, x−: pipelined 4 cycles
  - ÷, √: run in the background
  - 15 for SP, 29 for DP
- A25/AX25: +FP +Linux
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- Whetstone/MHz:

![Diagram with performance metrics]
V5 AndesCores: 22-series

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension

- **2-stage pipeline with AHB-lite main bus**

- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller

- **28nm PPA:**
  - 700 MHz (worst case)
  - 16K gates (minimal)

- **Best per-MHz performance:**
  - 1.8 DMIPS (no inline)
  - 3.95 Coremark
A(X)25MP Cache-Coherent Multicore

- **1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs**
  - RV-GCP ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes’ contribution to RISC-V

- **Hardware Multicore Cache Coherence**
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches

- **Level-2 Cache Controller**
  - 0/128/256K...2MB, 32-byte line, 16-way
  - ECC, SECDED support

- **Bus Interfaces**
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio

- **Platform Level Interrupt, Debug and Trace Support**
ACE: Andes Custom Extension

**COPILLOT**
Custom-OPtimized Instruction deveLOpment Tools

- **Extended Tools**
- **Extended ISS**
- **Extended RTL**

**Automated Env. For Cross Checking**
- Test Case Generator
  - Extended RTL
  - Extended ISS

**Concise RTL**
semantics, operands, test-case spec

script user.ace

Verilog user.v

**Extensible Baseline Components**
- Compiler
  - Asm/Disasm
  - Debugger
  - IDE
- CPU ISS
  - (near-cycle accurate)
- CPU RTL

Executable or library
Source file
Aggressive in RISC-V Community

Foundation Task Groups (partial list)

- Contributing hardware architecture extensions
  - Chair of the P-extension (Packed SIMD/DSP) Task Group
  - Co-chair of Fast Interrupts Task Group
  - Closely reviewing activities of other Task Groups
Andes Helps Strengthen RISC-V Ecosystem

► More choices for customers are good
► Andes works closely with partners to grow RISC-V ecosystem
RISC-V Software Ecosystem: GNU Toolchain

- GCC, binutils: May, 2017
- Newlib: Aug, 2017
- Glibc (rv64i): Feb, 2018
- GDB: Mar, 2018
- OpenOCD: July, 2018
- Glibc (rv32i):
  - Submitted in July 2018 (by Andes)
  - Review in progress
RISC-V Software Ecosystem: LLVM Compilation

- **LLVM:**
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Change status into “official” from LLVM 9: Sep, 2019 (est.)

- **compiler-rt:** Mar, 2018

- **LLD:** Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation
RISC-V System Software Ecosystem: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)
Andes Position in RISC-V

- Complete product portfolio
- Reliable RISC-V core IP provider
- Extreme low power consumption, high computing efficiency
- World’s leading Customer-Extension Capable RISC-V Core
Two Ecosystems: Andes and Knect.me
Built up Ecosystem **knect.me** to help IoT Developing
- to **knect** solutions - Silicon IP’s, SW stacks, tools, applications, systems and products

**Includes:**
- SoC IP Platforms
- Software Stack
- Development Boards
- Development Tools

**To Form a IoT League**
- to **knect** chip vendors, partners, application developers, system vendors
FreeStart Program

- **FreeStart Evaluation Program (FSEP)**
  - For all RISC-V enthusiasms and educator/researcher
  - Good for N22 evaluation and research project
  - Fixed-Configuration N22 RTL
  - Sign simple evaluation agreement directly on website

- **FreeStart Mass-production Program (FSMP)**
  - For industrial and academy mass production
  - Full-configuration N22
  - License fee: $0; only running royalty is required when mass production

- **Support Package (FSSP)**
  - For all
  - $20K for 1st year, including
    - 1 year e-service
    - FreeStart AE250 RTL
    - Corvette F1 FPGA board
2019 Event Promotion

RISC-V CON series
RISC-V Roadshow & Workshop Series
TSMC symposium & OIP series
Concluding Remarks
Andes: Trusted Computing Expert

- Andes stretched out for more opportunities in 1H’19 thru the launch of x6 new RISC-V cores, custom design service and FreeStart program.
- Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.
- Andes has successively signed >15 contracts with design service houses to authorize ASIC design to embed RISC-V core (i.e. Andes RISC-V EasyStart Program) for creating a "win-win" situation.
- Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry
Thank You!

www.andestech.com