

Andes Technology Corporation 2Q19 Investor Conference Report

Driving Innovations™



Stock #: 6533
2019/08/12

Safe Harbor Notice



Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

Agenda

- **Overview of Andes Technology Corporation**
- **Operating Results**
- **Product Applications**
- **New Products and Ecosystems**
- **Andes Awarded**
- **Concluding Remarks**

Overview of Andes Technology Corporation



Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Just over 180 people; 80% are engineers.
- EETimes' Silicon 60 Hot Startups to Watch (2012)
- TSMC OIP Award "Partner of the Year" for New IP (2015)
- A founding member of RISC-V Foundation (2016)
- MCU innovation award by China online press (2018)



Andes Mission

- Innovate **performance-efficient** processor solution for **low-power** SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

Operating Results

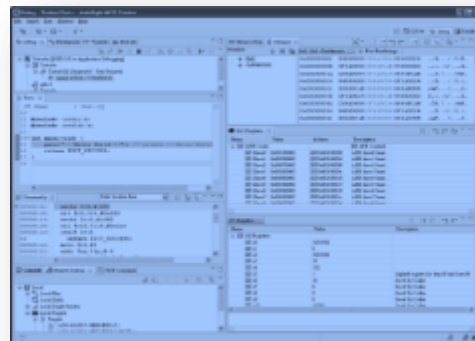


Business Status Overview

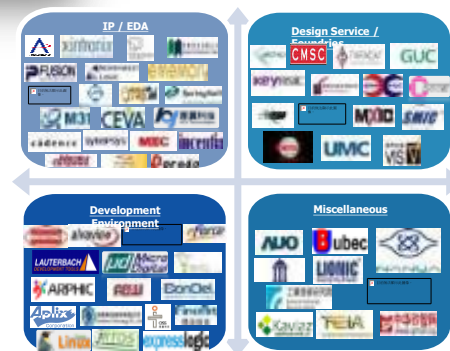
- **>160** commercial licensees
 - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
 - **>300** license agreements signed



- AndeSight™ IDE:
 - **>14,000** installations

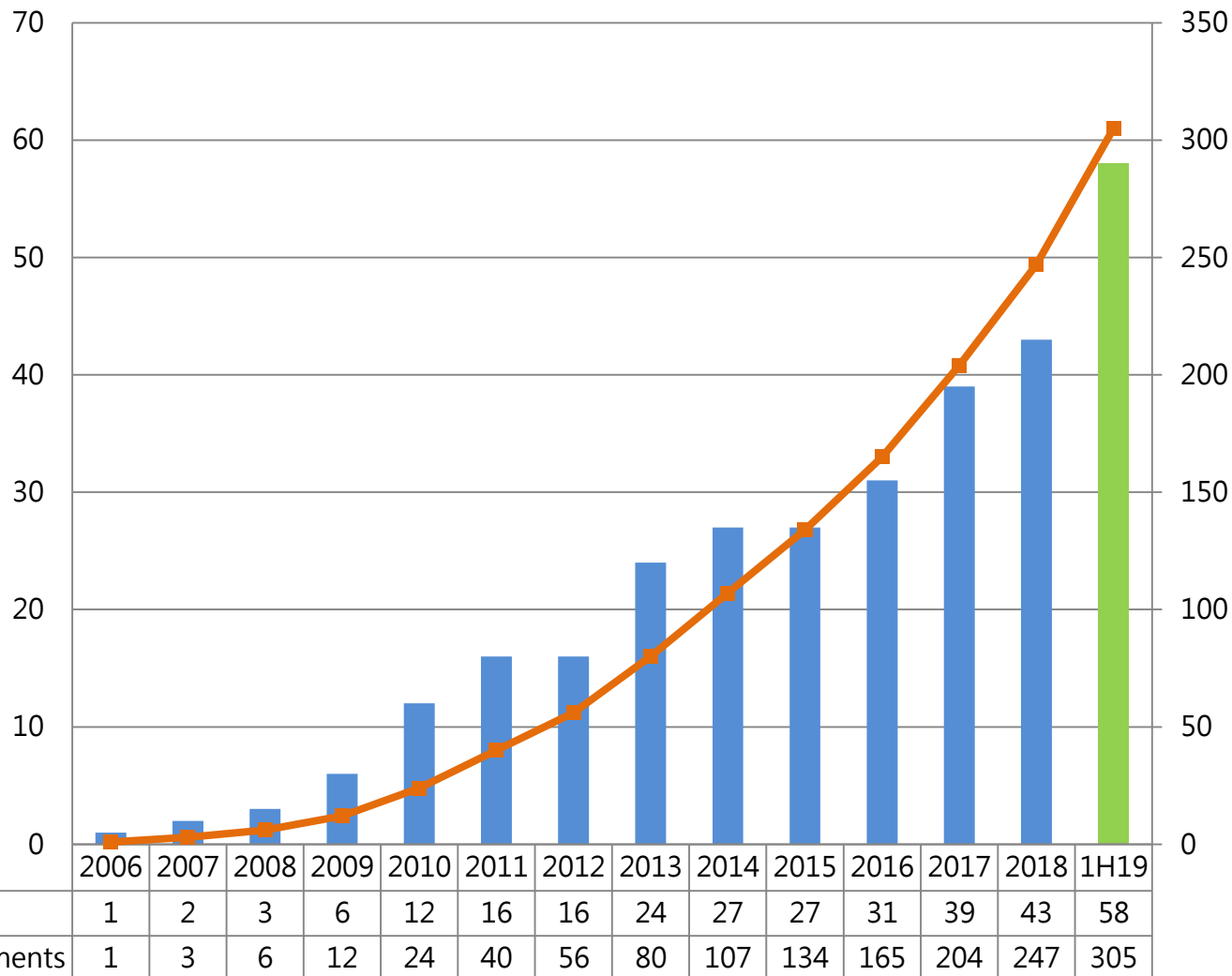


- Eco-system:
 - **>140** partners



- **>3.9B** Accumulative SoC Shipped
(by 2019 Q1)

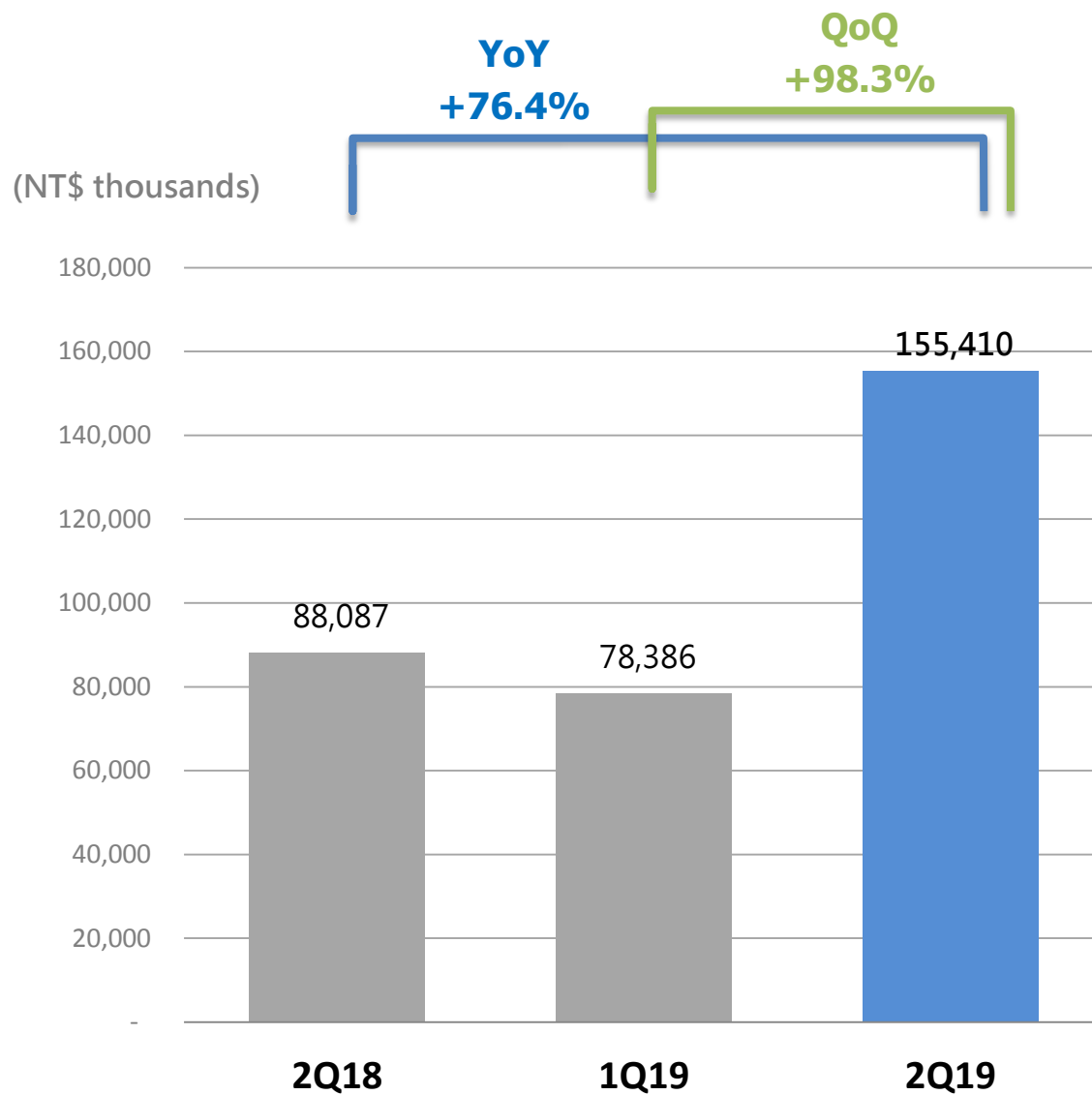
Agreement Growth Analysis



IP agreements

Accumulated IP agreements

2Q19 Revenue Analysis

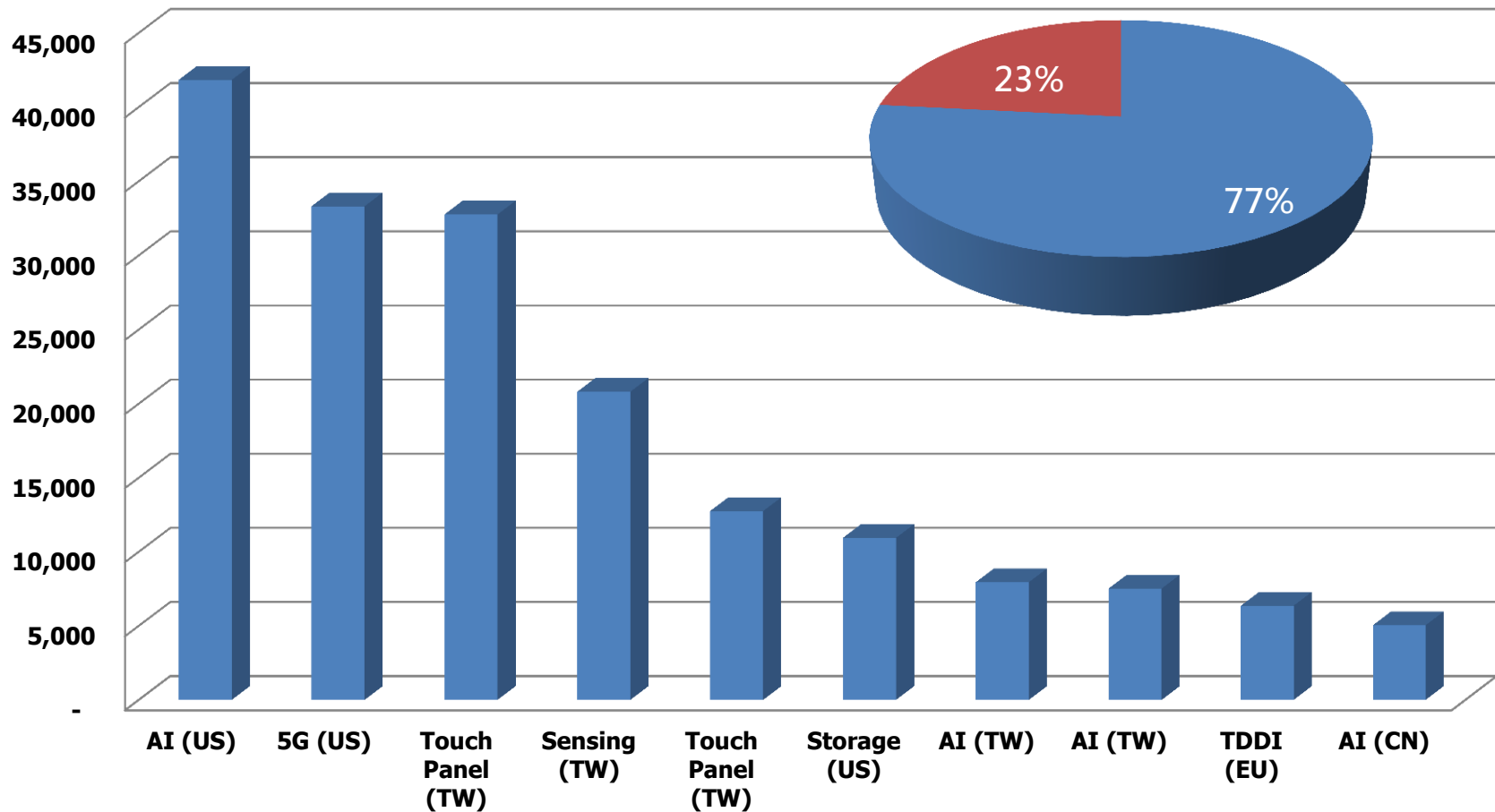


2Q19 Top 10 Customers Analysis by Revenue

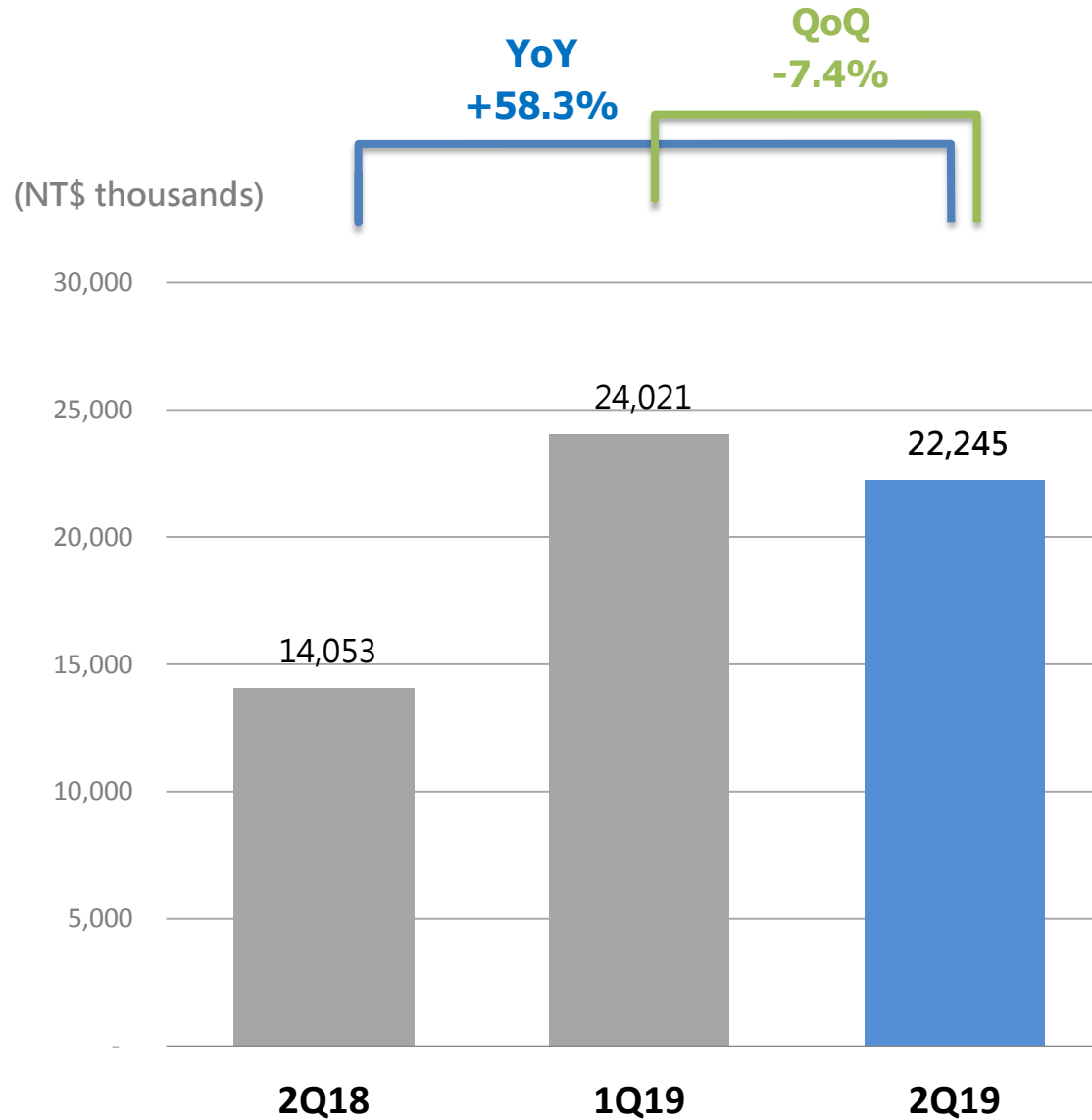


(NT\$ thousands)

Top 10 Customer Contributed 77% Revenue



2Q19 Royalty Analysis

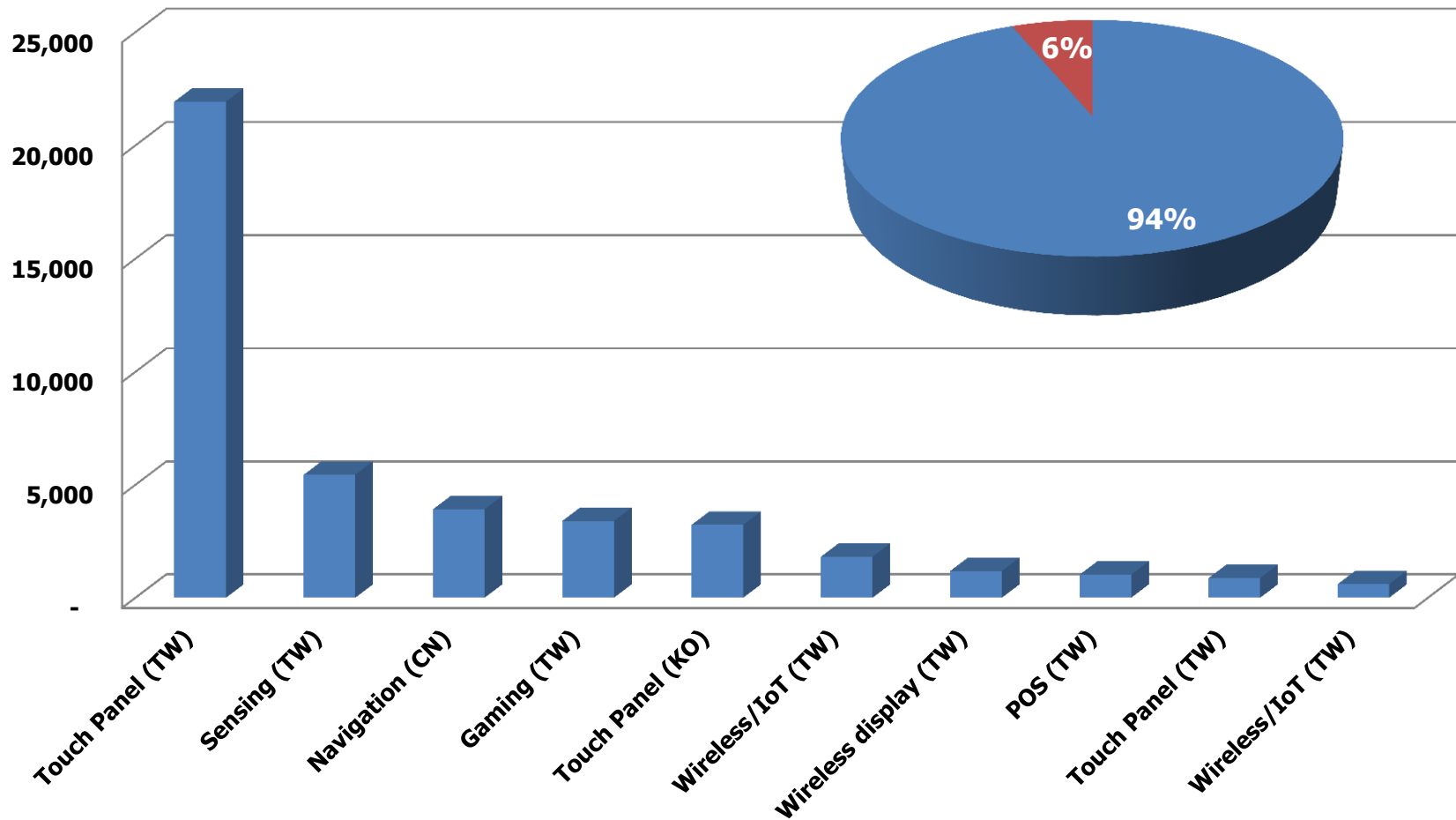


2Q19 Top Ten Royalty Contributors Analysis by Application



(NT\$ thousands)

**Top 10 Royalty Customers
Contribution Analysis: 94%**

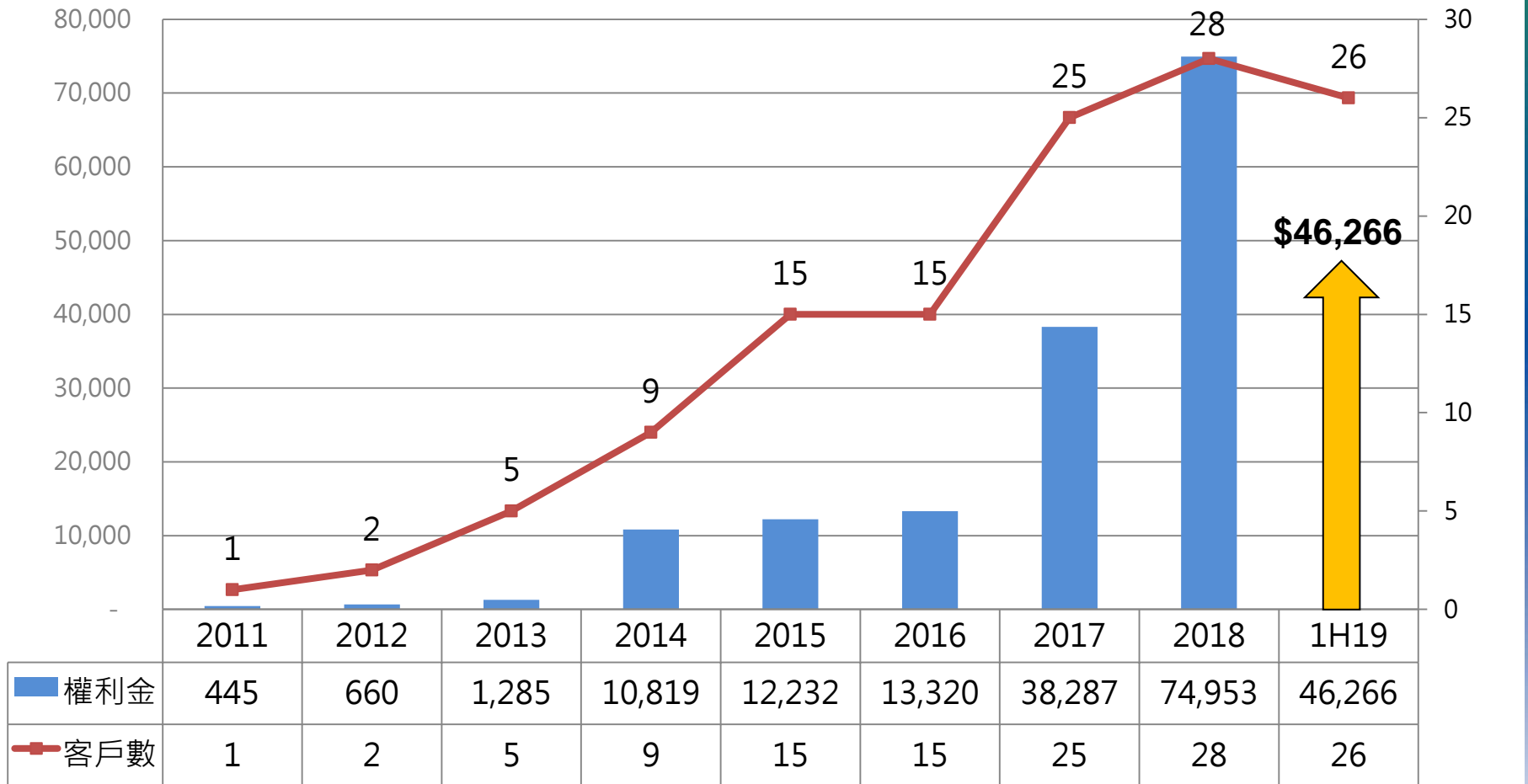


Royalty Analysis



(NT\$ thousands)

↑: 1H19 royalty collected

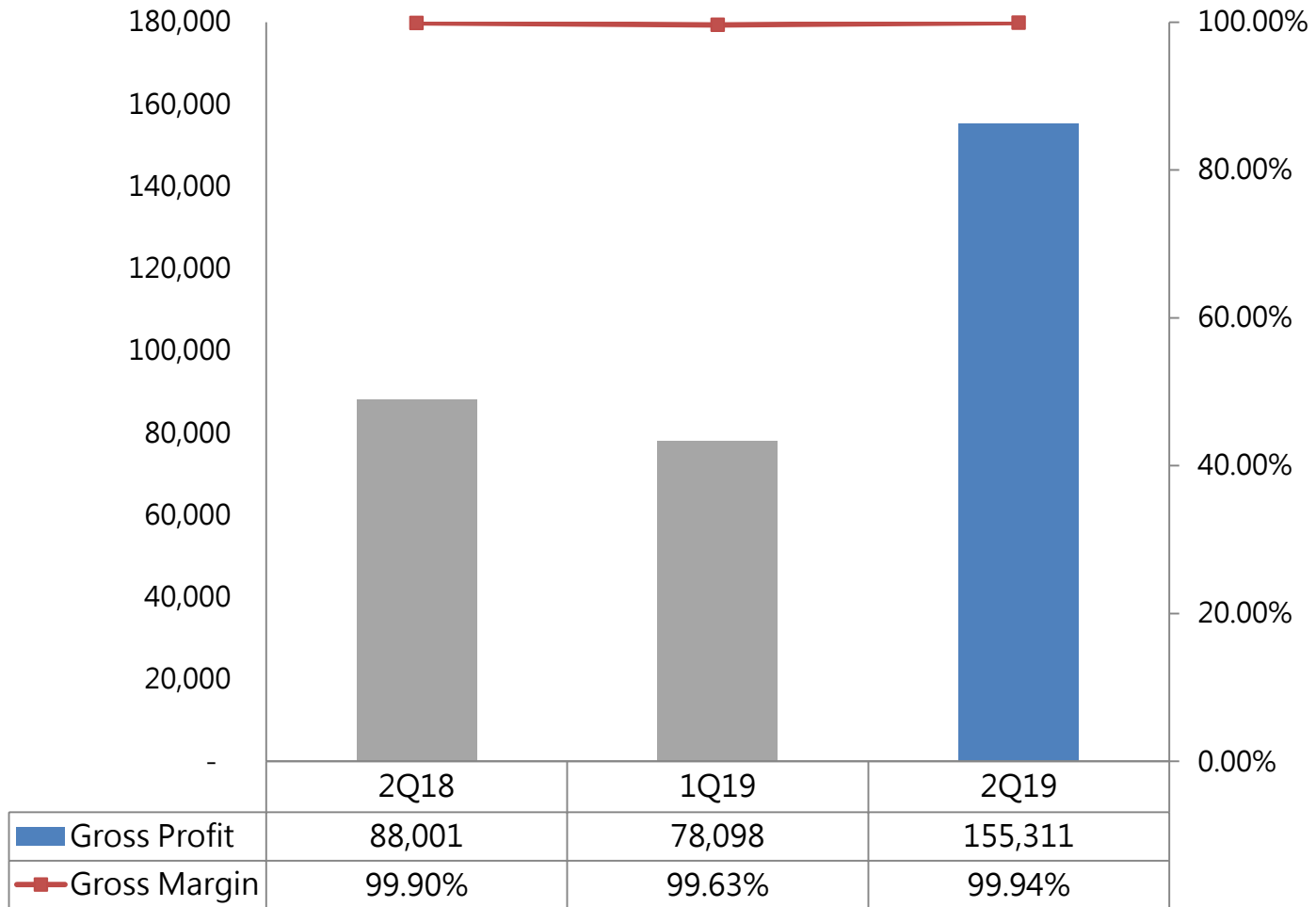


(單位:家數)

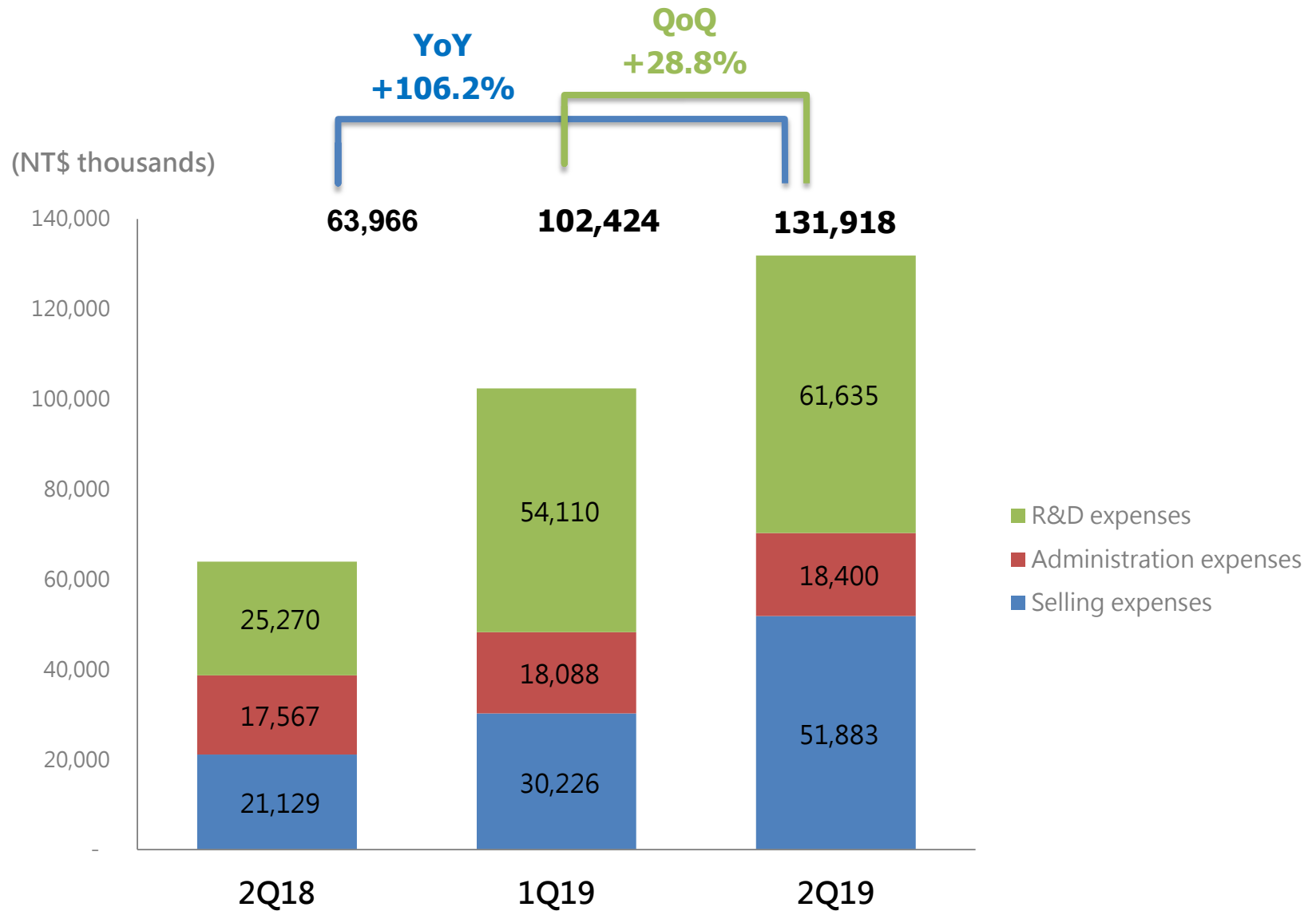
Consolidated Gross Margin



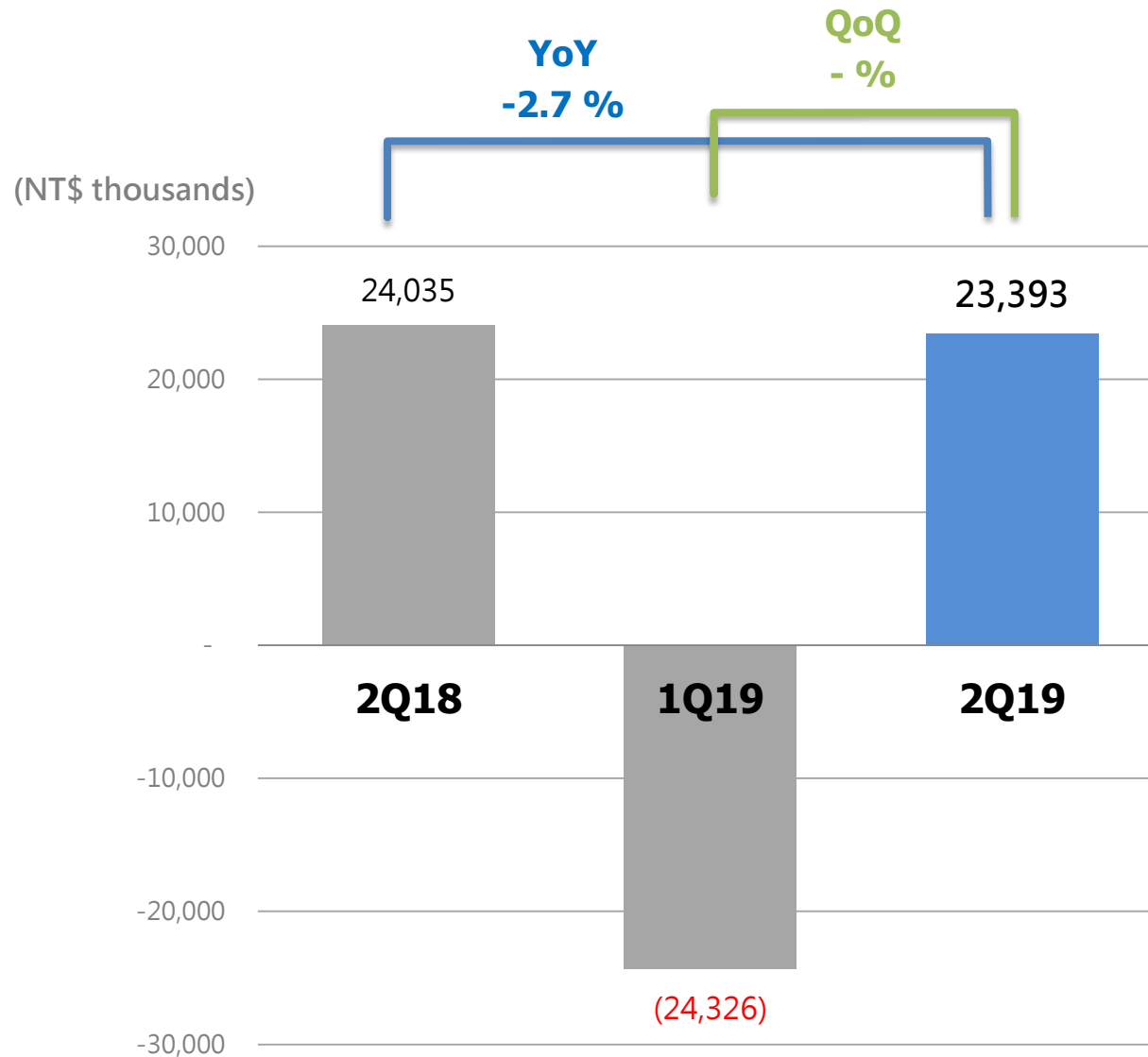
(NT\$ thousands)



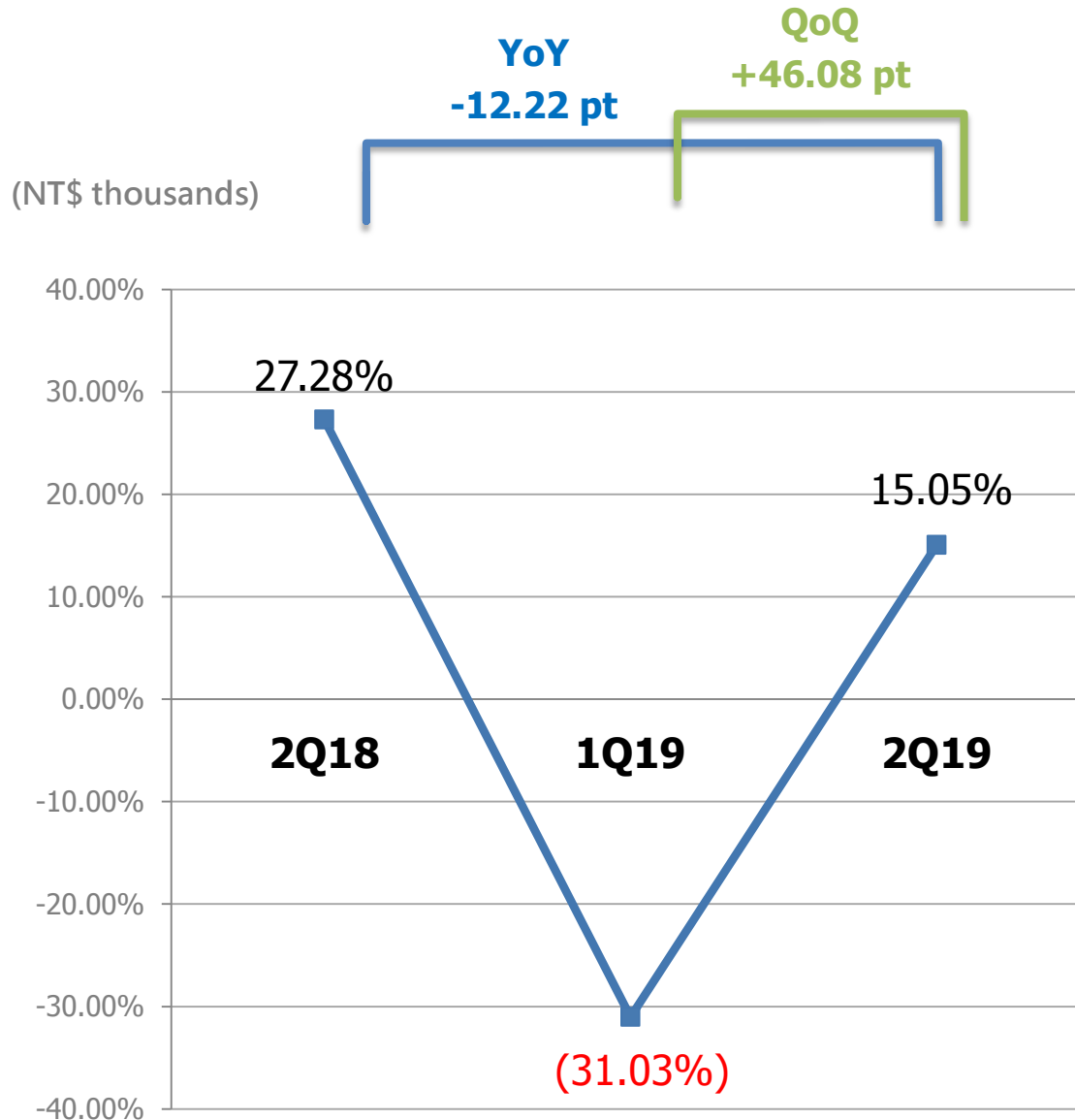
Consolidated Operating Expenses



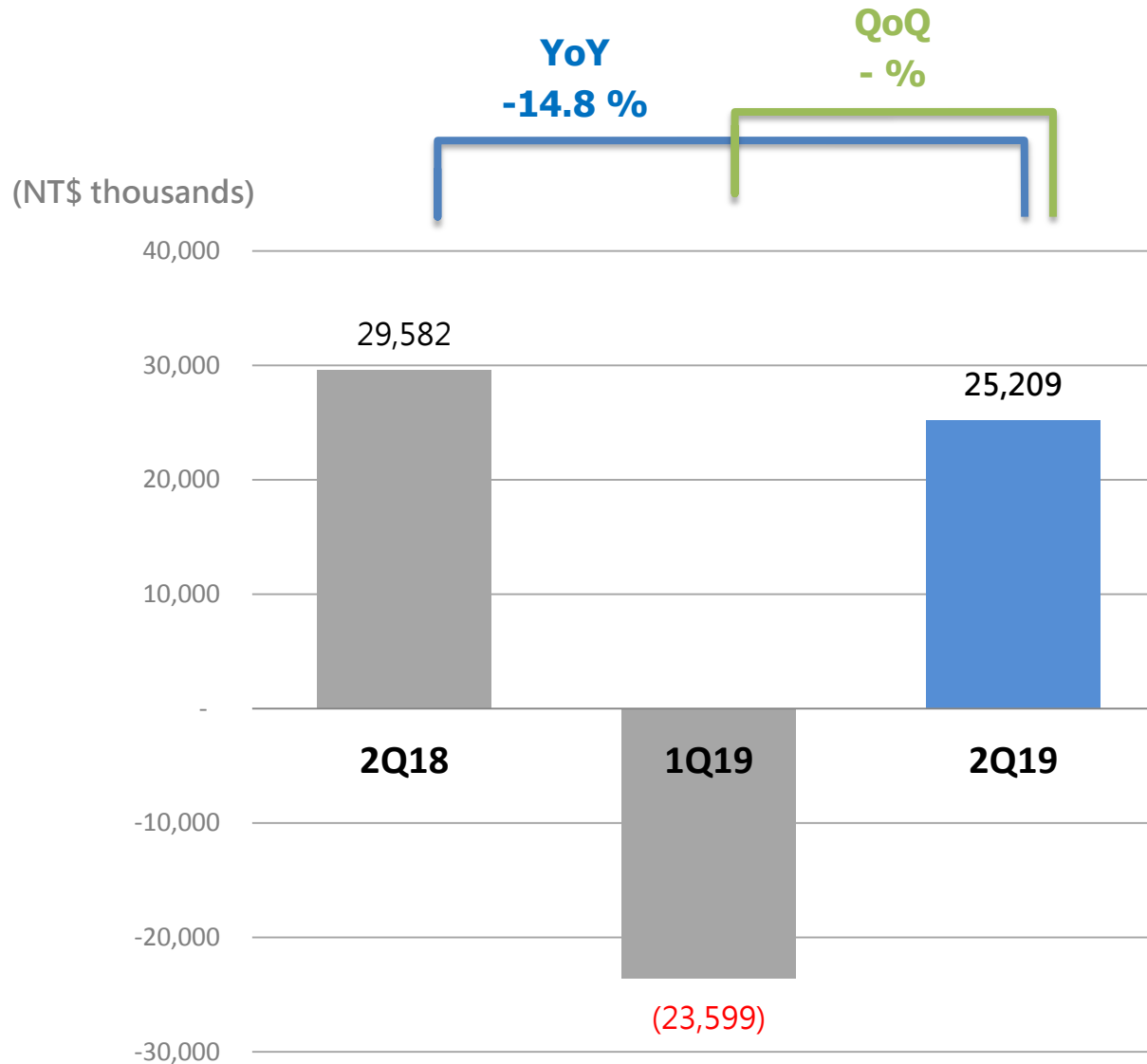
Consolidated Operating Income (Loss)



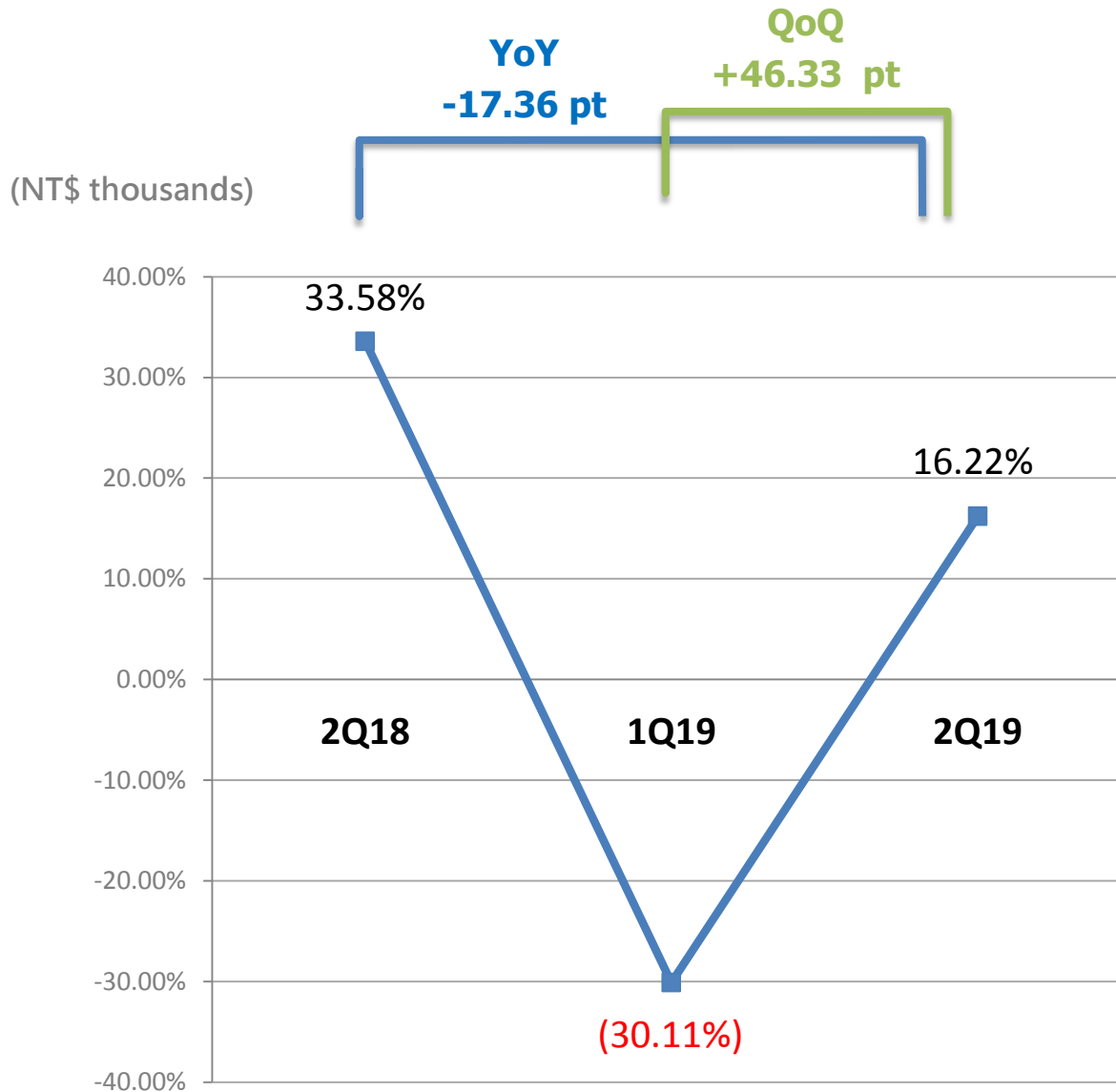
Consolidated Operating Margin



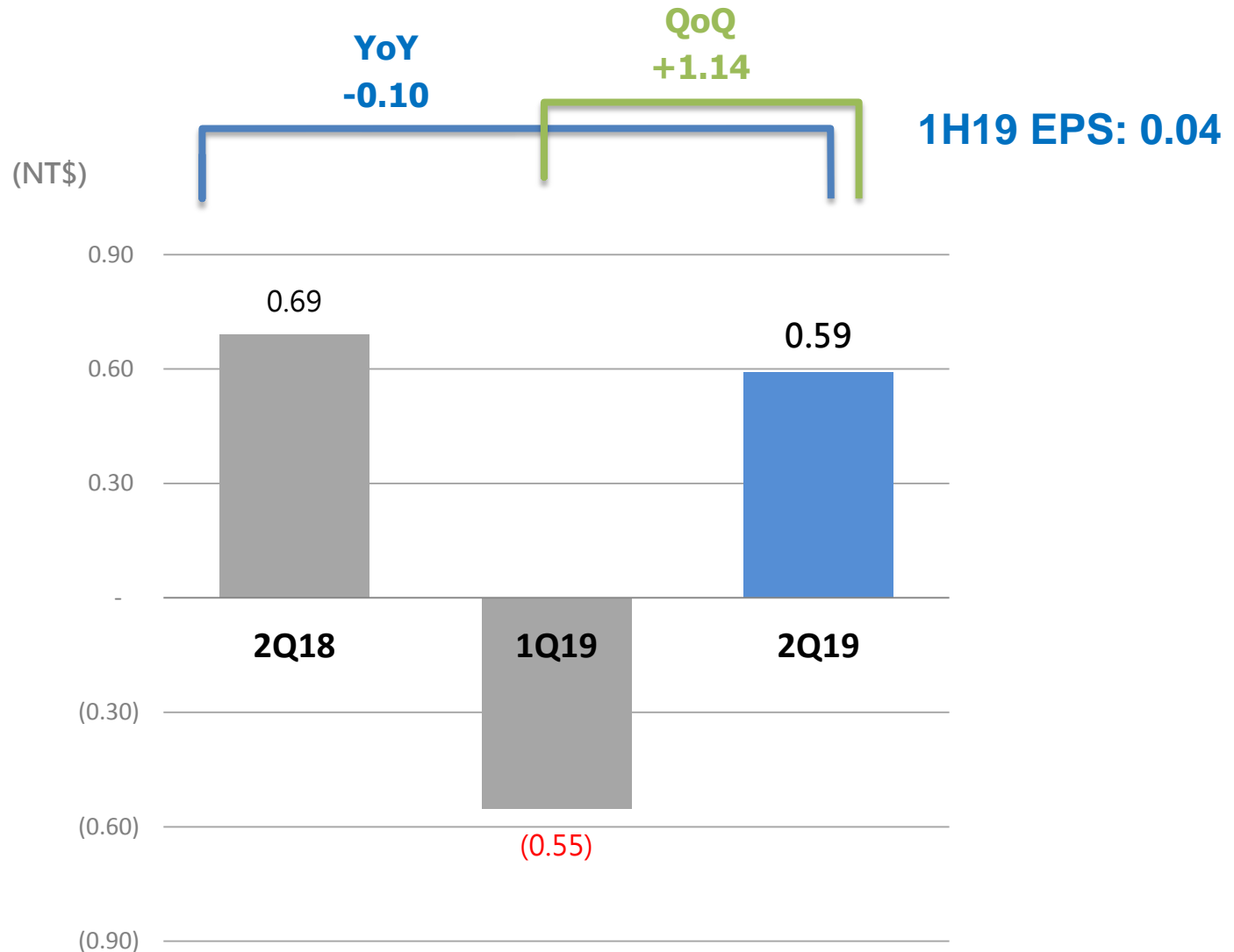
Consolidated Net Income (Loss)



Consolidated Net Profit Margin



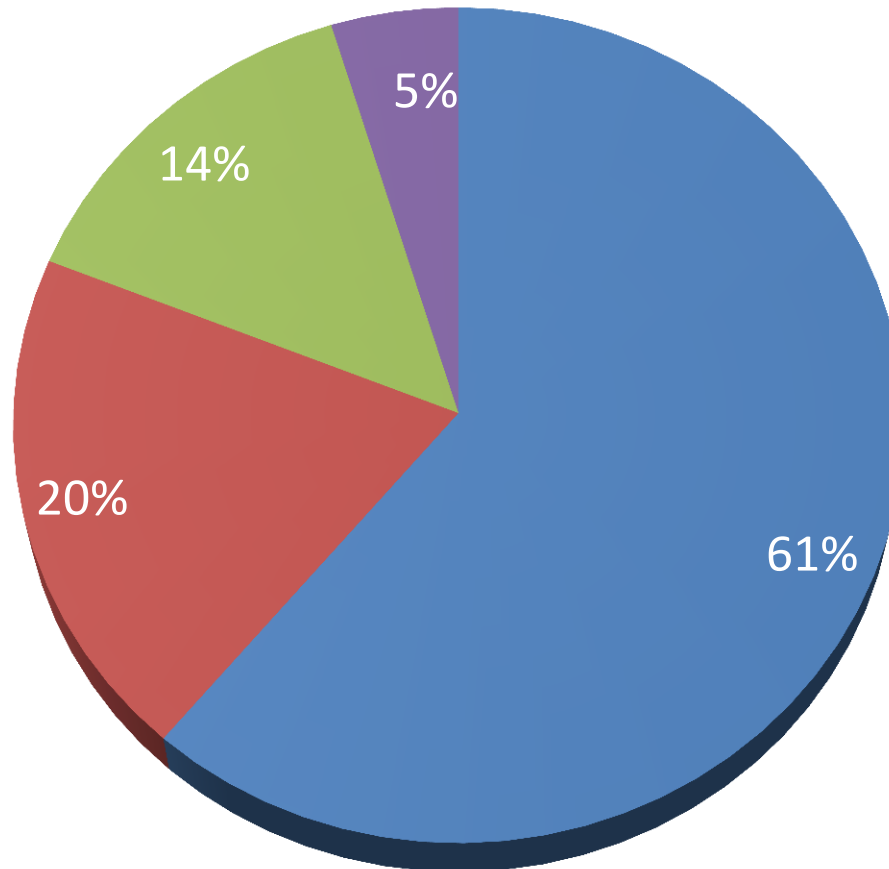
Consolidated Earnings Per Share



1H19 Revenue Analysis by Payment Model



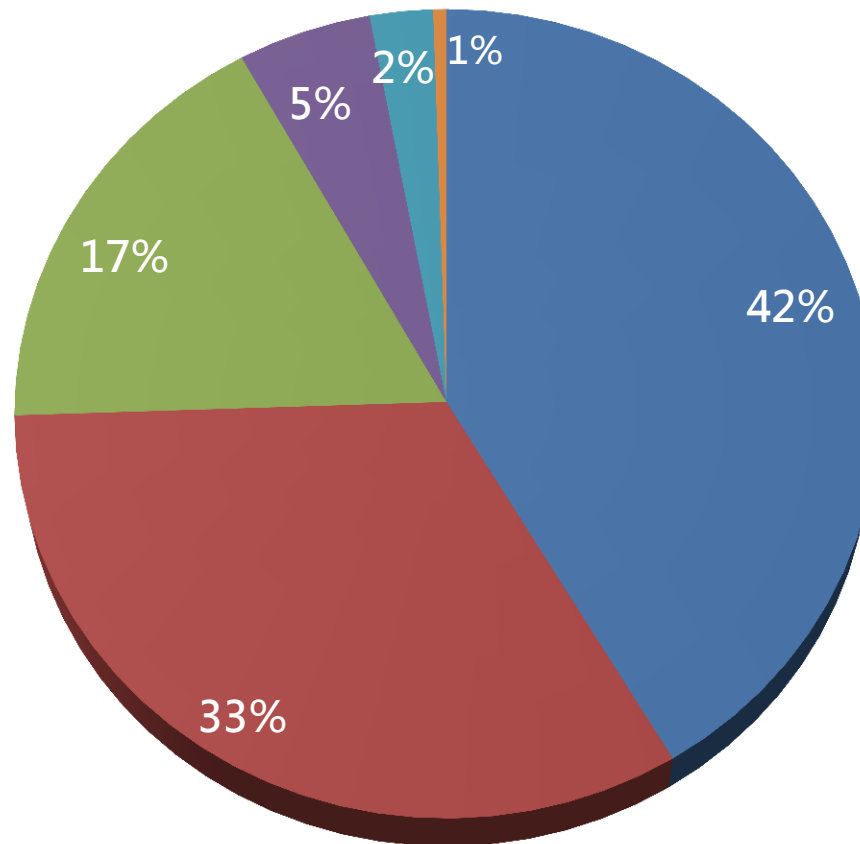
■ License Fee ■ Running Royalty ■ Custom Computing Service ■ Maintenance & Others



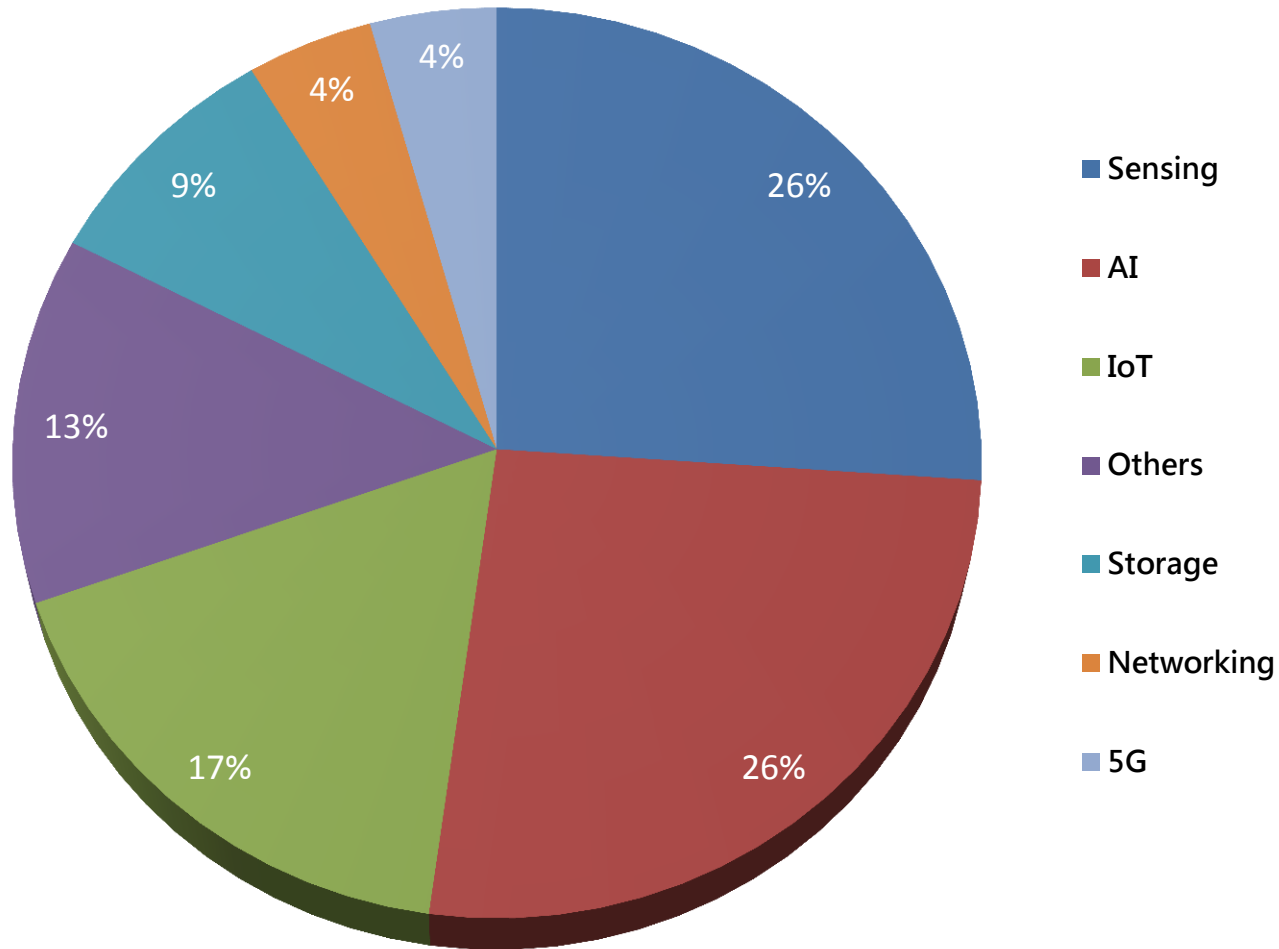
1H19 Revenue Analysis by Region



■ Taiwan ■ USA ■ China ■ Europe ■ Korea ■ Japan

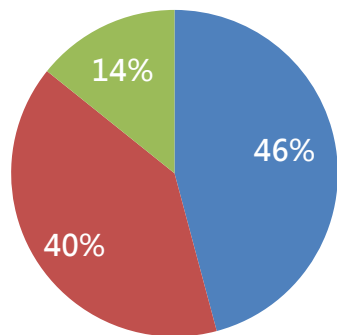


1H19 Customer Application Analysis



*Based on agreement number

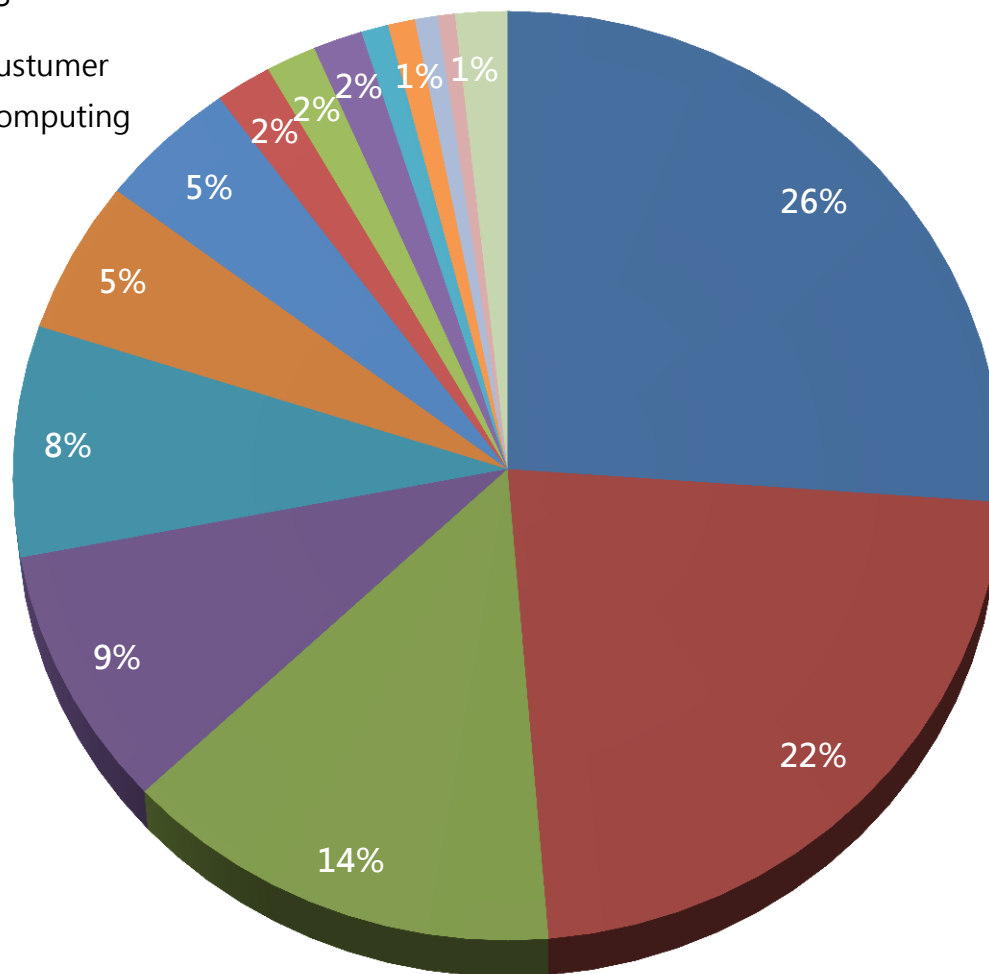
1H19 Revenue Analysis by Product



RISC-V

V3

Customer
Computing



N25

N8

Service

N9

AX25

NX25

ACE

D10

N15

S8

N10

N13

N7

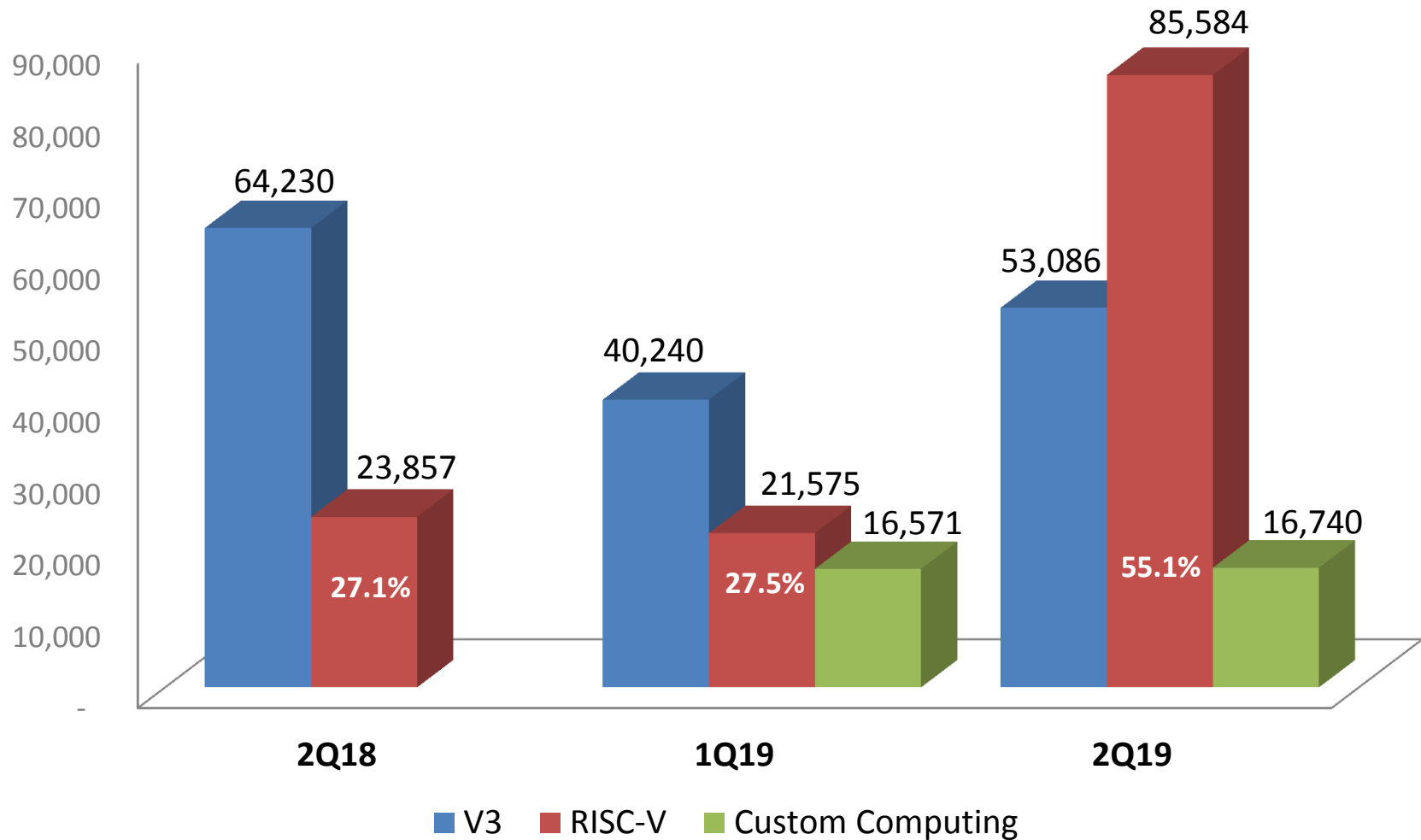
D25

Other

2Q19 Revenue Analysis - RISC-V



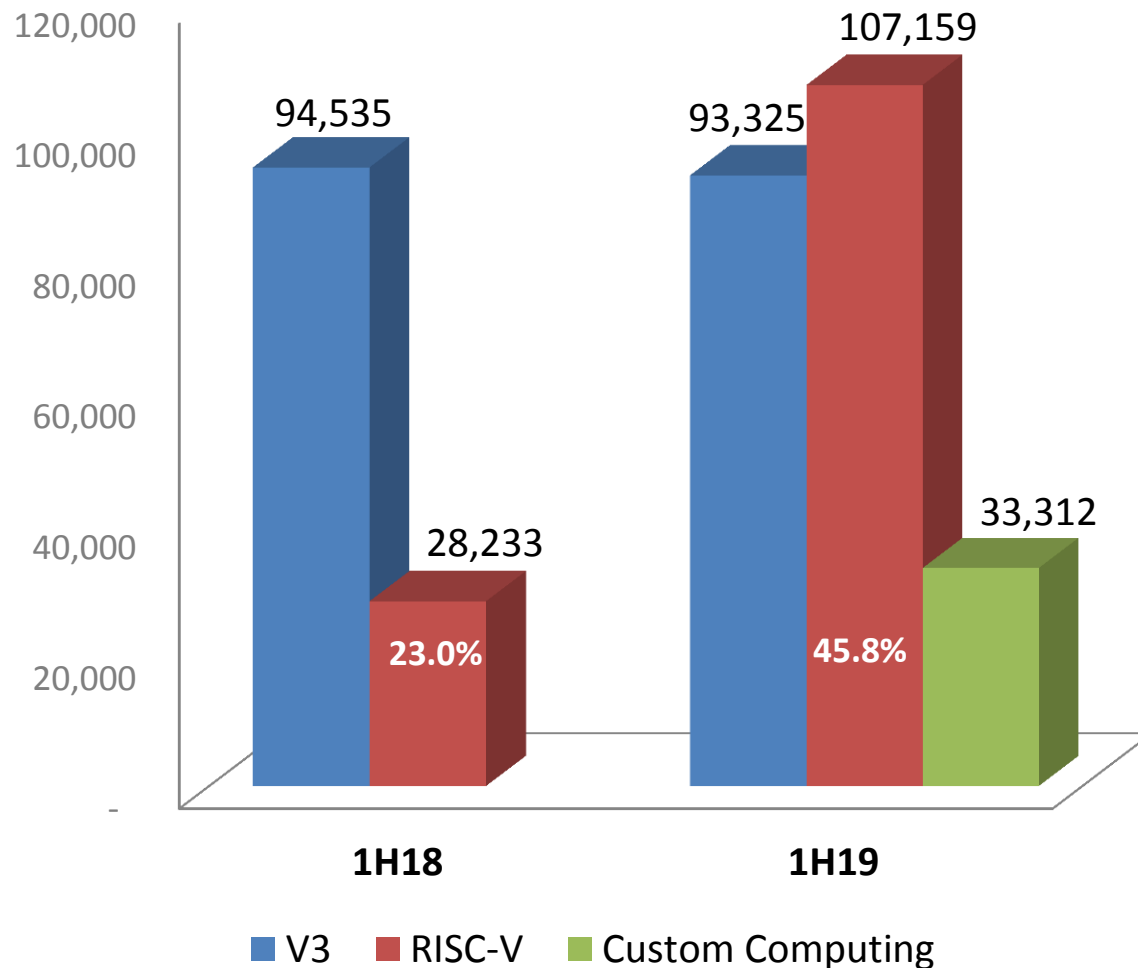
(NT\$ thousands)



1H19 Revenue Analysis - RISC-V



(NT\$ thousands)



Product Application

Andes Updates



❖ A 14-year-old public CPU IP company



❖ A founding member of the RISC-V Foundation

❖ A major open source maintainer/contributor

❖ Active involvement in standard extensions

- Chair of P-extension (Packed DSP/SIMD) Task Group
- Co-chair of Fast Interrupt Task Group

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports rv64i-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

GNU Toolchains

SiFive bluespec
redhat
ANDES TECHNOLOGY

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM
 - Talk yesterday afternoon
 - Poster on Tuesday night
- RV32IM[A]FD support upstream
 - Missing hard-float calling convention
 - Missing 64-bit support
 - Missing compressed support
- Clang, Go, and OpenJDK have run code
 - Rust port in progress
 - Poster on Tuesday

LLVM

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lowRISC
Berkeley

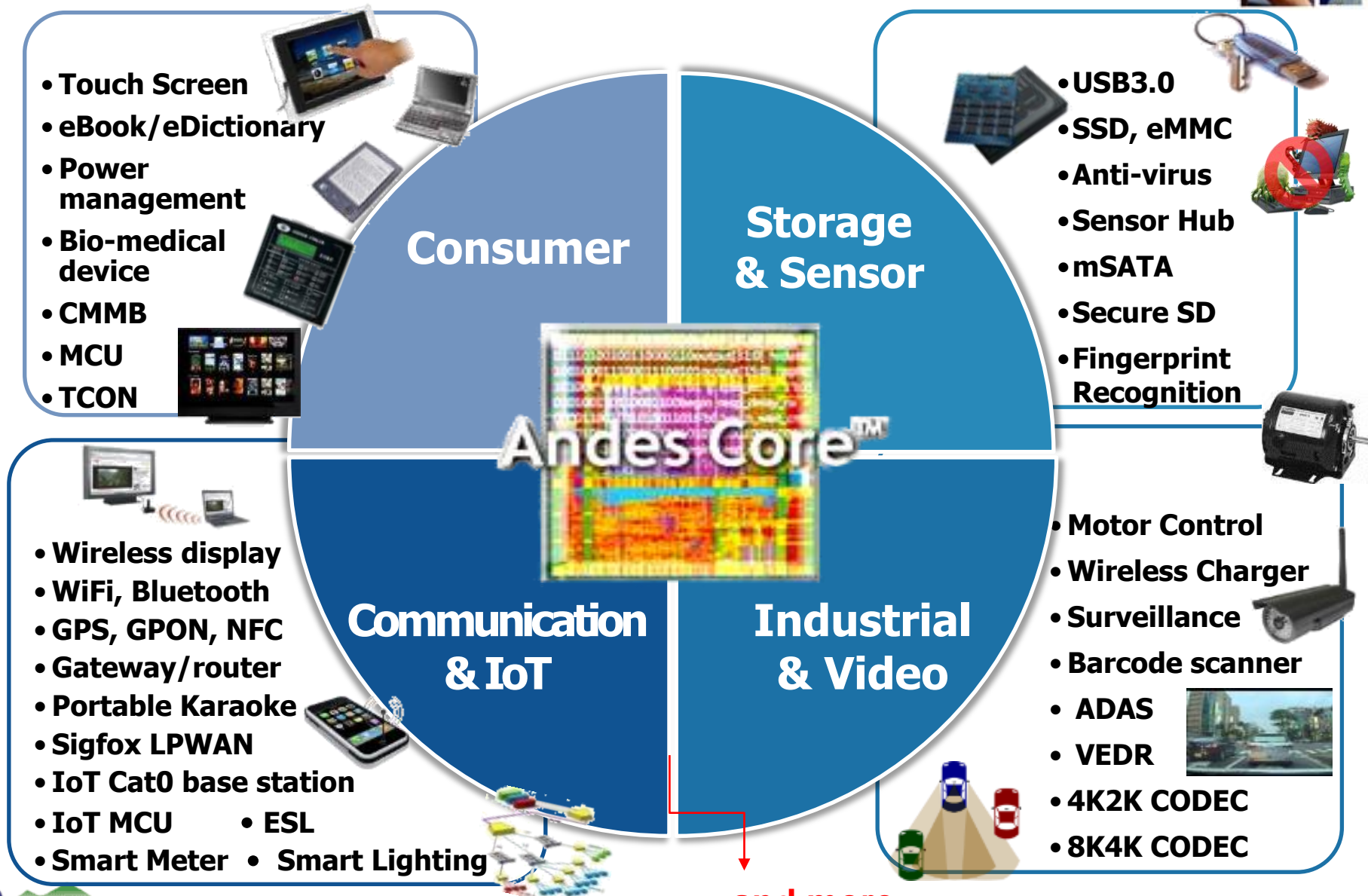
RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64i-based systems
 - Drivers are trickling in now

Linux

Berkeley
SiFive
ANDES TECHNOLOGY

Example Applications of Andes-Embedded™ SoC



and more.....

IoT Application -1



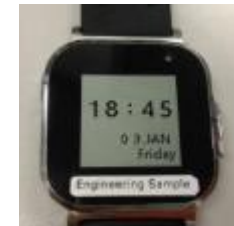
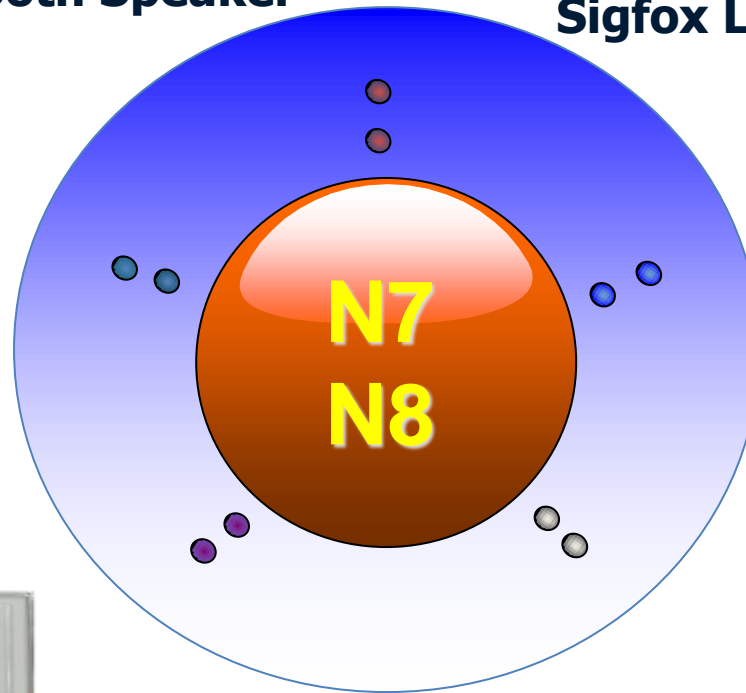
Bluetooth Speaker



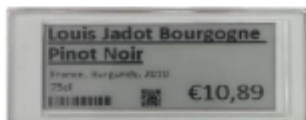
Sigfox LPWAN



Healthcare device



Wearable device



Electronic price tags



Sensor Hub

IoT Application -2



Wearable devices



Drone



Portable Karaoke



**WiFi/GPS/FM/Bluetooth
combo**



GPS/Beido in shared bikes



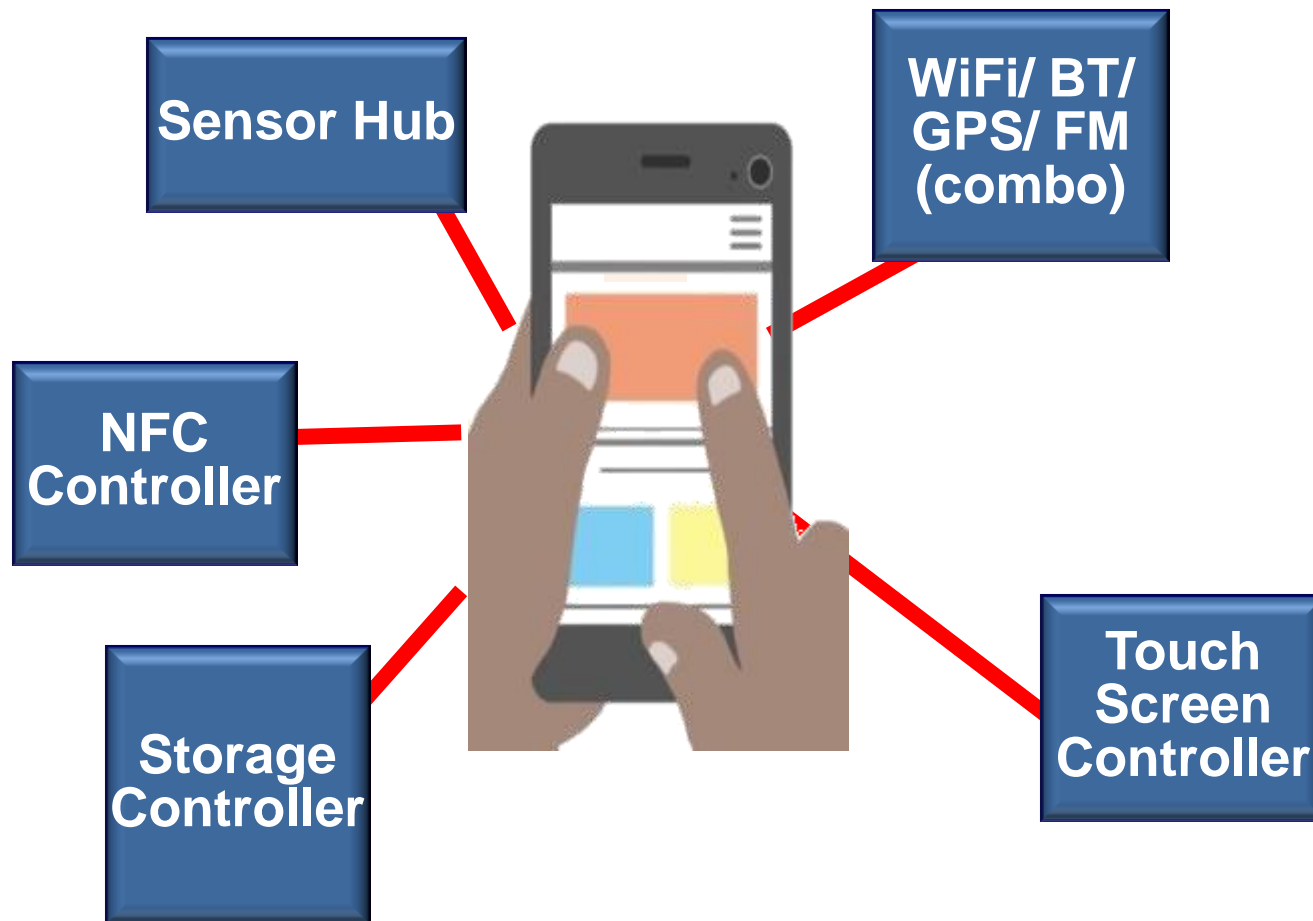
**Contactless payment
(NFC)**



Andes Embedded in Smart Phones



1 in 5 Smart Phones are with Andes Embedded



Andes Embedded in Consumer Devices, Cars and Datacenters



Switch:
MXIC Flash Ctrl



Echo Dot2:
Mediatek WiFi IoT



Bike Sharing:
GPS Ctrl



X-Trail:
ADAS Ctrl



- ❖ In leading machine learning computers for datacenter
- ❖ In tier-one switch routers for datacenter

- ❖ Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

New Products and Ecosystems

Product Lines



- ◆ New A-series Cores released in Andes Embedded Forum 2018

A N D E S



Andes RISC-V Product Overview



Best extensions to RISC-V

AndeStar™ Architecture V5



Highly optimized
design with
leading PPA

AndeCore™
Processors



Handy peripheral
IPs to speed up
SoC construction



AndeShape™ Platforms

AndeSight™
Tools



Professional IDE
with high code
quality



Extensive SW stacks
from bare metal,
RTOS to Linux

AndeSoft™ Stacks

V5 AndesCore™ Processors

N22

N25F/NX25F/D25F

A25/AX25

A25MP/AX25MP

AndesCore™ RISC-V Families



Cache-Coherent
Multicores

A25MP
1/2/4 A25, L2\$,
L1/IO coherence

AX25MP
1/2/4 AX25, L2\$,
L1/IO Coherence

Linux
with FPU/DSP

A25
N25F, MMU, DSP

AX25
NX25F, MMU, DSP

Fast/Compact
with FPU/DSP

N25F/D25F
V5/32b, FPU, PMP,
DSP (D25F)

NX25F
V5/64b, FPU, PMP

Slim and
Efficient

N22
V5[e]/32b, 32/16
GPR

5-stage, ACE, > 1.2 GHz*

LM/Caches, Branch Pred, Vec. Intpt

2-stage,
700 MHz*

* 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

Bring Andes Strength to RISC-V Core Family



- **Architecture beyond the kernel for diversified requirements**
- **Efficient processor pipeline for leading PPA**
- **Platform IP support to help speed up SoC construction**
- **AndeSight IDE, and compiler/library optimizations**
- **RTOS and Linux support, and middleware (such as IoT stacks)**
- **Commercial-grade verification for all products**
- **Mass production experience with high quality deliverables**
- **Professional supporting infrastructure**

V5 AndesCores: 25-series



❖ N25F: 32-bit, NX25F: 64-bit

- From scratch for the best PPA
- Very configurable

❖ AndeStar V5 ISA

❖ 5-stage pipeline

❖ Configurable multiplier

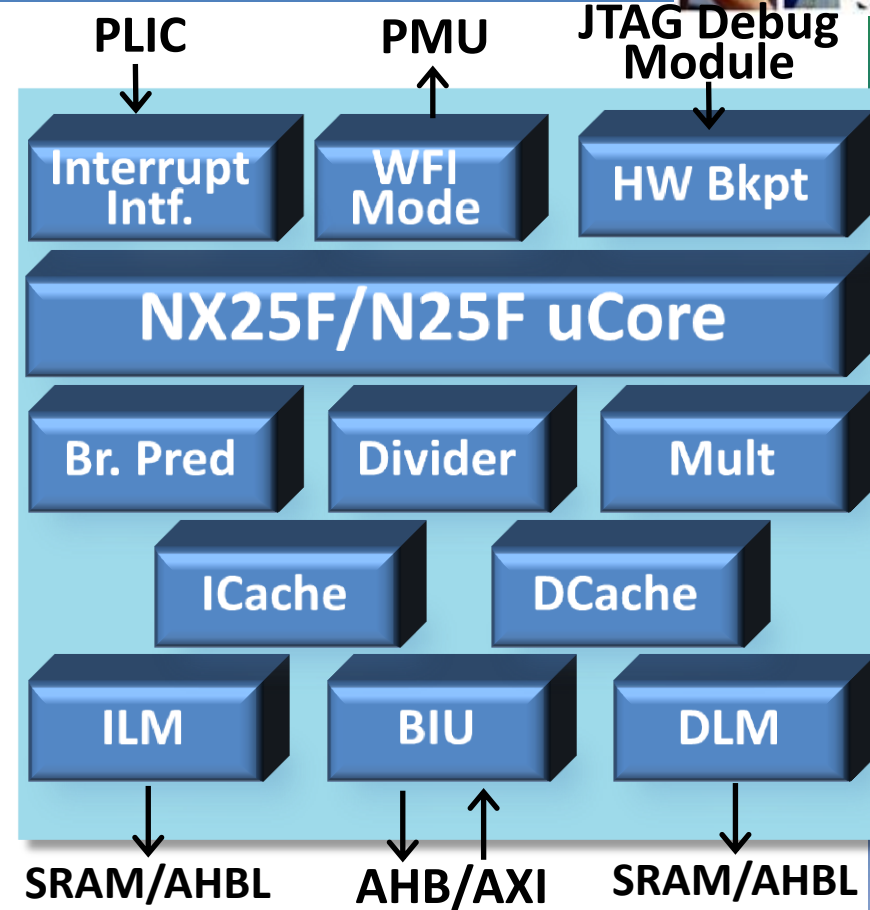
❖ Optional branch prediction

❖ Flexible memory subsystem

- I/D Local Memory (LM): to 16MB
- I/D caches: up to 64KB, 4-way
- Optional parity or ECC
- Hit-under-miss caches
- load/store: unaligned accesses

❖ N25F sample configurations @TSMC 28HPC+ RVT:

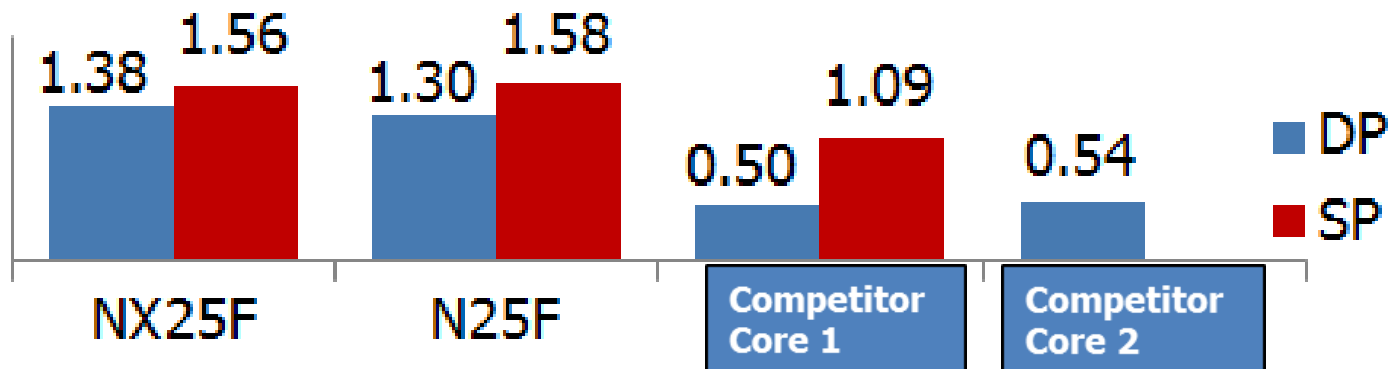
- Small config: 37K gates, 1.0 GHz (worst case, w/o caches)
- Large config: 136K gates, 1.2GHz (worst case, w/ caches)
- **Best-in-class Coremark: 3.58/MHz**



V5 AndesCores: 25-series



- ❖ **Fast-n-small for control tasks in AR/VR, networking, storage, AI**
- ❖ **N25F/NX25F: +FPU**
 - $+$, $-$, \times , $\underline{x+}$, $\underline{x-}$: pipelined 4 cycles
 - \div , $\sqrt{}$: run in the background
 - ◆ 15 for SP, 29 for DP
- ❖ **A25/AX25: +FP +Linux**
 - Support RISC-V MMU and S-mode
 - 4 or 8-entry ITLB and DTLB
 - 4-way 32~128-entry Shared-TLB
- ❖ **Whetstone/MHz:**



V5 AndesCores: 22-series



❖ AndeStar V5 or V5e ISA

- RV32-IMC or RV32-EMC
- Plus Andes extension

❖ 2-stage pipeline with AHB-lite main bus

❖ Rich baseline options:

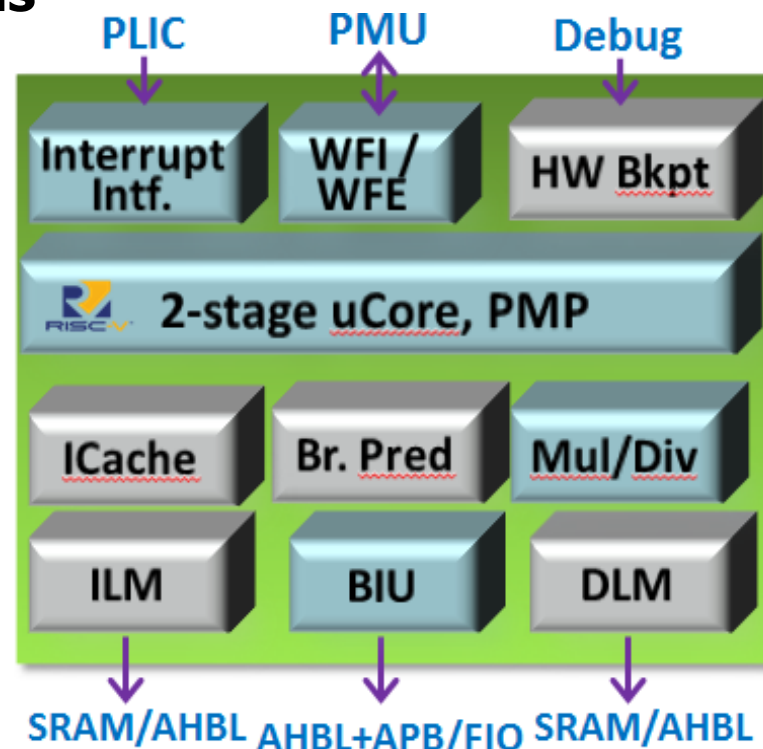
- I/D Local Memory (1KB~512MB), I cache
- Fast or small multiplier, branch predictions
- Up to 16-entry PMP, StackSafe
- M-mode, or M+U-mode
- APB private peripheral port, fast IO port
- WFI, WFE, and PowerBrake
- Vectored and preemptive interrupt controller

❖ 28nm PPA:

- **700 MHz** (worst case)
- **16K gates** (minimal)

❖ Best per-MHz performance:

- **1.8 DMIPS** (no inline)
- **3.95 Coremark**



A(X)25MP Cache-Coherent Multicore



❖ 1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs

- RV-GCP ISA, supporting SMP Linux
- With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V

❖ Hardware Multicore Cache Coherence

- Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
- Support I/O coherence without data caches

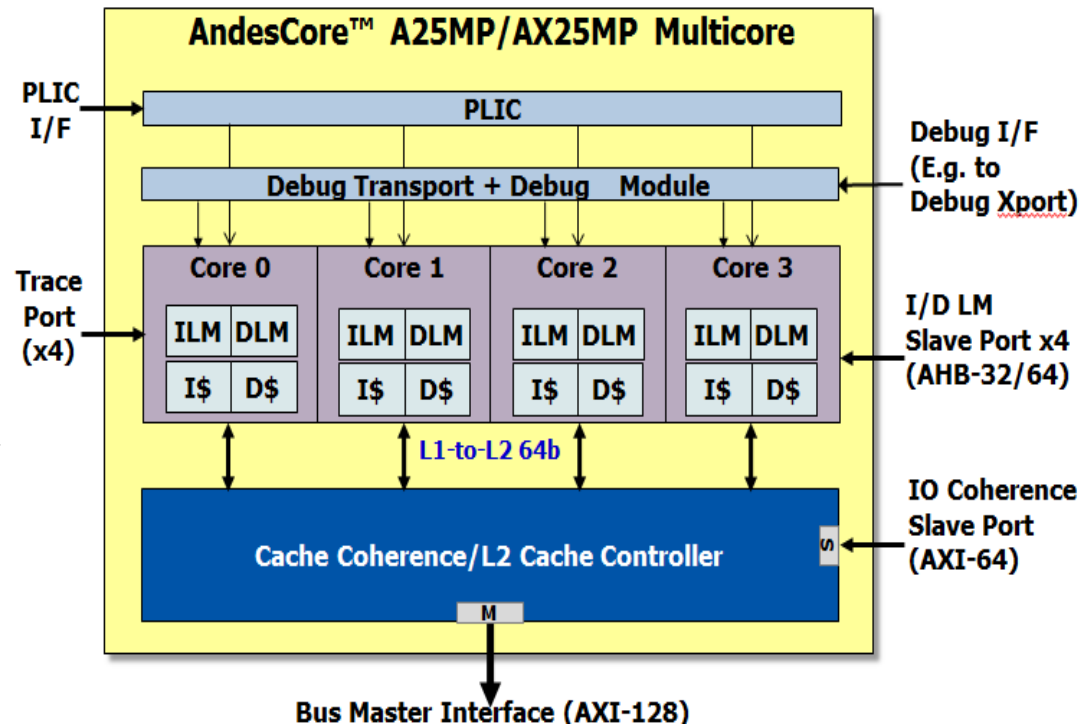
❖ Level-2 Cache Controller

- 0/128/256K...2MB, 32-byte line, 16-way
- ECC, SECDED support

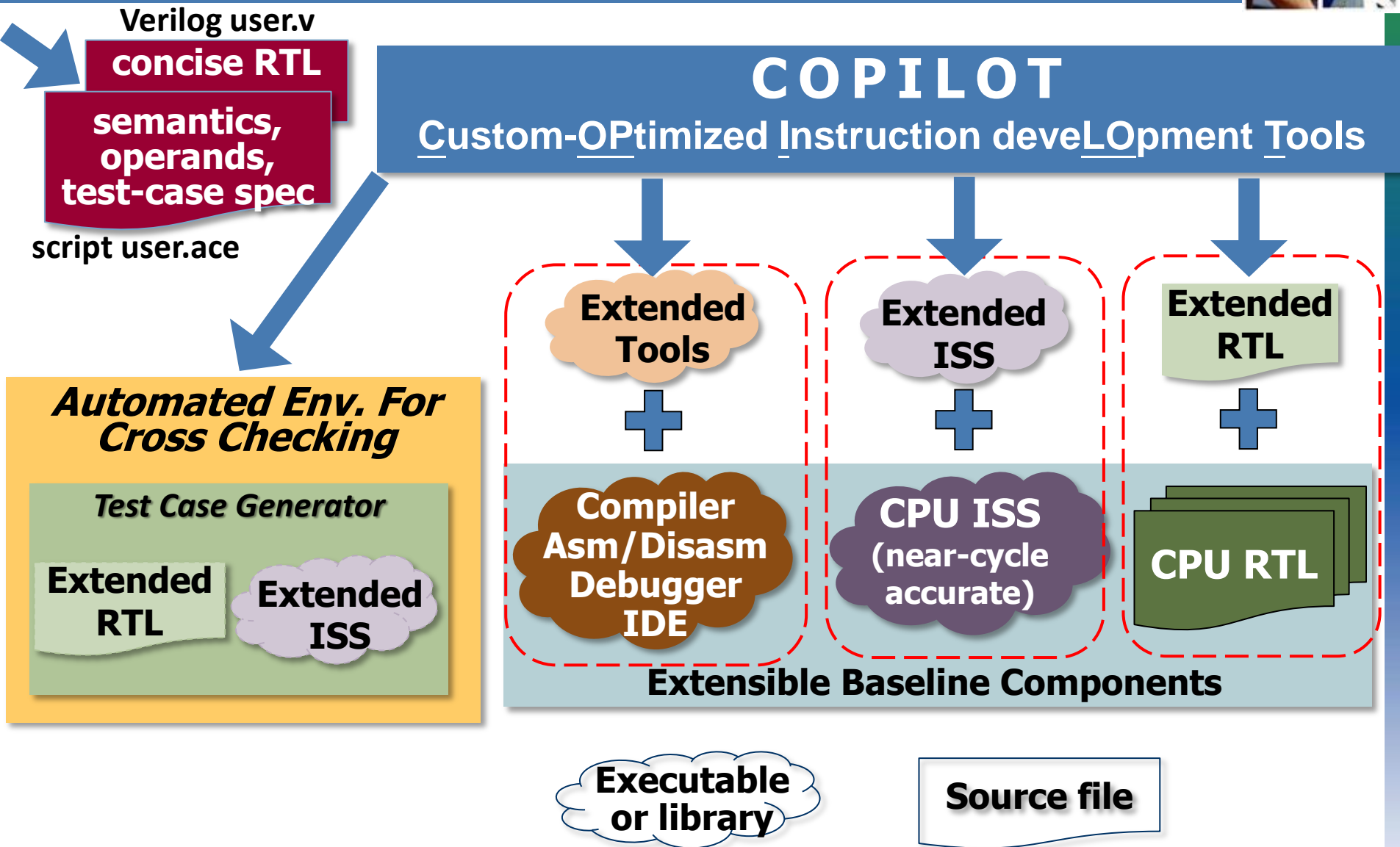
❖ Bus Interfaces

- AXI bus master interface
- Local memory slave port, for each A25/AX25 CPU
- I/O coherence slave port
- MP subsystem vs. bus interface synchronous N:1 clock ratio

❖ Platform Level Interrupt, Debug and Trace Support



ACE: Andes Custom Extension



Aggressive in RISC-V Community



Foundation Task Groups (partial list)



- ❖ **Contributing hardware architecture extensions**
 - Chair of the P-extension (Packed SIMD/DSP) Task Group
 - Co-chair of Fast Interrupts Task Group
 - Closely reviewing activities of other Task Groups

Andes Helps Strengthen RISC-V Ecosystem



- ▶ **More choices for customers are good**
- ▶ **Andes works closely with partners to grow RISC-V ecosystem**




RISC-V Software Ecosystem: GNU Toolchain



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bluespec




 **Zurich**
June 2018

Palmer Dabbelt
RISC-V Software State of the Union

C Compilers



- GNU-based toolchain is stable
 - Embedded since August, 2017
 - Linux since February, 2018
- LLVM is still experimental

GNU Toolchains and LLVM

Bootloaders for UNIX-Class Systems

- **Berkeley Boot Loader (BBL)**
 - Designed to boot university test chips
- **OpenSBI**
 - Clean implementation of SBI and early boot
- **u-boot**
 - Standard bootloader for embedded Linux systems
- **Coreboot**
 - First bootloader to add RISC-V support

Linux Kernel

- Core RISC-V architecture support merged in early 2018
 - Runs on QEMU and HiFive Unleashed
- Most HiFive Unleashed drivers are posted for the next MW
- Upstream device tree bindings also posted for the next MW
 - Ready to begin integrating SOCs and boards
- BPF JIT was recently merged
- NOMMU port posted to the mailing list yesterday

Linux

- ❖ **GCC, binutils:** May, 2017
- ❖ **Newlib:** Aug, 2017
- ❖ **Glibc (rv64i):** Feb, 2018
- ❖ **GDB:** Mar, 2018
- ❖ **OpenOCD:** July, 2018
- ❖ **Glibc (rv32i):**
 - Submitted in July 2018 (by Andes)
 - Review in progress

RISC-V Software Ecosystem: LLVM Compilation



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TECHNOLOGY



Berkeley
UNIVERSITY OF CALIFORNIA



lowRISC
OPEN TO THE CORE

Zurich June 2018

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RISC-V Software State of the Union

C Compilers

SiFive ANDES TECHNOLOGY redhat lowRISC bluespec

bluespec

LLVM

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❖ LLVM:

- RV32IMAFDC: June, 2018
- Relaxation: May, 2018 (by Andes)
- 64b support: Nov, 2018
- Change status into "official" from LLVM 9: Sep, 2019 (est.)

❖ compiler-rt: Mar, 2018


❖ LLD: Aug, 2018 (by Andes)

- Initial port (relocation and TLS) in Oct. 2017
- Dynamic linking review in progress since Oct, 2017
- Missing link-time relaxation

RISC-V System Software Ecosystem: Linux






- ❖ **U-boot**: Jan, 2018 (by Andes)
- ❖ **Kernel (rv64i)**: Jan, 2018
- ❖ **Key utilities**: (by Andes)
 - Perf: Feb, 2018
 - Kernel Module: May, 2018
 - Ftrace: May, 2018
- ❖ **Kernel (rv32i)**: Jun, 2018 (by Andes)
- ❖ **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)



 **Zurich**
June 2018

Palmer Dabbelt



RISC-V Software State of the Union

C Compilers

bluespec

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 - Code generation for RV32 and RV64

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Andes Position in RISC-V



Complete product portfolio

Reliable RISC-V core IP provider

Extreme low power consumption, high computing efficiency

World's leading Customer-Extension Capable RISC-V Core



Two Ecosystems: Andes and Knect.me



Knect.me Ecosystem



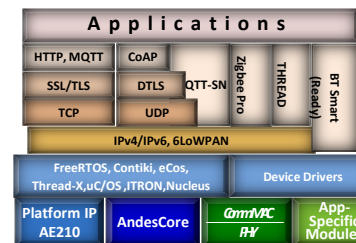
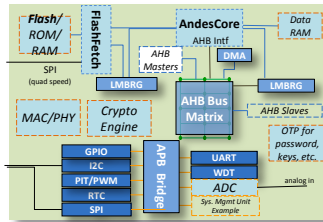
- ❖ **Built up Ecosystem knect.me to help IoT Developing**
 - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products

- ❖ **Includes:**

- SoC IP Platforms
- Software Stack
- Development Boards
- Development Tools

- ❖ **To Form a IoT League**

- to **knect** chip vendors, partners, application developers, system vendors



ectime™



FreeStart Program



❖ FreeStart Evaluation Program (FSEP)

- For all RISC-V enthusiasts and educator/researcher
- Good for N22 evaluation and research project
- Fixed-Configuration N22 RTL
- Sign simple evaluation agreement directly on website

❖ Support Package (FSSP)

- For all
- \$20K for 1st year, including
 - 1 year e-service
 - FreeStart AE250 RTL
 - Corvette F1 FPGA board

❖ FreeStart Mass-production Program (FSMP)

- For industrial and academy mass production
- Full-configuration N22
- License fee: \$0; only running royalty is required when mass production

2019 Event Promotion



RISC-V CON
Silicon Valley

RISC-V CON
Beijing

RISC-V CON
Shanghai

RISC-V CON
Hsinchu

RISC-V CON
Shenzhen

RISC-V CON series
RISC-V Roadshow & Workshop Series
TSMC symposium & OIP series

Concluding Remarks

Andes: Trusted Computing Expert



- ❖ Andes stretched out for more opportunities in 1H'19 thru the launch of x6 new RISC-V cores, custom design service and FreeStart program.
- ❖ Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.
- ❖ Andes has successively signed >15 contracts with design service houses to authorize ASIC design to embed RISC-V core (i.e. Andes RISC-V EasyStart Program) for creating a "win-win" situation.
- ❖ Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry



Andes Core

www.andestech.com

Q&A