

晶心科技股份有限公司 2019年第一季法人說明會

Driving Innovations™



股票代號: 6533
2019/05/14

投資安全聲明



除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

- 公司簡介
- 營運成果
- 產品應用
- 新產品及生態系統
- 近期獲獎
- 總結

公司簡介

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數達170人；80%為工程師。
- EETimes評為全球60家最具潛力半導體新創公司。(2012)
- 獲得TSMC 2015年新的 IP OIP Award。
- RISC-V基金會創始成員。(2016)
- 中国电子报 2018 MCU 設計創新獎。



晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

晶心利基

- 智能及環保之電子設備
- 雲端應用, 人工智慧及物聯網

營運成果



Driving Innovations™

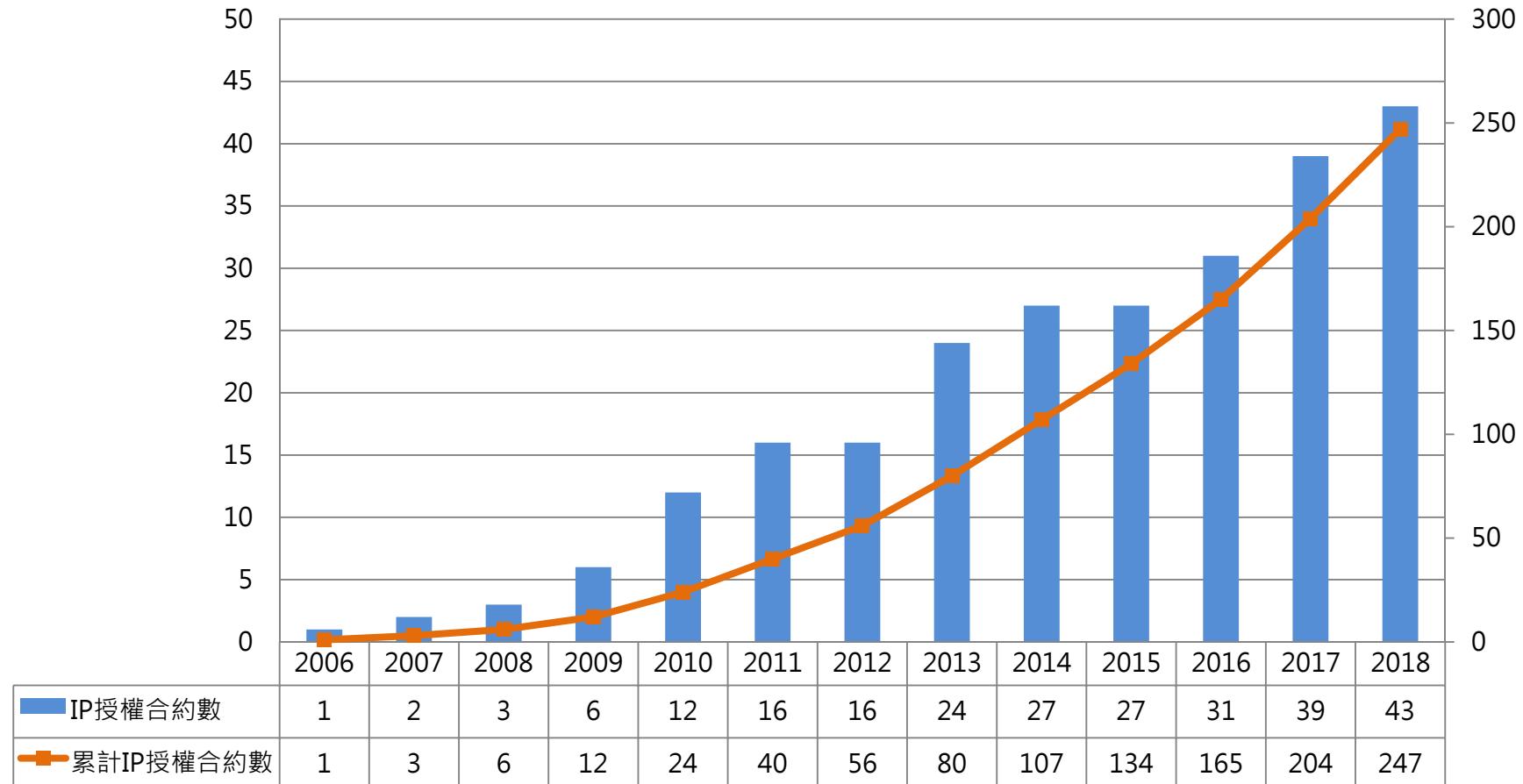
重要里程碑



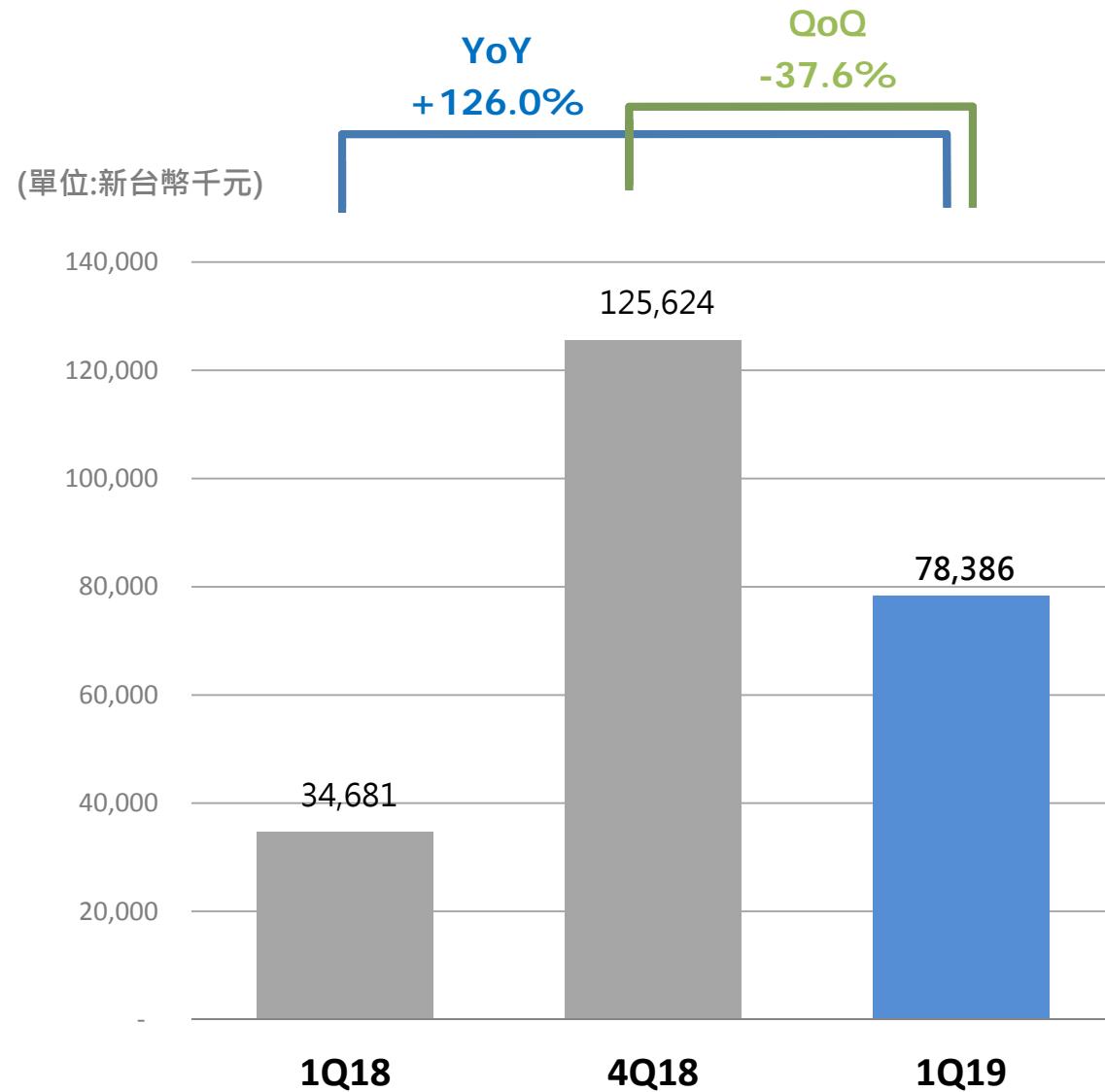
- 全球授權客戶超過 **160家**
 - 台灣, 大陸, 韓國, 日本, 歐洲, 及美國
 - 授權合約超過**250份**
- AndeSight™ IDE:
 - 安裝次數超過 **14,000 次**
- 生態系統:
 - 合作夥伴超過 **140 家**
- 嵌入晶心處理器之系統晶片累計出貨量
 - 超過**36億顆**



IP 授權合約數穩健成長



2019年第一季營業收入

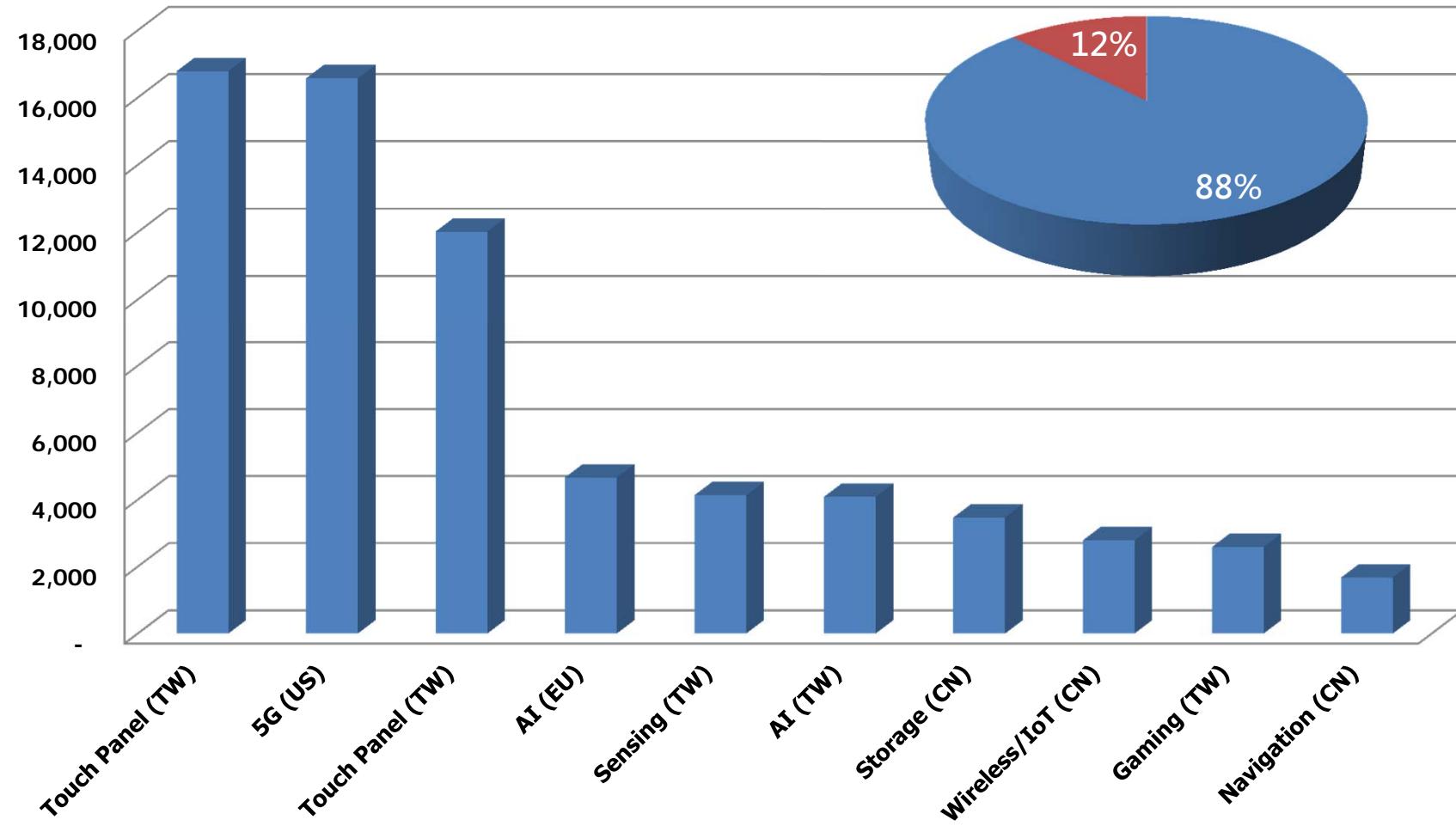


2019第一季前十大客戶之應用分析



單位: 新台幣千元

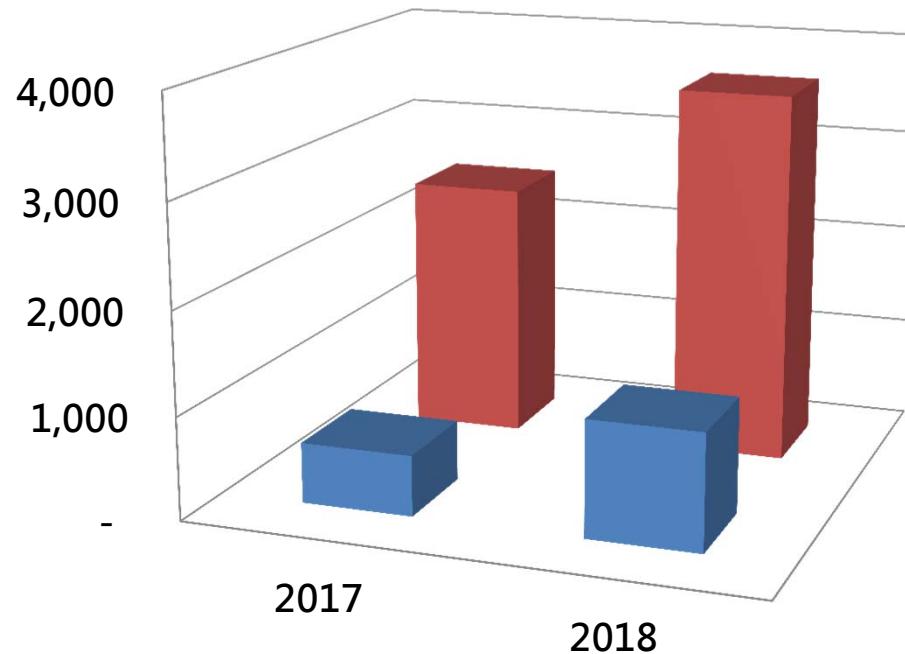
前十大客戶貢獻88%的營收



年度及累積 客戶出貨量

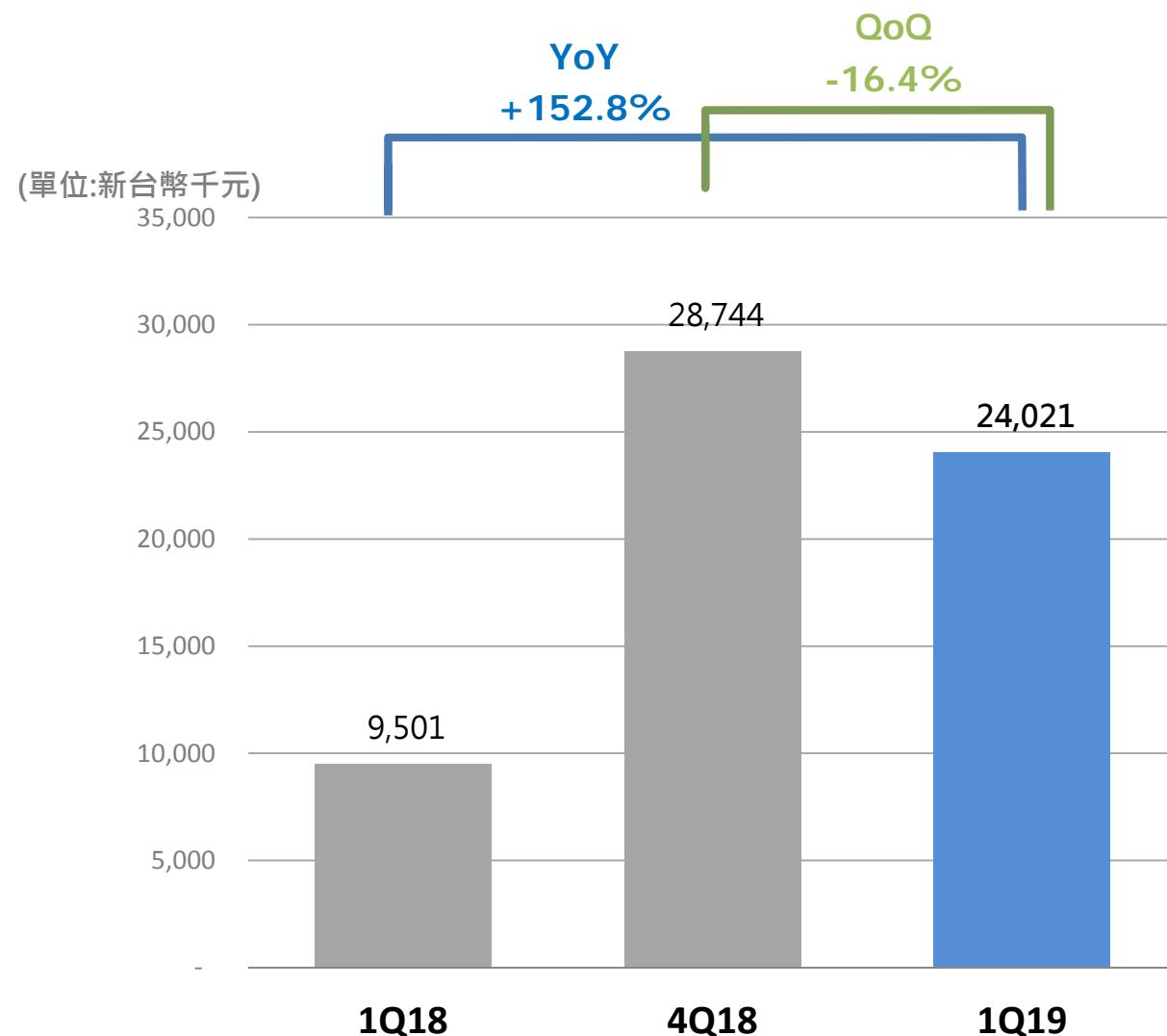


(單位:百萬 顆)



	2017	2018
■ 年度出貨量	590	1,132
■ 累計出貨量	2,500	3,632

2019年第一季權利金收入

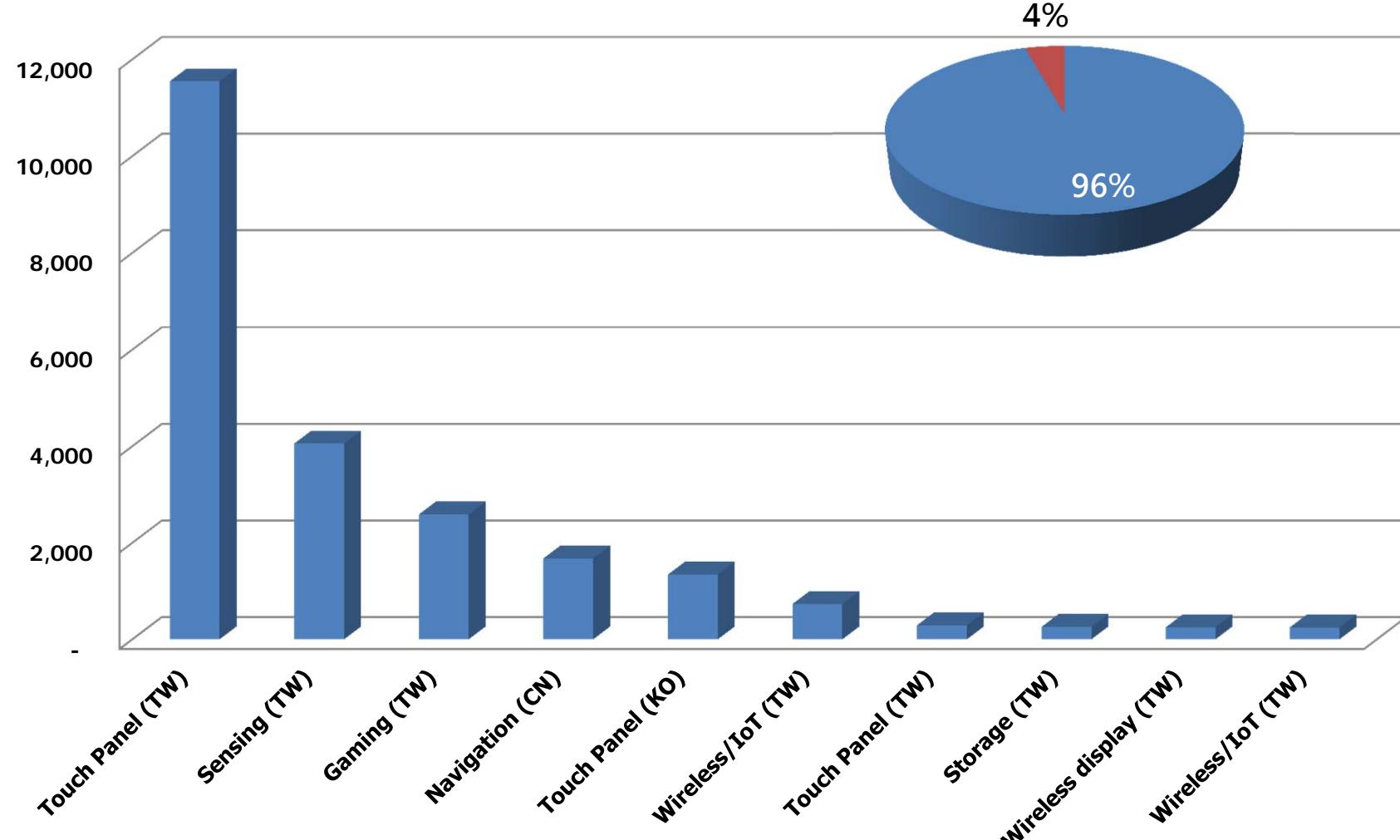


2019年第一季權利金應用分析



(單位:新台幣千元)

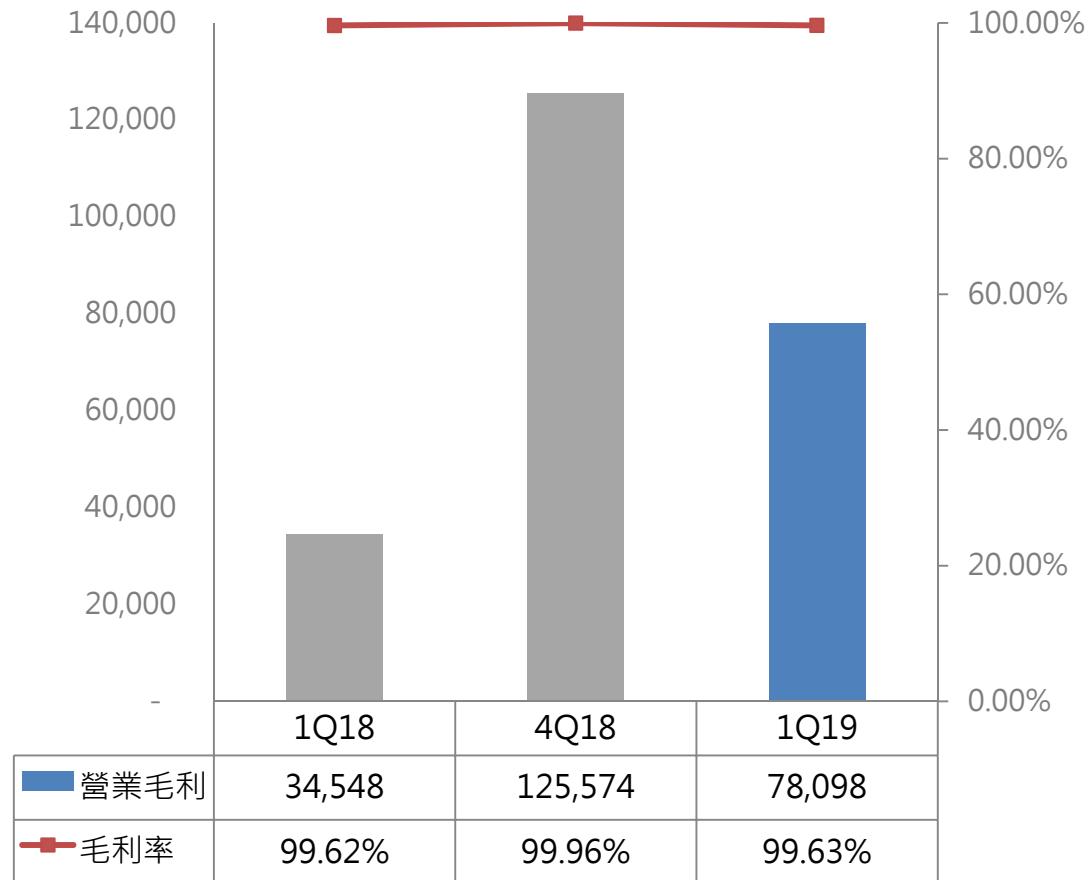
前十大權利金客戶貢獻比率 96%



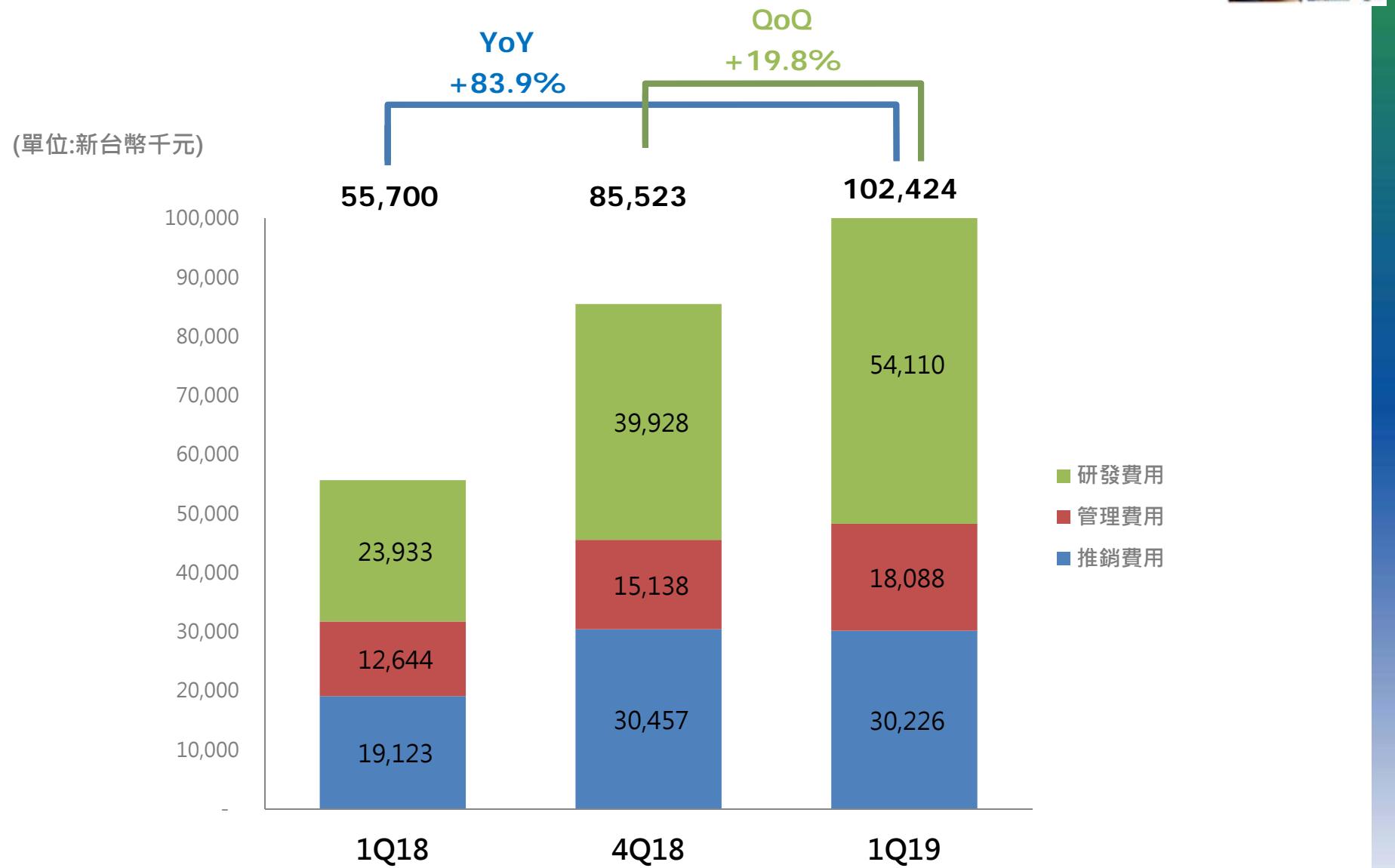
營業毛利與毛利率



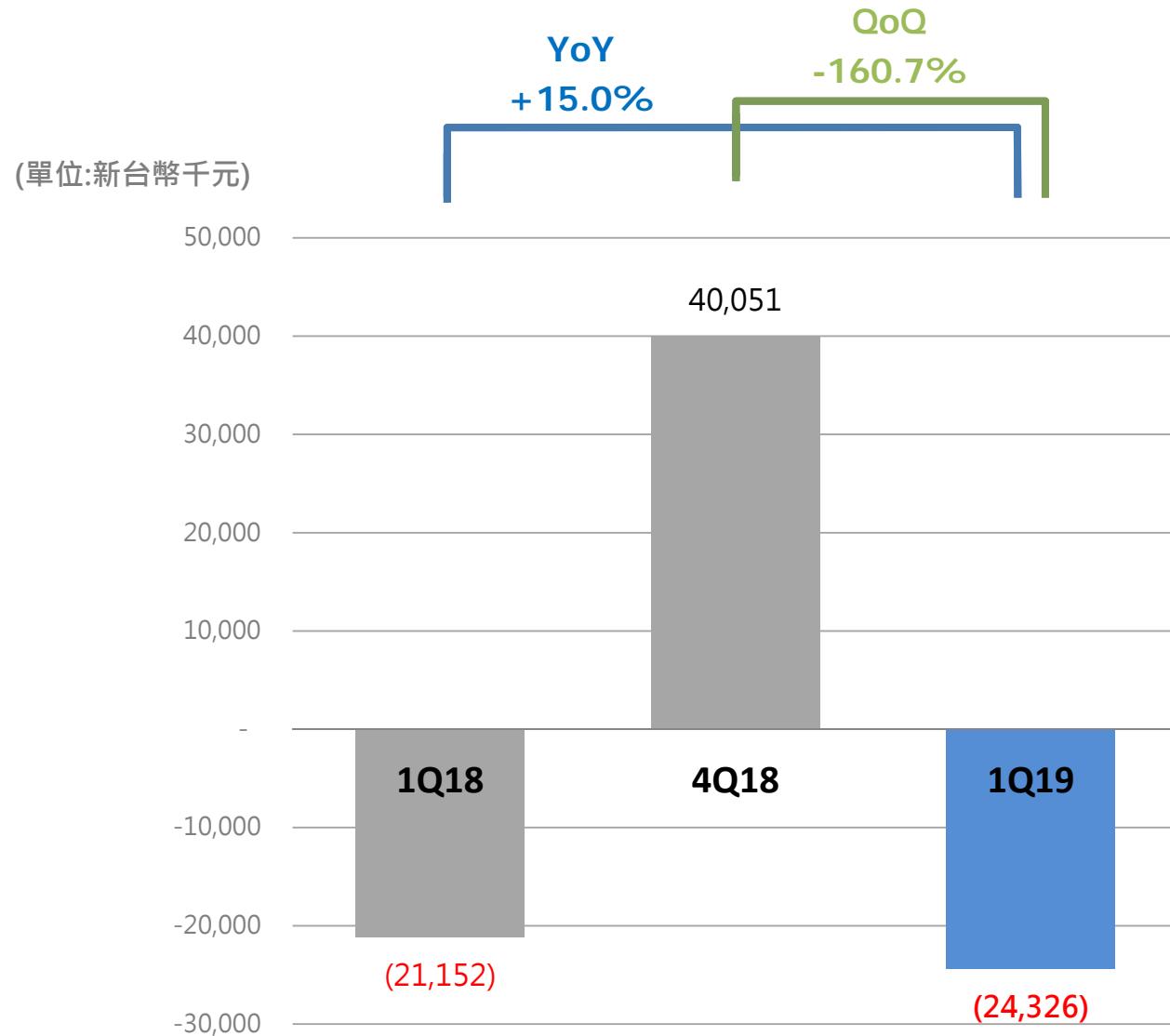
(單位:新台幣千元)



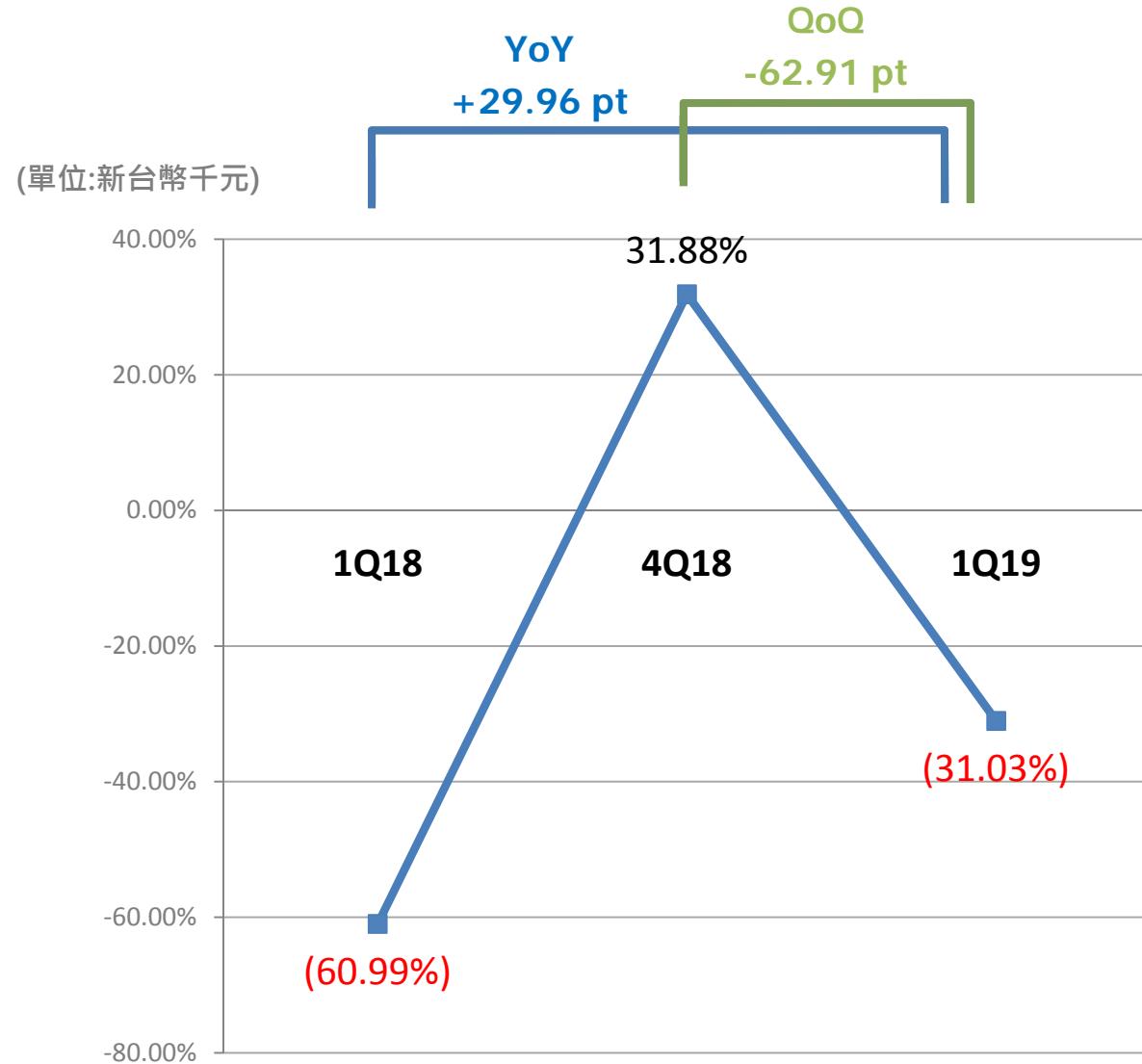
營業費用



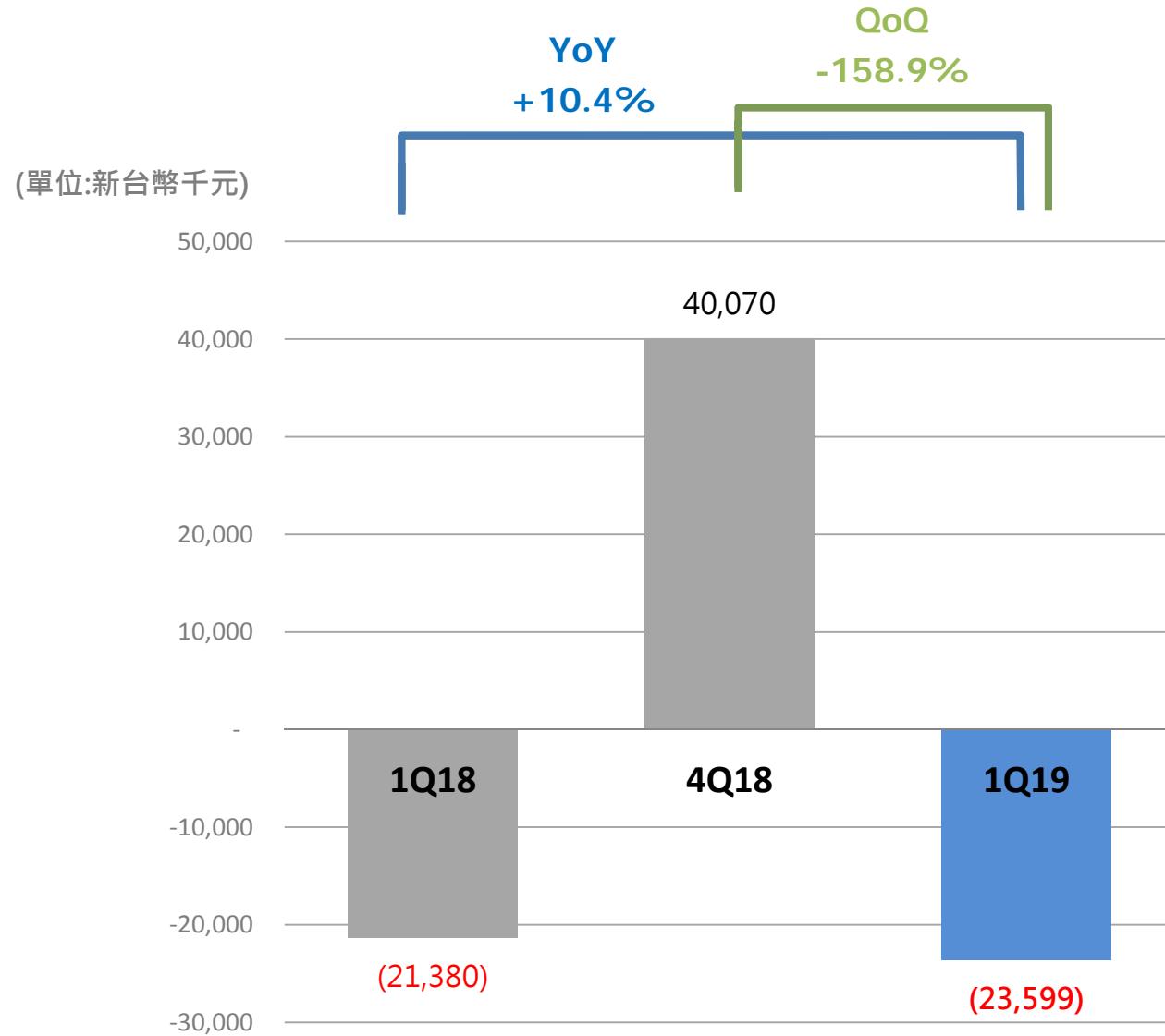
營業利益(損失)



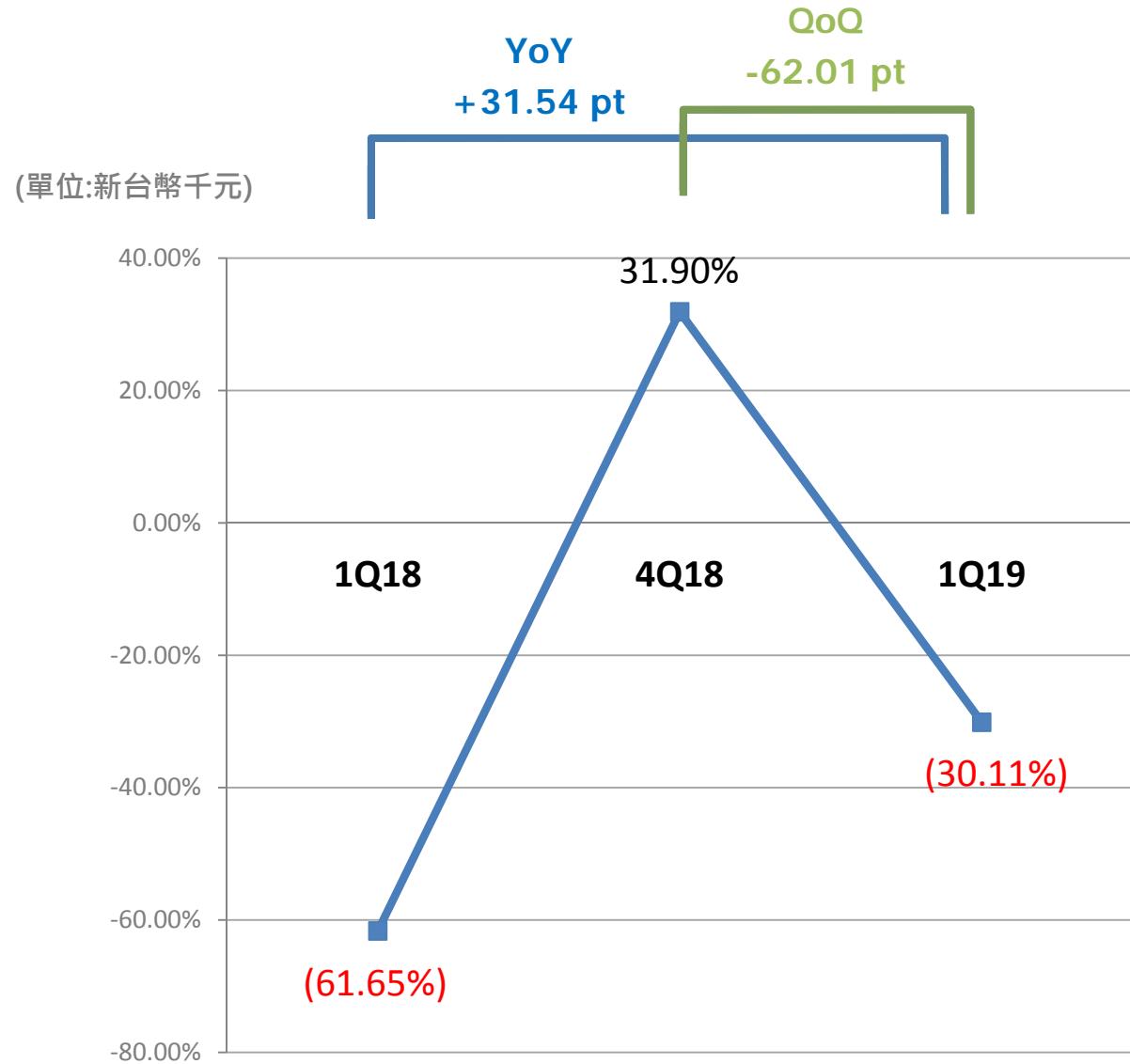
營業利益率



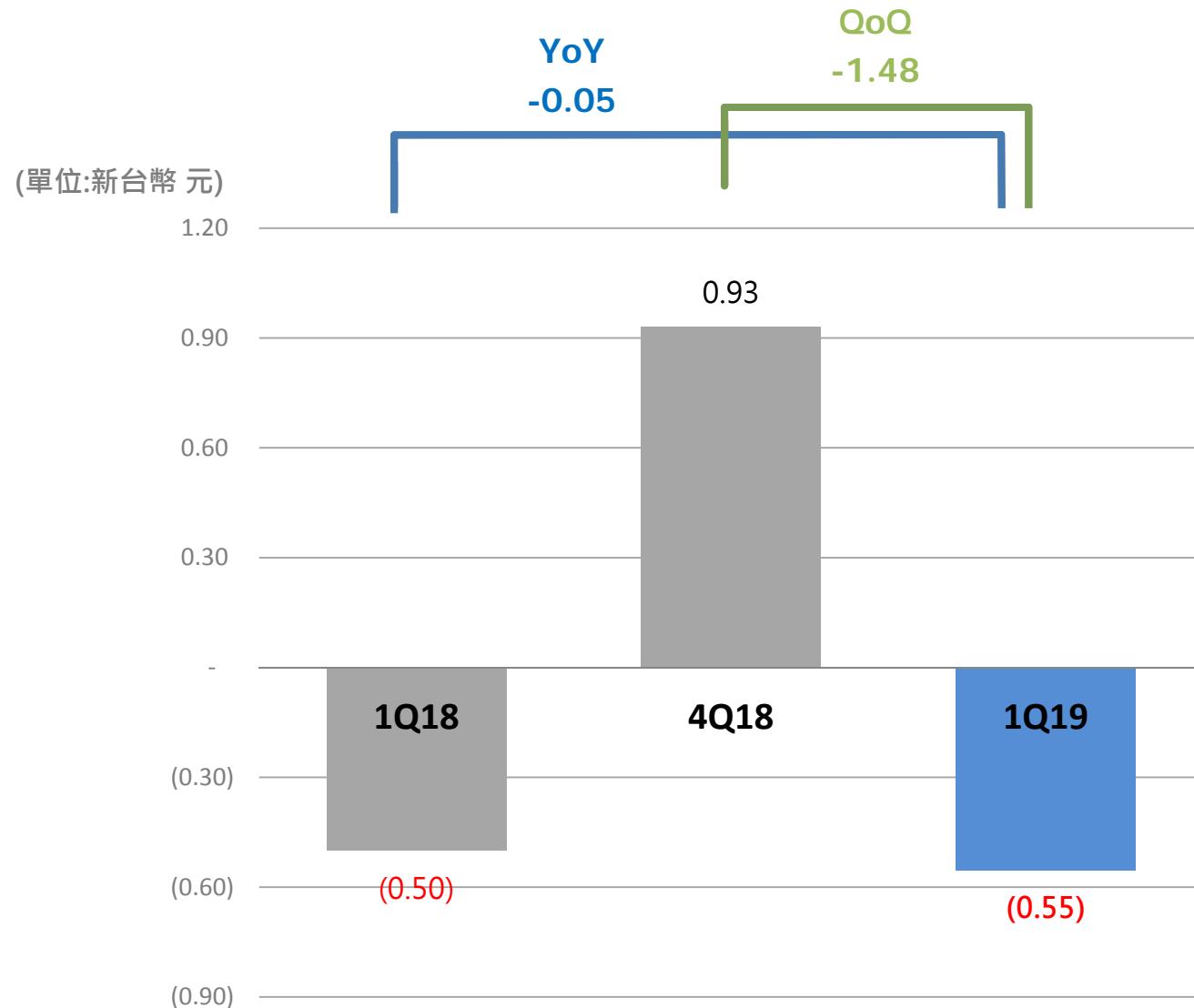
合併淨利(損)



合併淨利率



每股盈餘

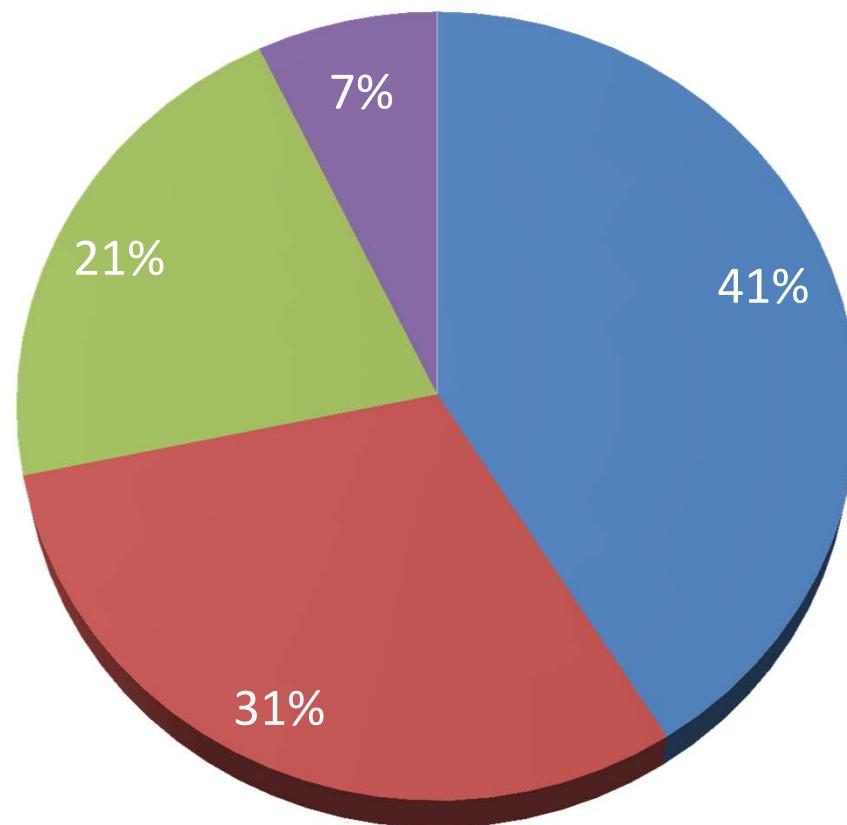


2019年第一季銷售分析-收入模式

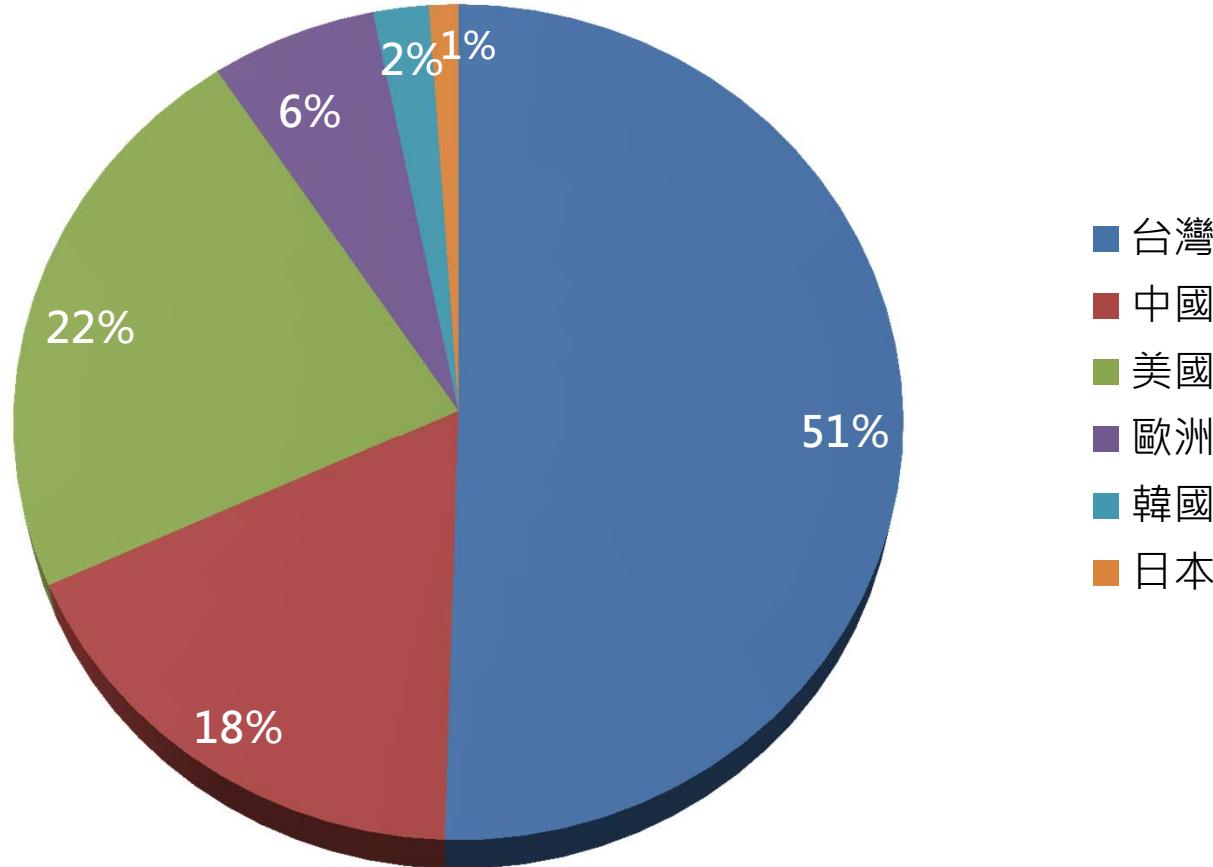


(2019年第一季新合約數: 7)

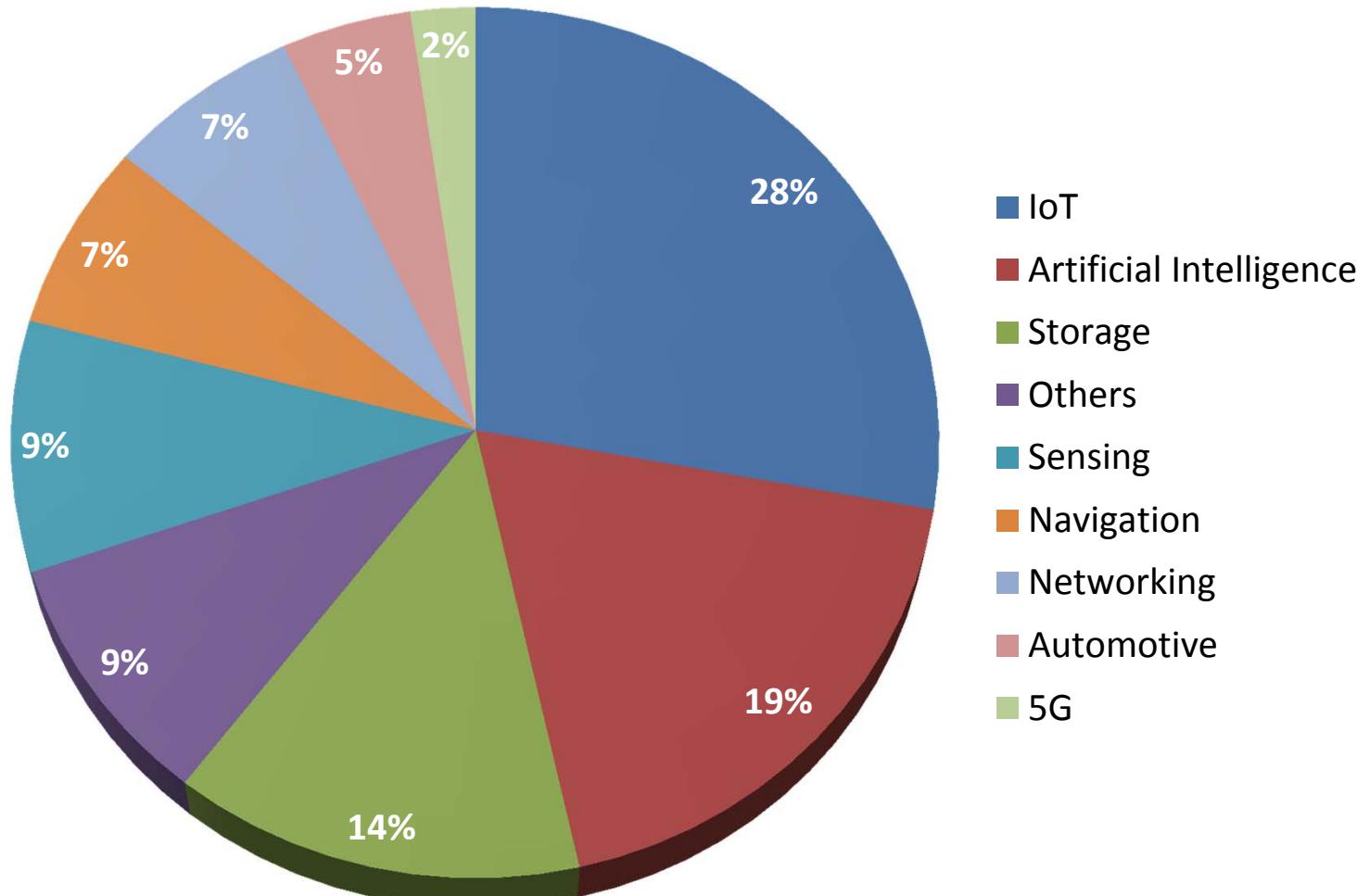
■ 矽智財授權收入 ■ 權利金收入 ■ 技術服務收入 ■ 維護服務收入及其他



2019年第一季銷售分析-地區別

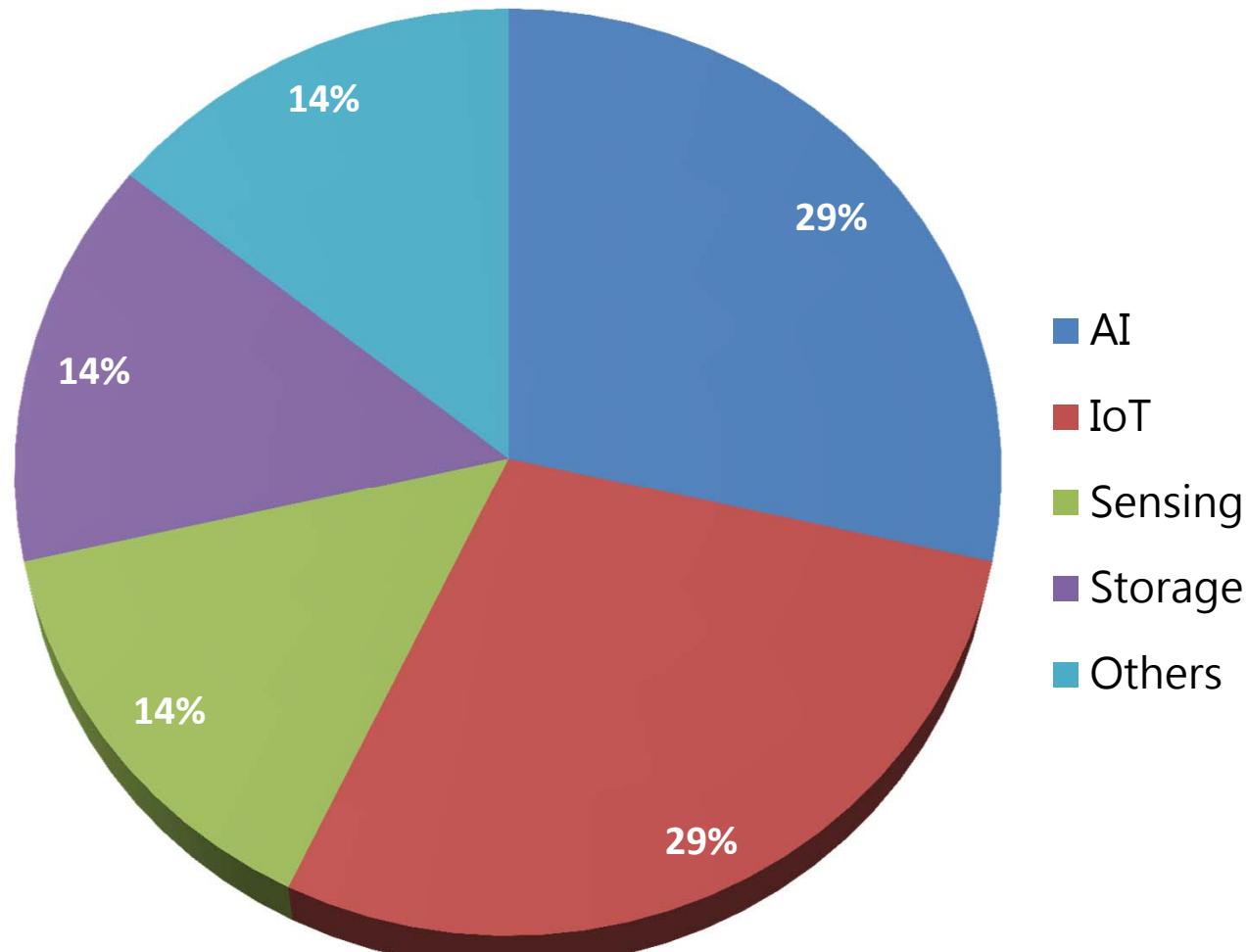


2018年度銷售分析-客戶應用



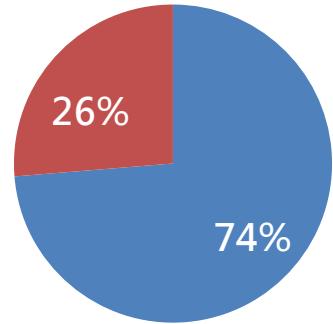
*Based on agreement number

2019年第一季銷售分析-客戶應用

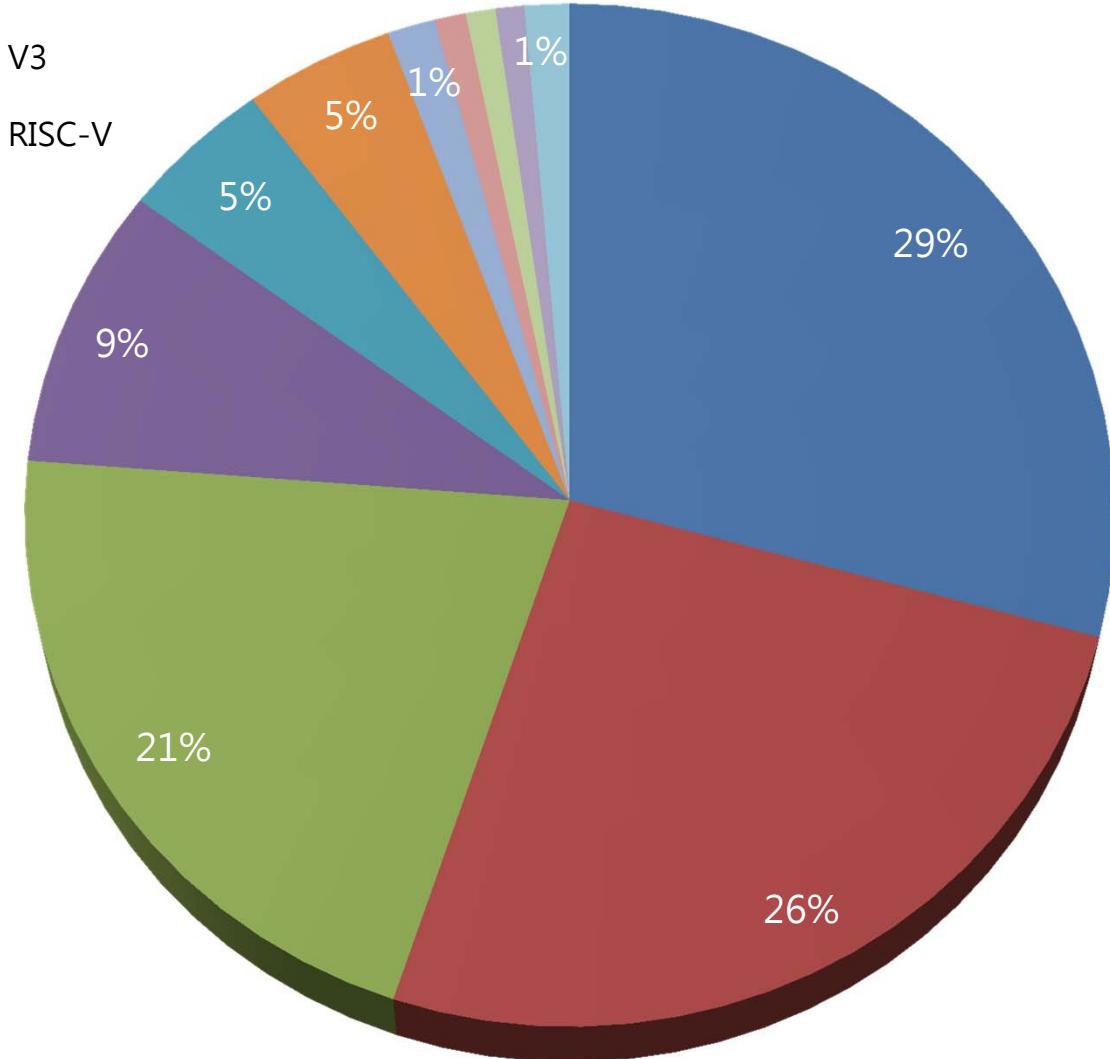


*Based on agreement number

2019年第一季銷售分析-產品別



■ V3
■ RISC-V

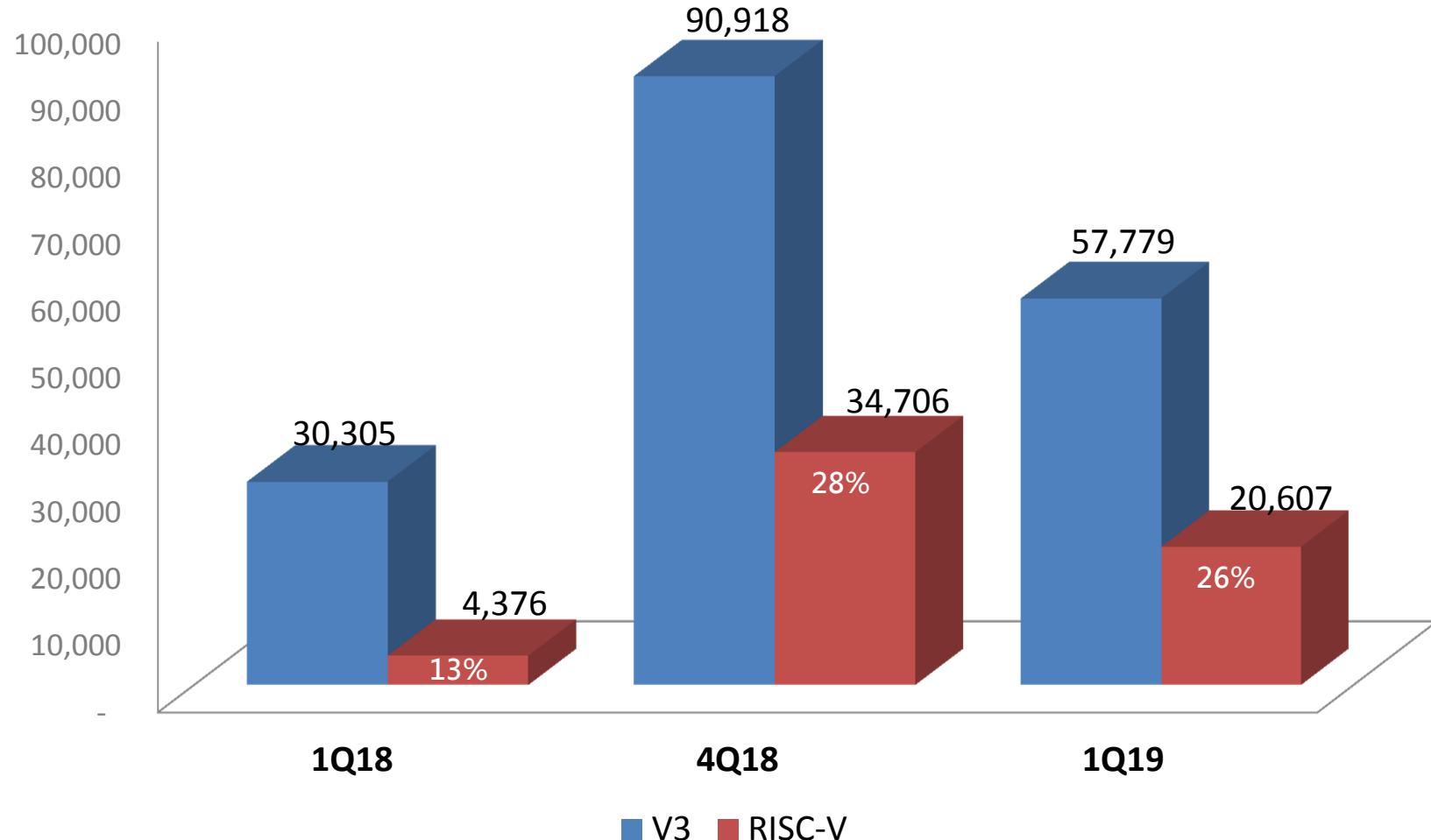


■ N8
■ N25
■ Service
■ N9
■ S8
■ D10
■ N13
■ N10
■ EVB
■ N7
■ OTHERS

2019年第一季銷售分析 - RISC-V



(單位:新台幣千元)



產品應用



Driving Innovations™

晶心概況



- ❖ A 14-year-old public CPU IP company
- ❖ >1B Andes-Embedded SoC shipped in 2018. >3.6B cumulatively.



- ❖ A founding member of the RISC-V Foundation
- ❖ A major open source maintainer/contributor
- ❖ Active involvement in standard extensions
 - Chair of P-extension (Packed DSP/SIMD) Task Group
 - Co-chair of Fast Interrupt Task Group

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports rv64i-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

GNU Toolchains

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM/EM
 - Talk yesterday afternoon
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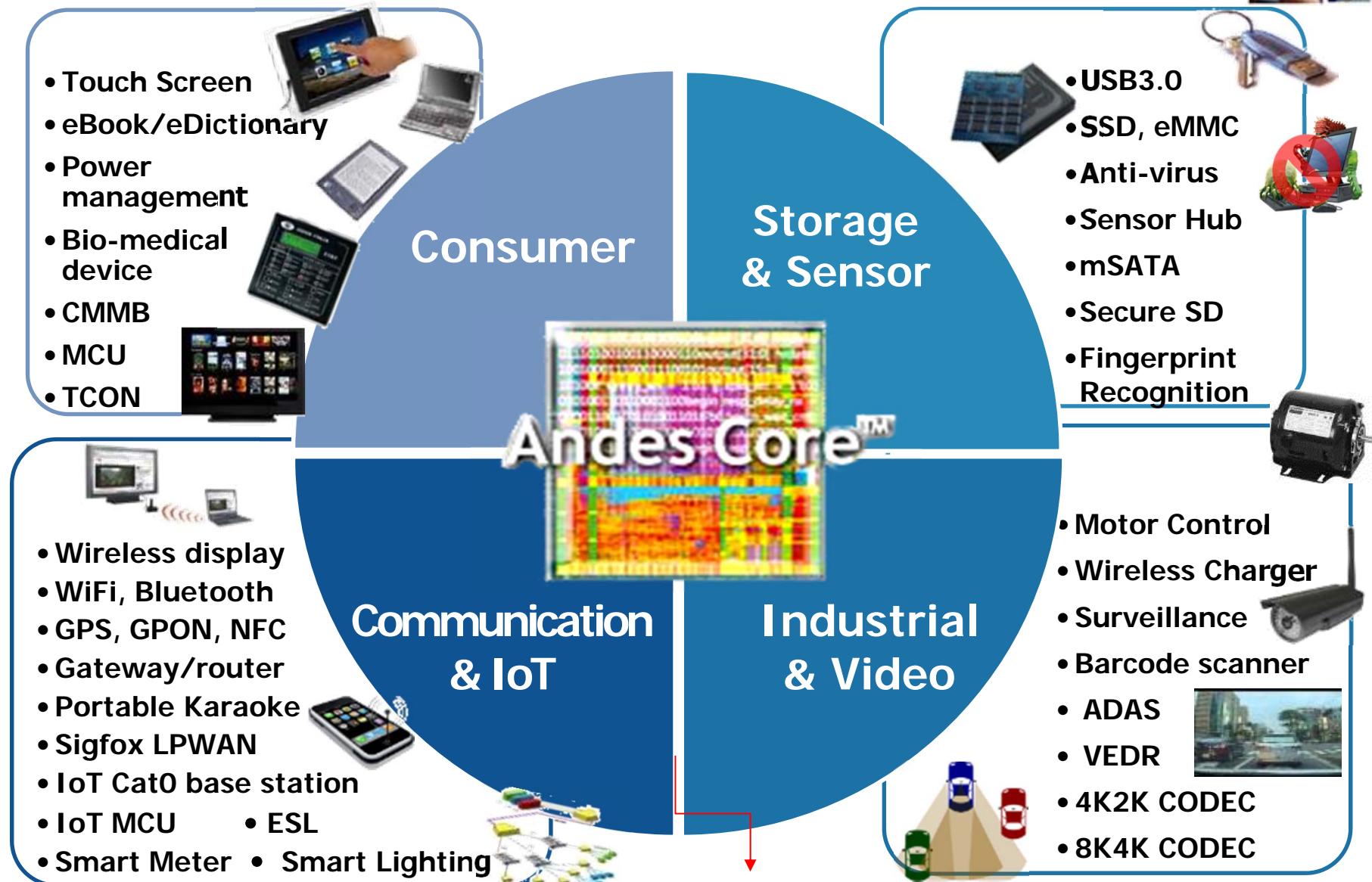
LLVM

RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64i-based systems
 - Drivers are trickling in now

Linux

豐富多樣的客戶應用



物聯網應用 - 1



Bluetooth Speaker



Healthcare device



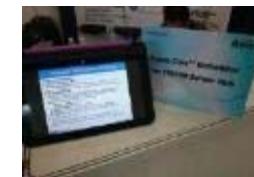
Electronic price tags



Sigfox LPWAN



Wearable device



Sensor Hub

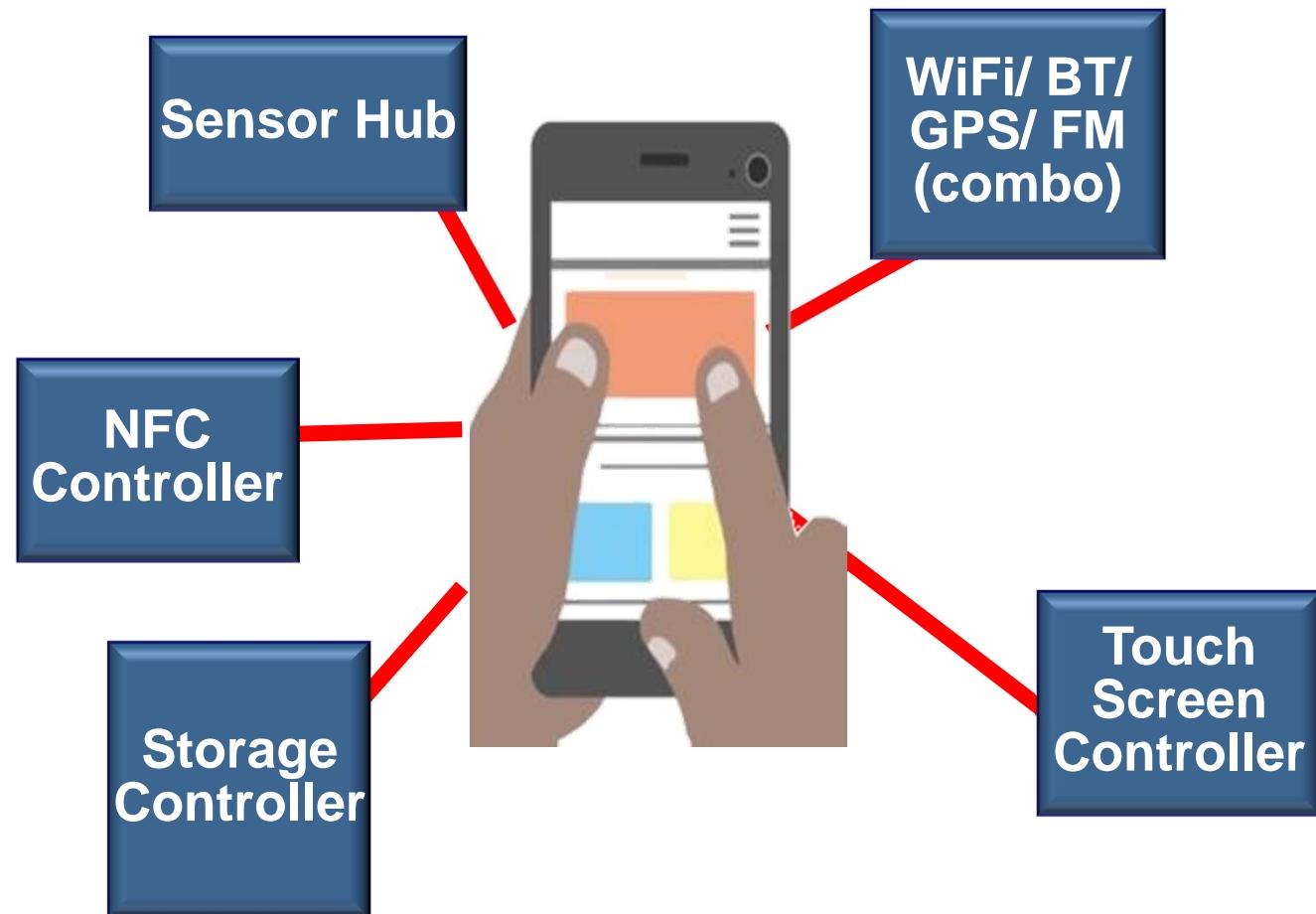
物聯網應用 - 2



晶心嵌入智能手機



1 in 5 Smart Phones are with Andes Embedded



晶心嵌入消費性裝置、車用電子 及資料處理中心



Switch:
MXIC Flash Ctlr



Echo Dot2:
Mediatek WiFi IoT



Bike Sharing:
GPS Ctrl



X-Trail:
ADAS Ctlr



- ❖ In leading machine learning computers for datacenter
- ❖ In tier-one switch routers for datacenter

- ❖ Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

新產品及生態系統

完整產品線



- ◆ New A-series Cores released in Andes Embedded Forum 2018

A N D E S



晶心 RISC-V 產品概述



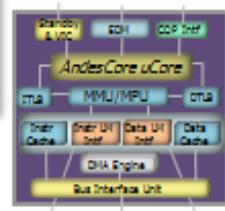
Best extensions to RISC-V

AndeStar™ Architecture V5



Highly optimized
design with
leading PPA

AndesCore™
Processors



Handy peripheral
IPs to speed up
SoC construction



AndeShape™ Platforms

AndeSight™
Tools



Professional IDE
with high code
quality

AndeSoft™ Stacks



Extensive SW stacks
from bare metal,
RTOS to Linux



V5 AndesCore™ 處理器核心

N22/D22

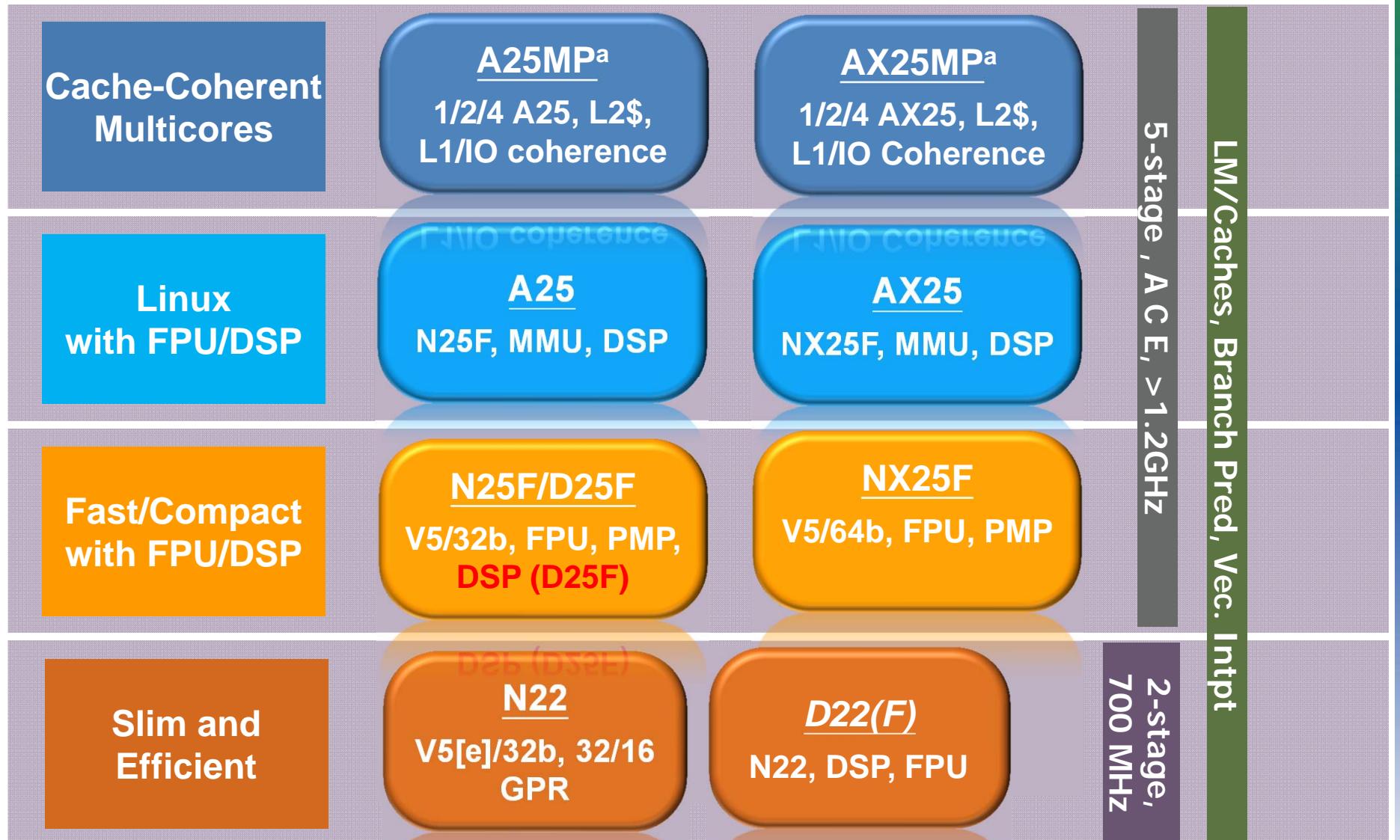
N25F/NX25F

A25/AX25

A25MP/AX25MP



最新產品路線圖



a. 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

將晶心的優勢帶進 RISC-V 處理器家族



- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure

V5 AndesCores: 25-系列



❖ N25F: 32-bit, NX25F: 64-bit

- From scratch for the best PPA
- Very configurable

❖ AndeStar V5 ISA

❖ 5-stage pipeline

❖ Configurable multiplier

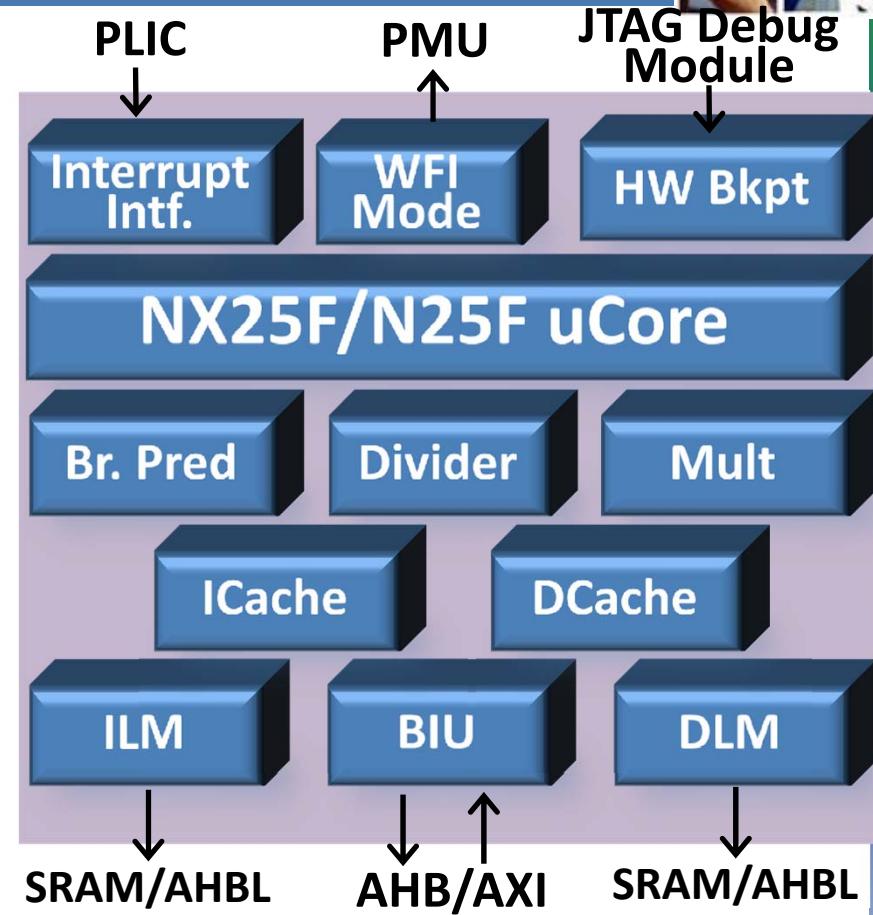
❖ Optional branch prediction

❖ Flexible memory subsystem

- I/D Local Memory (LM): to 16MB
- I/D caches: up to 64KB, 4-way
- Optional parity or ECC
- Hit-under-miss caches
- load/store: unaligned accesses

❖ N25F sample configurations @TSMC 28HPC+ RVT:

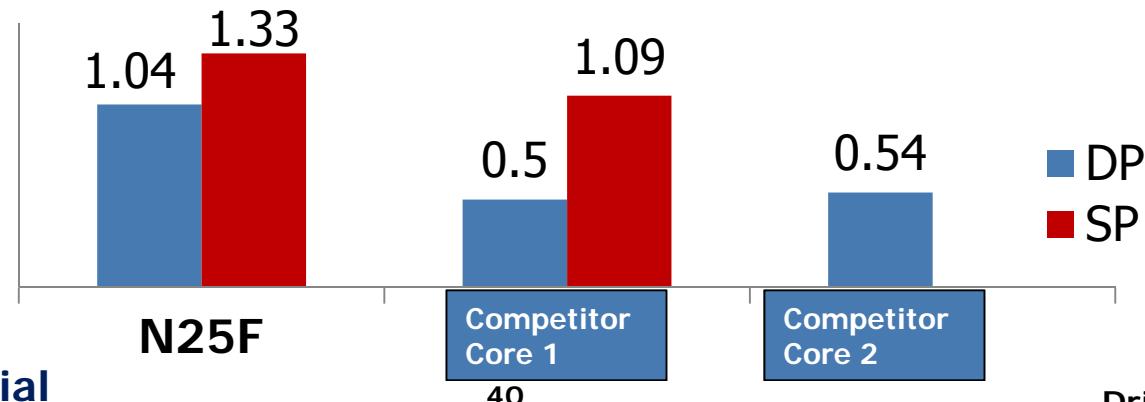
- Small config: 37K gates, 1.0 GHz (worst case)
- Large config: 130K gates, 1.2GHz (worst case)
- **Best-in-class Coremark: 3.58/MHz**



V5 AndesCores: 25-系列



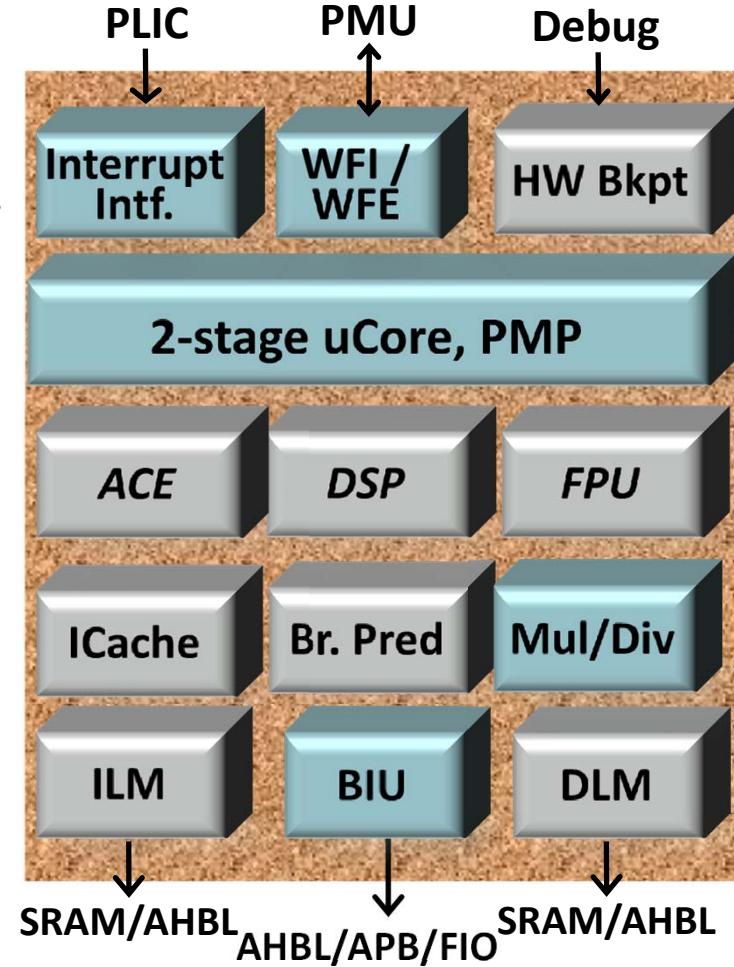
- ❖ Fast-n-small for control tasks in AR/VR, networking, storage, AI
- ❖ N25F/NX25F: +FPU
 - +, -, x, x+, x-: pipelined 4 cycles
 - ÷, √ : run in the background
 - ◆ 15 for SP, 29 for DP
 - FP load/store: support HP
- ❖ A25/AX25: +FP +Linux
 - Support RISC-V MMU and S-mode
 - 4 or 8-entry ITLB and DTLB
 - 4-way 32~128-entry Shared-TLB
- ❖ Whetstone/MHz:



V5 AndesCores: 22-系列



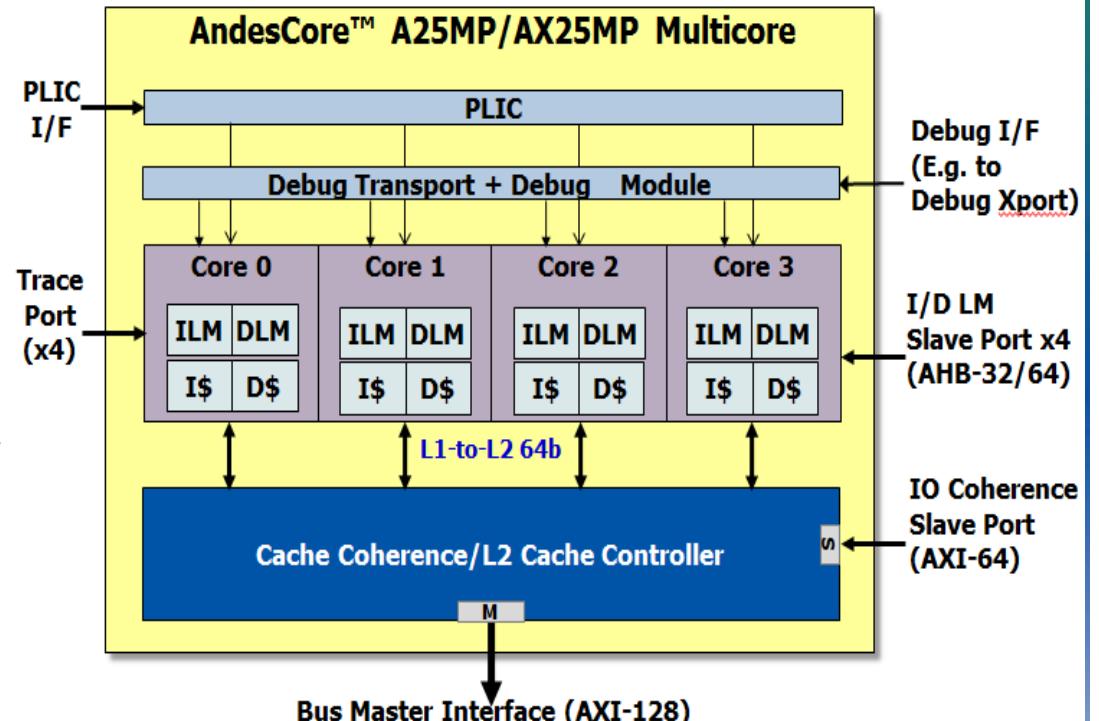
- ❖ **AndeStar V5 or V5e ISA**
 - RV32-IMC or RV32-EMC
 - Plus Andes extension
- ❖ **2-stage pipeline with AHB-lite main bus**
- ❖ **Rich baseline options:**
 - I/D Local Memory (1KB~512MB), I cache
 - Fast or small multiplier, branch predictions
 - Up to 16-entry PMP, StackSafe
 - M-mode, or M+U-mode
 - APB private peripheral port, fast IO port
 - WFI, WFE, and PowerBrake
 - Vectored and preemptive interrupt controller
- ❖ **Advanced options: ACE, DSP, FPU**
- ❖ **28nm PPA:**
 - 700 MHz (worst case)
 - <15K gates (minimal)
- ❖ **Best per-MHz performance:**
 - 1.8 DMIPS (no inline)
 - 3.95 Coremark



A(X)25MP Cache-Coherent Multicore



- ❖ 1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs
 - RV-IMACFD ISA, supporting SMP Linux
 - With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V
- ❖ Hardware Multicore Cache Coherence
 - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
 - Support I/O coherence without data caches
- ❖ Level-2 Cache Controller
 - 0/128/256K...2MB, 32-byte line, 16-way
 - ECC, SECDED support
- ❖ Bus Interfaces
 - AXI bus master interface
 - Local memory slave port, for each A25/AX25 CPU
 - I/O coherence slave port
 - MP subsystem vs. bus interface synchronous N:1 clock ratio
- ❖ Platform Level Interrupt, Debug and Trace Support





ACE: Andes Custom Extension



Verilog user.v

concise RTL

semantics,
operands,
test-case spec

script user.ace

*Automated Env. For
Cross Checking*

Test Case Generator

Extended
RTL

Extended
ISS

COPilot Custom-OPtimized Instruction deveLOpment Tools

Extended
Tools



Compiler
Asm/Disasm
Debugger
IDE

Extended
ISS



CPU ISS
(near-cycle
accurate)

Extended
RTL



CPU RTL

Extensible Baseline Components

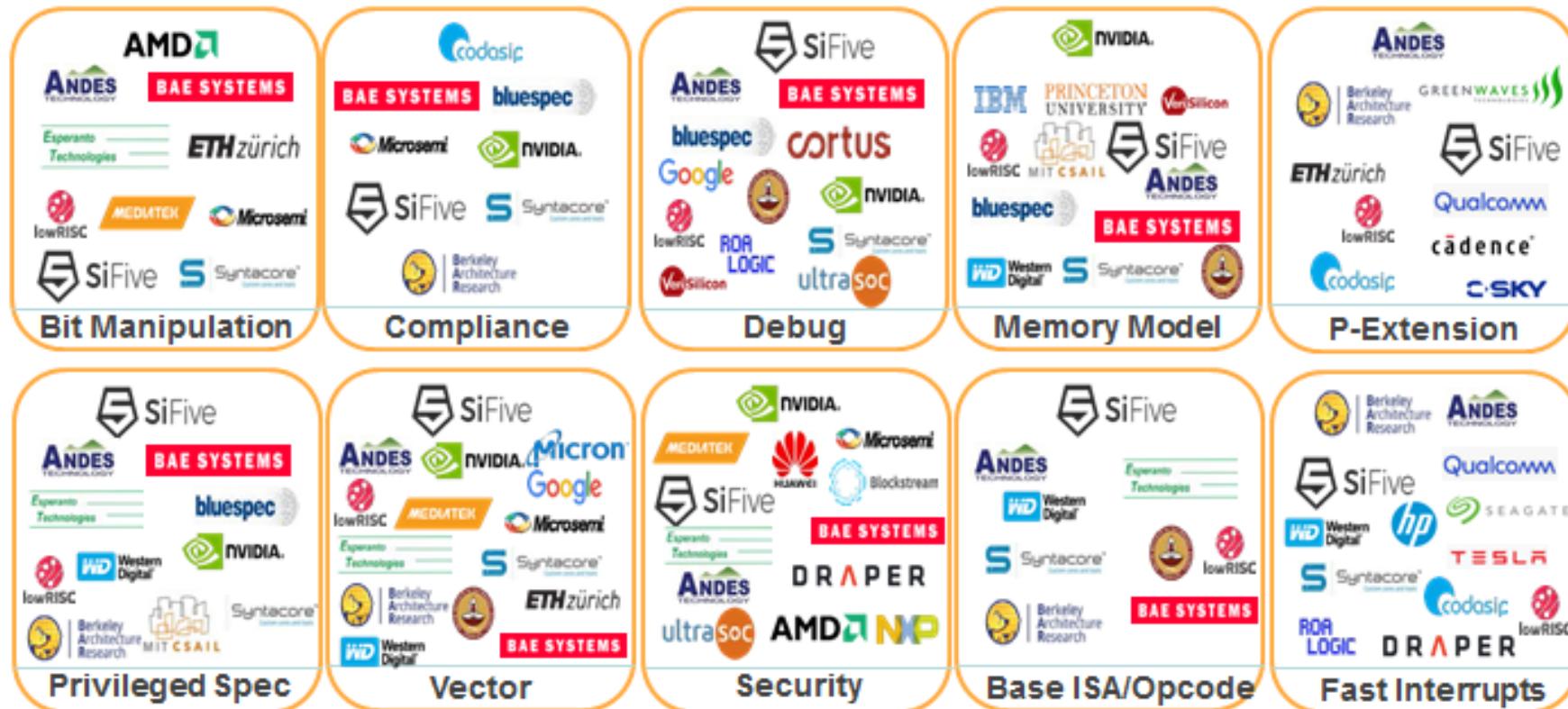
Executable
or library

Source file

積極參與RISC-V社群活動



Foundation Task Groups (partial list)



- ❖ Contributing hardware architecture extensions
 - Chair of the P-extension (Packed SIMD/DSP) Task Group
 - Co-chair of Fast Interrupts Task Group
 - Closely reviewing activities of other Task Groups

晶心協助強化RISC-V生態系統



- ▶ More choices for customers are good
- ▶ Andes works closely with partners to grow RISC-V ecosystem



RISC-V 軟體生態系統: GNU Toolchain



Barcelona
May 2018

The State of RISC-V Software

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports rvfpu-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

SiFive bluespec redhat ANDES

GNU Toolchains

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM
 - Talk yesterday afternoon
 - Poster on Tuesday night
- RV32IM[AFD] support upstream
 - Missing hard float calling convention
 - Missing 64-bit support
 - Missing compressed support
- Clang, Go, and OpenJDK have run code
 - Rust yet
 - Poster

lowRISC Berkeley LLVM

RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV32I-based systems
 - Drivers are trickling in now

Berkeley SiFive ANDES

Linux

- ❖ **GCC, binutils:** May, 2017
- ❖ **Newlib:** Aug, 2017
- ❖ **Glibc (rv64i):** Feb, 2018
- ❖ **GDB:** Mar, 2018
- ❖ **OpenOCD:** July, 2018
- ❖ **Glibc (rv32i):**
 - Submitted in July 2018 (by Andes)
 - Review in progress

RISC-V 軟體生態系統: LLVM Compilation



❖ LLVM:

- RV32IMAFDC: June, 2018
- Relaxation: May, 2018 (by Andes)
- 64b support: Nov, 2018
- Missing hard-float calling convention

❖ compiler-rt: Mar, 2018

❖ LLD: Aug, 2018 (by Andes)

- Initial port (relocation and TLS) in Oct. 2017
- Dynamic linking review in progress since Oct, 2017
- Missing link-time relaxation

The State of RISC-V Software

Barcelona May 2018

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports soft-float-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

SiFive bluespec redhat ANDES

RISC-V LLVM Porting Effort

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 - Poster on Tuesday night
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 - Missing hard float calling convention
 - Missing 64-bit support
 - Missing compressed support
- Clang, Go, and OpenJDK have run code
 - Rust project
 - Poster on Tuesday night

LLVM

RISC-V Linux Kernel Port

- Linux: January, 2018
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Berkeley SiFive ANDES

RISC-V 軟體生態系統: Linux



The State of RISC-V Software

Barcelona
May 2018

GNU-Based Toolchains

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 - Missing 64-bit support
 - Missing compressed support
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 - First port in progress
 - Poster on Tuesday

RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64-based systems
 - Drivers are trickling in now

SiFive
bluespec
redhat
ANDES
lowRISC
Berkeley
Intel

Linux

- ❖ U-boot: Jan, 2018 (by Andes)
- ❖ Kernel (rv64i): Jan, 2018
- ❖ Key utilities: (by Andes)
 - Perf: Feb, 2018
 - Kernel Module: May, 2018
 - Ftrace: May, 2018
- ❖ Kernel (rv32i): Jun, 2018 (by Andes)
- ❖ Kernel with CONFIG_FPU: Oct, 2018 (by Andes)

晶心在 RISC-V 上的定位



完整的產品組合

可靠的 RISC-V 核心 IP 供應商

可在Linux環境中執行的RISC-V 處理器核心

超低功耗、高運算效能的處理器核心

領先世界推出具有客戶可自訂指令的
RISC-V處理器核心



生態系統: Andes 與 Knect.me



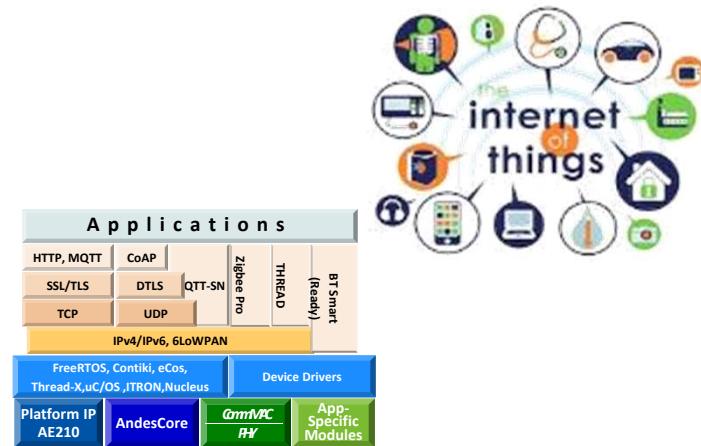
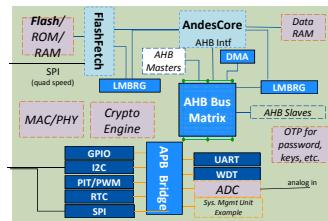
ANDES
TECHNOLOGY

knectme™

Knect.me 生態系統



- ❖ Built up Ecosystem [knect.me](#) to help IoT Developing
 - to knect solutions - Silicon IP's, SW stacks, tools, applications, systems and products
- ❖ Includes:
 - SoC IP Platforms
 - Software Stack
 - Development Boards
 - Development Tools
- ❖ To Form a IoT League
 - to knect chip vendors, partners, application developers, system vendors





近期獲獎

引領新興科技潮流



► “2018 Top25最佳新興科技解決方案提供公司”
— CIO Advisor Magazine



總結

晶心科技擴大產品陣線,強化生態系統

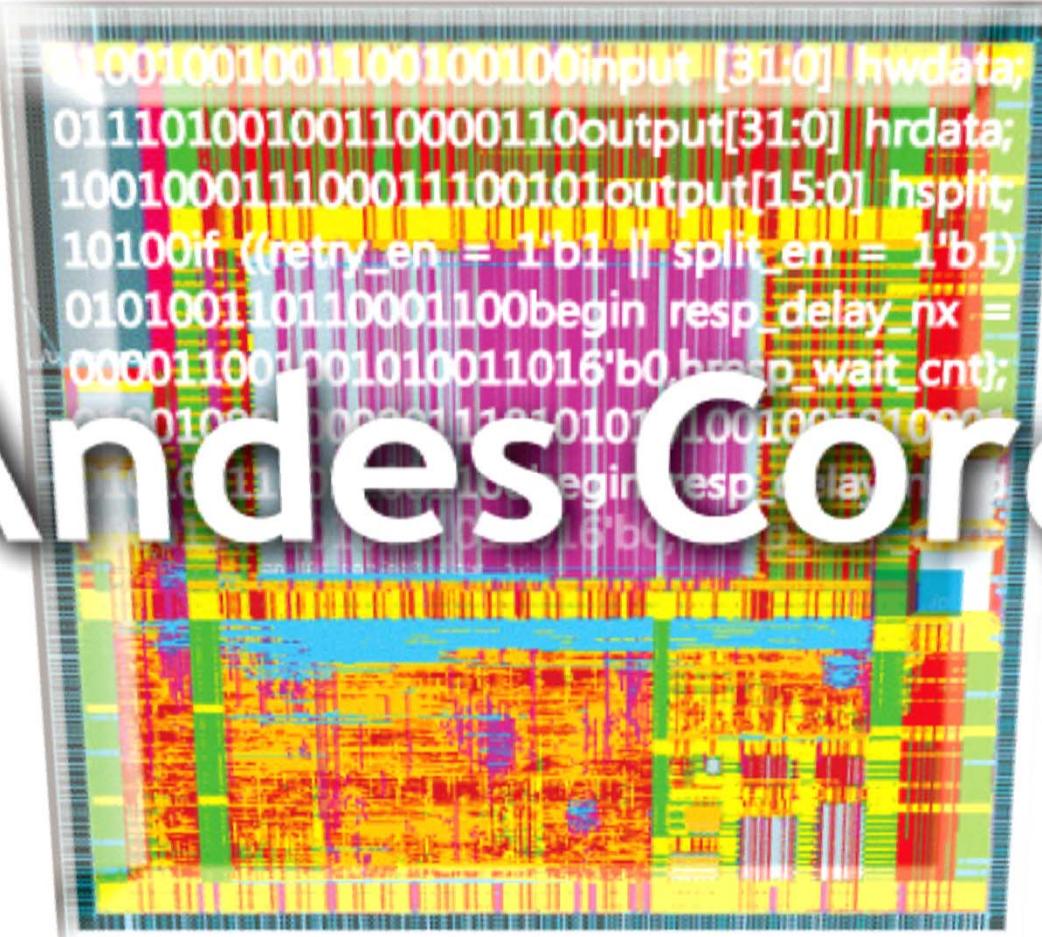


- ❖ 晶心科技發布了新的RISC-V處理器核心 (N22, A(X)25MP, D25F) , 適合更多的客戶應用。
- ❖ 晶心科技積極參與 RISC-V 基金會科技與社群發展，並與RISC-V 生態系統互助。
- ❖ 晶心科技持續與全球 Design service houses簽訂合約，授權其協助客戶開發內嵌 Andes RISC-V core的 ASIC (稱為Andes RISC-V Easy Start Program) ，創造晶心、Design service house與產業共贏的局面。

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