TWS Solution Using Andes D25+ACE

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### Highlights of TWS with ACE

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<tr>
<th>Function Name</th>
<th>Insn cycles</th>
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Agenda

- TWS Platform
- Andes V5 Role in TWS
- D25 + ACE TWS Solution
- TWS ACE Instruction
TWS Platform Introduction
TrueWireless Stereo (TWS) Platform

Playback sync: TrueWireless™ Stereo

Bluetooth Version: Bluetooth 5.0, 4.2

Bluetooth Technology: Dual-mode, Single, BLE

ANC: Feedforward, Feedback, Hybrid

Audio interface: I2S, SPDIF, DAC

MIC: N * AMIC, N * DMIC
TWS Challenges

- **Audio playback synchronization**
  - PLL accuracy
  - Playback start timing

- **Active noise control computation** **ACE**
  - High amount of computation
  - Low latency data path requirement

- **Audio codec and audio format conversion**
  - PCM(24bits), little endian, big endian **ACE**
  - LDAC, APTX, AAC

- **Computation and power trade off**
  - Large amount of multiplication and addition **ACE**
  - Low power & high precision DAC (Analog)
  - Low latency ADC
ANC Challenges in TWS

- ANC challenges
  - Restrict latency
  - Real time sample base streaming (1 sample in, 1 sample out)
  - Limited resource with high computation requirement
  - Low power, Low latency, High sample rate ADC & DAC

- Example:
  - ADC & DAC in 192KHz (1 sample = \(\frac{1}{192\text{KHz}}\) \(\sim\) 5us)
  - CPU clock 160MHz
  - The algorithm should be finished in 800 clock cycles. (160M * 5us = 800)
ANC Algorithm (Hybrid)

• For higher noise control performance, the higher filter tap number should be used

• For example: how many addition and multiplication are needed for 128 taps?

• Total 896 additions & 896 multiplications for 1 sample
ANC Conclusion

- Example:
  - ADC & DAC in 192KHz (1 sample = $\frac{1}{192kHz} \approx 5\text{us}$)
  - CPU clock 160MHz
  - The algorithm should be finished in 800 clock cycles. (160M * 5us = 800)
  - ANC Feedforward : Total 384 MACs for 1 sample
  - ANC Hybrid : Total 896 MACs for 1 sample
### ANC FIR & LMS Profiling

<table>
<thead>
<tr>
<th>Name</th>
<th>Calls</th>
<th>Self InsC</th>
<th>Self CycC</th>
<th>Total InsC</th>
<th>Total CycC</th>
<th>Time Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>fir_cal</td>
<td>4</td>
<td>5,148</td>
<td>6,765</td>
<td>5,148</td>
<td>6,765</td>
<td>30.08%</td>
</tr>
<tr>
<td>init_buf</td>
<td>7</td>
<td>5,411</td>
<td>5,522</td>
<td>5,411</td>
<td>5,522</td>
<td>24.55%</td>
</tr>
<tr>
<td>do_printf</td>
<td>4</td>
<td>1,808</td>
<td>3,938</td>
<td>3,536</td>
<td>6,002</td>
<td>17.51%</td>
</tr>
<tr>
<td>lms_cal</td>
<td>2</td>
<td>2,826</td>
<td>3,639</td>
<td>2,826</td>
<td>3,639</td>
<td>16.18%</td>
</tr>
<tr>
<td>vprintf</td>
<td>68</td>
<td>1,156</td>
<td>1,426</td>
<td>1,564</td>
<td>1,846</td>
<td>6.44%</td>
</tr>
<tr>
<td>__riscv_save_3</td>
<td>68</td>
<td>408</td>
<td>420</td>
<td>408</td>
<td>420</td>
<td>1.87%</td>
</tr>
<tr>
<td>vprintf</td>
<td>4</td>
<td>124</td>
<td>159</td>
<td>3,688</td>
<td>6,215</td>
<td>0.71%</td>
</tr>
<tr>
<td>main</td>
<td>1</td>
<td>96</td>
<td>155</td>
<td>17,229</td>
<td>22,380</td>
<td>0.69%</td>
</tr>
<tr>
<td>strlen</td>
<td>4</td>
<td>88</td>
<td>124</td>
<td>88</td>
<td>124</td>
<td>0.55%</td>
</tr>
<tr>
<td>__riscv_save_12</td>
<td>4</td>
<td>76</td>
<td>94</td>
<td>76</td>
<td>94</td>
<td>0.42%</td>
</tr>
<tr>
<td>printf</td>
<td>4</td>
<td>60</td>
<td>84</td>
<td>3,748</td>
<td>6,299</td>
<td>0.37%</td>
</tr>
<tr>
<td>_write</td>
<td>4</td>
<td>28</td>
<td>54</td>
<td>28</td>
<td>54</td>
<td>0.24%</td>
</tr>
<tr>
<td>memset</td>
<td>1</td>
<td>25</td>
<td>43</td>
<td>38</td>
<td>60</td>
<td>0.19%</td>
</tr>
<tr>
<td>_start</td>
<td>1</td>
<td>24</td>
<td>36</td>
<td>17,299</td>
<td>22,491</td>
<td>0.16%</td>
</tr>
<tr>
<td>memset + 70</td>
<td>1</td>
<td>13</td>
<td>17</td>
<td>13</td>
<td>17</td>
<td>0.08%</td>
</tr>
<tr>
<td>_exit</td>
<td>1</td>
<td>8</td>
<td>15</td>
<td>8</td>
<td>15</td>
<td>0.07%</td>
</tr>
</tbody>
</table>

**Total Self Cycle Count:** 22491

**Single 128-tap FIR takes about **1600 cycles**

**Single 128-tap LMS takes about **1800 cycles**
ANC in Hardware

Advantage
1. Parallel computing
2. Optimized data path

Absolute Efficiency (not flexible)

Disadvantage
1. Fixed architecture, Fixed algorithm
2. Complicated SRAM access

Complete Flexibility (power consuming)

High Efficiency & Flexibility

FIR (128taps)
LMS (128taps)
Andes V5 Role in TWS
Andes V5 Role in TWS

- CPU + DSP
  - Lots of redundant functions

- DSP + DSP
  - Lots of redundant functions

- D25 + ACE
  - Best choice for TWS!
TWS Platform

- RF
- Baseband Controller
- Exchange memory (64KB)
- PLL CPU
- PLL AUD
- PLL BT
- ADC
- DAC
- Audio subsystem
- Internal memory (192KB, 256KB, 384KB)
- Internal memory (192KB, 256KB, 384KB)

AXI/AHB Bus Matrix

- D25F
  - (RISC-V with P extension)
  - CPU + DSP
  - ACE (e.g. background fir)
  - ACE (e.g. background lms)
  - ACE (e.g. background dma)

- APB Bridge
- APB Device

Driving Innovations™
D25 + ACE TWS Solution
ANC: D25 W/ ACE Solution

ANC Hybrid solution (low power, small area)

800 cycles

- Bg DMA
- Bg 128 taps FIR (Shat)
- Bg 128 taps LMS
- Bg 128 taps FIR (ADAP)
- ANC control
- Audio codec
- MISC routine
- DMA
- BT control flow
Example:

- ADC & DAC in 192KHz (1 sample = \( \frac{1}{192KHz} \) \( \sim \) = 5us)
- CPU clock 160MHz
- The algorithm should be finished in 800 clock cycles. (160M * 5us = 800)

Example (with ACE):

- ADC & DAC in 192KHz (1 sample = \( \frac{1}{192KHz} \) \( \sim \) = 5us)
- CPU clock 80MHz
- The algorithm should be finished in 400 clock cycles. (80M * 5us = 400)
TWS D25+ACE Solution

ram coef_sram {  //coef. Custom Memory
}
ram data_sram{  //vector Custom Memory
}
vec bg_insn fir_cal {
    operand=...;
    csim=...;
    latency= 128;  //enable multi-cycle ctrl
};
vec bg_insn lms_cal {
    operand=...;
    csim=...;
    latency= 128;  //enable multi-cycle ctrl
};
bg_insn bt_dma{
    operand=...;
    csim=...;
};

//ACE_BEGIN: fir_cal
reg [31:0] fir_out_reg;
wire [31:0] acc;
assign acc = (ace_vstart) ? 64'd0 : fir_out_reg;
assign fir_out = coef32[31:0] * buf32[31:0] + acc;
always @(posedge core_clk or negedge core_reset_n)
begin
    ......
end
//ACE_END

//ACE_BEGIN: lms_cal
assign coef32_out = .....;
//ACE_END

//ACE_BEGIN: bt_dma
......
//ACE_END
TWS ACE Instruction
Introduction
128-Tap FIR Instruction

\[ W(z) \Rightarrow y[n] = \sum_{k=0}^{M} W_k \times x[n - k] \]

```cpp
for (int k = 0; k < M; k++)
    Y += (W[k] * X[k]); //calculate filter output
```

![Diagram of ACM and ACR](image-url)
D25 ACE Platform

Diagram showing the architecture of the D25 ACE Platform, with various components and connections labeled.

Component labels include:
- d25_core_top
- vc_ilm_ram
- vc_dlm_ram
- debugint
- mtip
- msip
- meip
- d25_core
- ace_sram0 (s_hat coef)
- ace_sram1 (ADAP_A)
- ace_sram2 (ADAP_C)
- ace_sram3 (Audio_buf)
- ace_sram4 (adder_buf)

Other labels:
- lms_cal0
- lms_cal1
- fir_cal0
- fir_cal1
- fir_cal2
- bt_dma
- Bus Master (AHB_M)
- Bus Matrix

The diagram illustrates the connections and components within the ACE Platform architecture.
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D25 + ACE @CPU clock 80MHz
Conclusion

- TWS solution using Andes D25+ACE
- New idea of how to design a SOC
- Andes V5 role in the TWS platform
- Example of ANC customized instruction using ACE
Thank you,
See you next webinar!