RISC-V CON

ONLINE WEBINAR

Andes RISC-V V5 CPUs

Mark Lai

Andes RISC-V CPU IPs

- **Andes with rich experience on CPU design and market**

- **Provides high quality RISC-V CPU IPs – Risk Free**
  - Andes RISC-V good at PPA performance – Power, Performance, Area
  - Professional DSP support – DSP ISA, C libraries and compiler
  - ACE & COPILOT – Generate custom instructions automatically

- **RISC-V + ACE**
  - Compact + High Performance + Flexible + Low Power

Andes: Trusted Computing Expert and Your Best RISC-V Partner!

Highlights of RISC-V V5 CPU IPs

- Andes Custom Extension™ (ACE)
- P-extension (DSP) and V-extension (Vector)
- Excellent PPA performance and code density
- Caches
  - Complete cache management, controlled by CSRs
- Local memories
  - Capable of copying boot code to LM when resetting CPU
  - Access up to 32 MB local memories via V5's AHB slave port
- Support vectored interrupt & unaligned mem access
- Comprehensive debug solutions

Andes V5 Processor Lineup

	RV32	RV64	Vector Ext.	Superscalar
Cache-Coherent 1-4 Cores	A25MP	AX25MP	**27-Series:** MemBoost Vector Ext. NX27V A27/AX27 and more.	**45-Series:** MemBoost Dual Issue. N45/NX45 D45/DX45 A45/AX45 and more.
Linux with FPU/DSP	A25	AX25		
Fast/Compact with FPU/DSP	N25F D25F	NX25F		
	5-stage		5-stage	8-stage

N22
2-stage

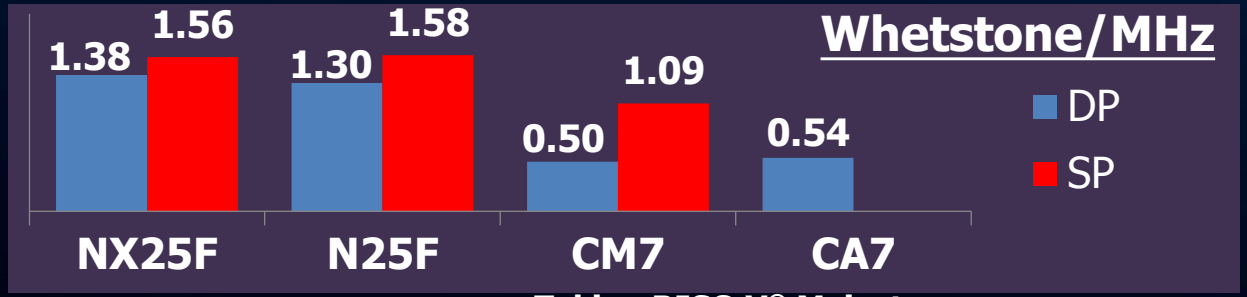
Note: Common features are RV*IMACN, Caches, LM, ECC, BrPred, CoDense™, PowerBrake , StackSafe™ ACE (Andes Custom Extension™); Frequencies at 28nm

V5 25-Series Performance

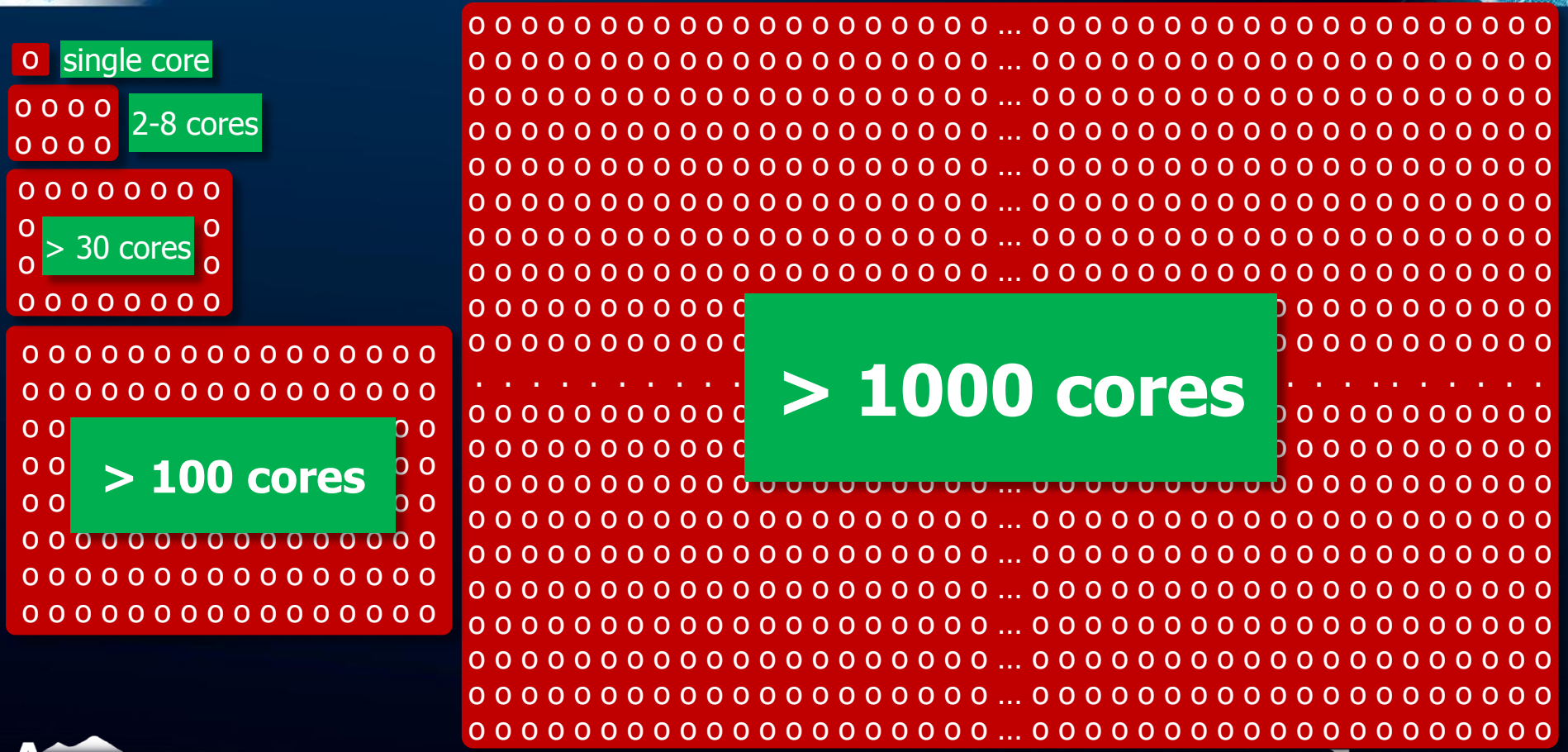
Features	Base	FP	Linux	Linux
32KB I$/D$ + 256 BTB	Yes	Yes	Yes	Yes
SP/DP FPU	--	Yes	Yes	Yes
MMU and S-Mode	--	--	Yes	Yes
RV-P ext. draft (DSP)	--	--	--	Yes
Worst-Case Freq. (GHz)[1]	1.2	1.2	1.2	1.1
Coremark/MHz[2]	3.57 (rv32), 3.53 (rv64)			
DMIPS/MHz[2]	1.97 (rv32), 2.13 (rv64)			

1: **28nm** SVT 9T library and high-speed memory. Frequency at 0.81v/-40ºc.
2: **AndeSight v320** toolchain; DMIPS/ground rule uses no-inline option.

- **Linux support**
  - RISC-V MMU and S-mode
    - SV{32,39,48}, all page sizes
  - 4-way 32~128-entry STLB
  - 4 or 8-entry ITLB and DTLB
- **FPU (RV-F or RV-FD)**
  - +, –, x, x+, x–:
    - pipelined 5 cycles
  - ÷, √ : run in background
    - SP: 15 cycles, DP: 29 cycles

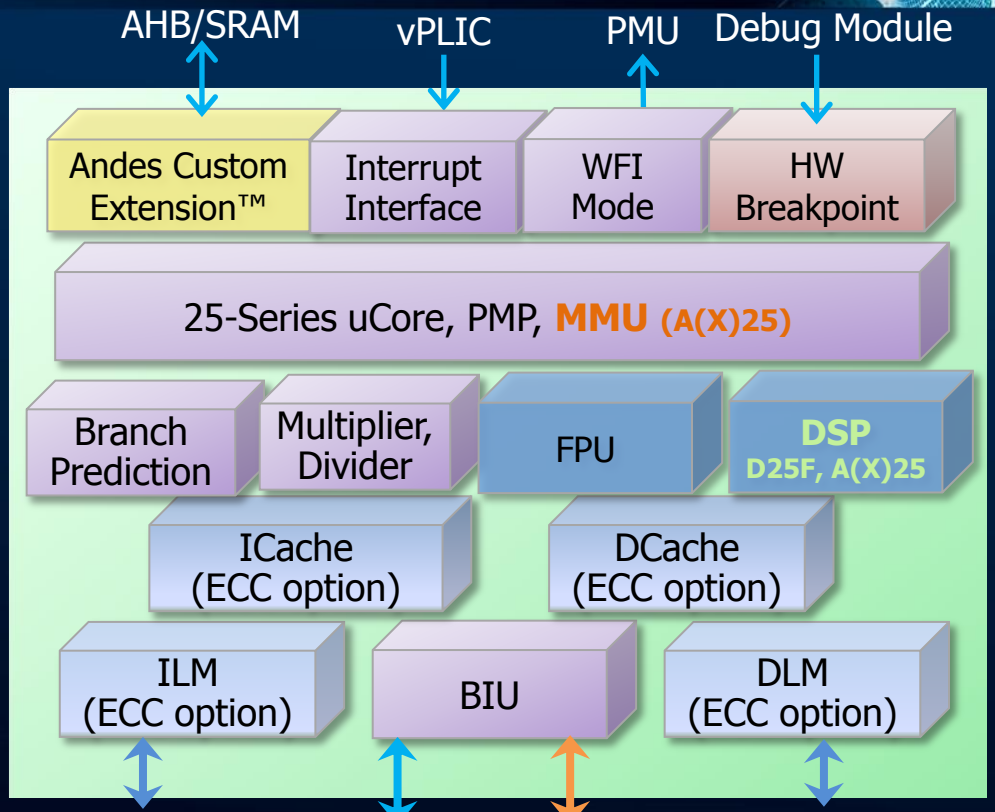


Andes RISC-V V5 in SoC



Andes RISC-V 25-Series Core Overview

- **AndeStar V5 architecture:**
  - RV32/RV64-IMACN + Andes Extensions
  - Optional FPU: SP, DP
  - Optional **DSP/SIMD: P**
  - Optional S-mode/MMU: SV32/39/48
- **5-stage pipeline, single-issue**
- **Configurable multiplier**
- **Optional branch prediction**
- **I/D caches and Local Memory**
  - Optional parity or ECC protection
  - Hit-under-miss caches
  - HW unaligned load/store accesses
- **Bus interface**
  - Master ports (AXI64*2/AHB{64,32})
  - Optional **AHB slave port accessing 4KB ~ 32MB LM address space**



25-Series Features Overview

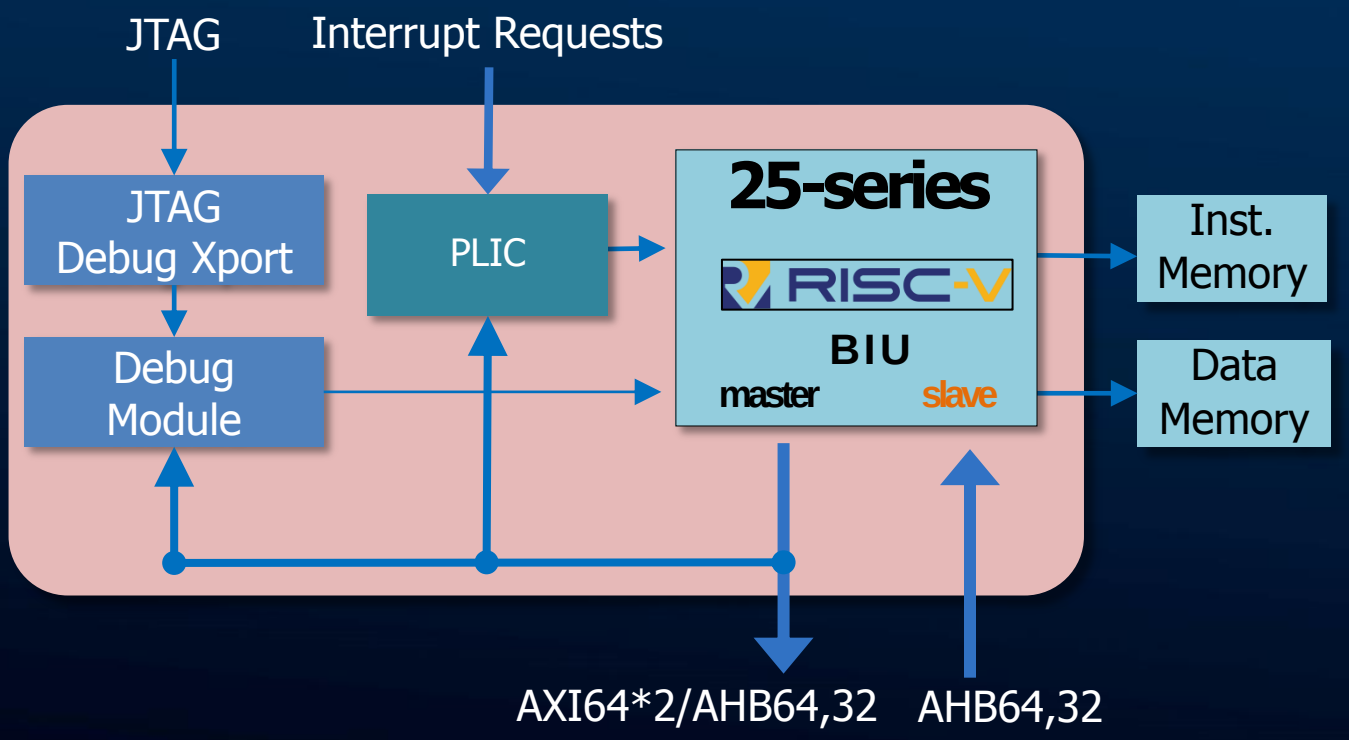
Features	N25F	D25F	A25	NX25F	AX25
AndeStar ™	V5+RV32-FD-N	V5+RV32-FD-P-N		V5+RV64-FD-N	V5+RV64-FD-P-N
Pipeline & GPR#	5-stage, 32 32-bit GPRs			5-stage, 32 64-bit GPRs	
FPU	Single/Double precision (IEEE754-compliant)				
DSP	--	RV32-P (draft), DSP/SIMD		--	RV64-P (draft), DSP/SIMD
MMU	--	--	Sv32 virtual-memory	--	Sv39 & SV48 virtual-memory
Privilege mode	M+U		M+U+S	M+U	M+U+S
Master Bus	AXI64*2, AXI64, AHB64 or AHB32 32 (A25: 32-34) bit address			AXI64*2, AXI64 or AHB64 32-64 bit address	
Slave Bus	AHB64 or AHB32			AHB64	
Branch Pred.	Static/Dynamic (BTB,BHT,RAS)				
Multiplier	Radix2/Radix4/Radix16/Radix256/Fast				
Memory system	I&D Local Memory, up to 16MiB; I&D cache, up to 64KiB				
Unique Features	CoDense™, StackSafe™, PowerBrake, QuickNap™, ECC/Parity, misaligned access, **Andes Custom Extension™**				
Debug Module	4-wire JTAG/2-wire Serial Debug Port; with Exception Redirection				
PLIC	Vectored dispatch, priority-based preemption, up to 1023 sources, 255 priorities, 16 targets				

Andes CPU GUI Configuration Tool

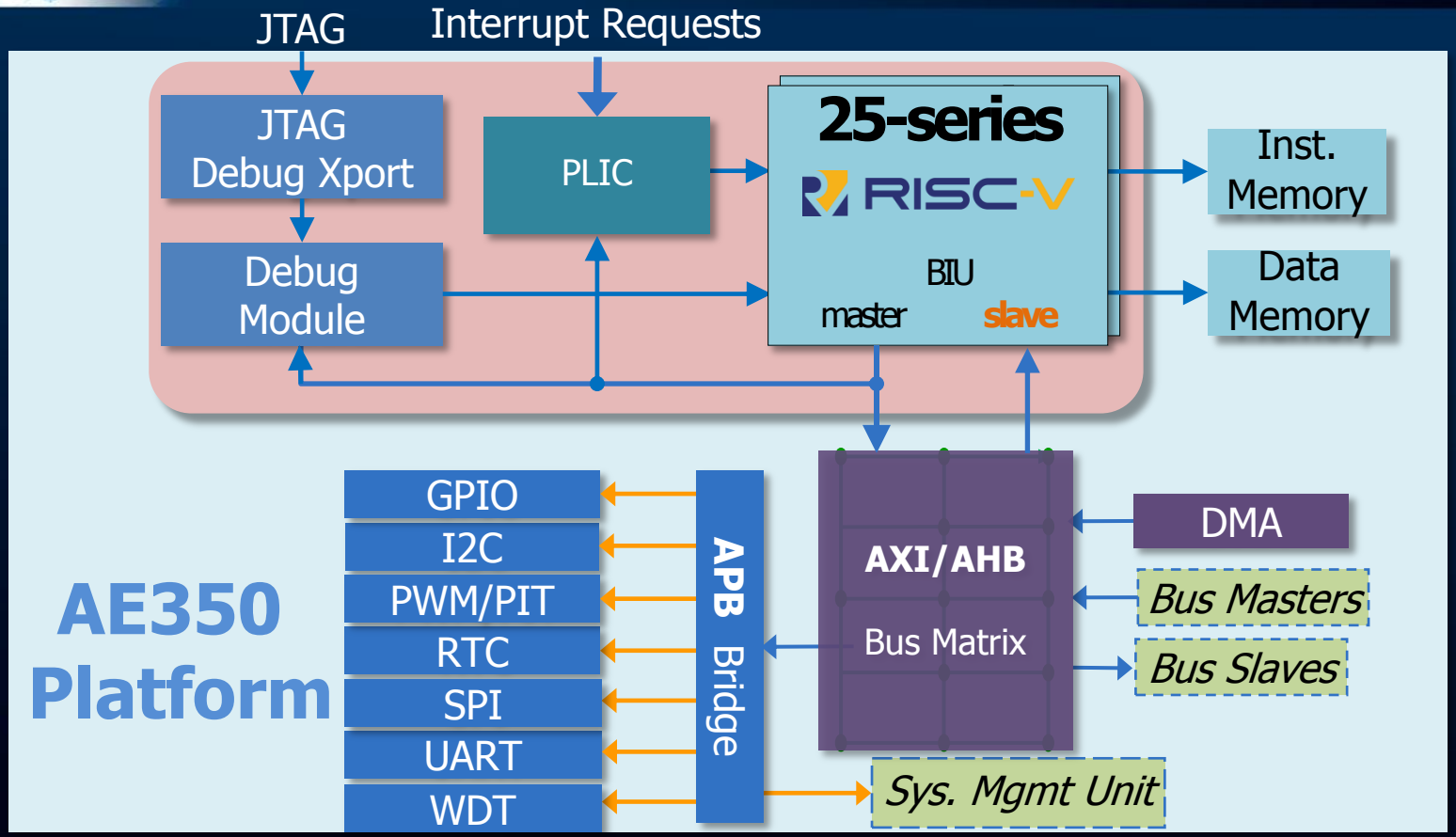
Generate n25_core | Save | Load | Quit

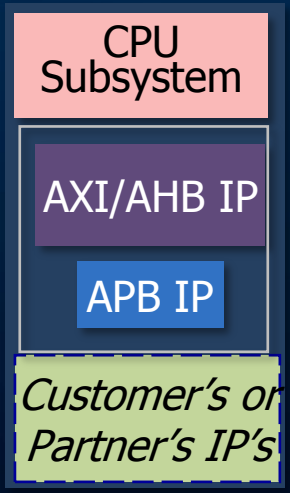
ISA	
RISC-V User-Level Interrupt Extension	○ yes ◉ no
RISC-V Atomic Instruction Extension	○ yes ◉ no
RISC-V Float-Point Extension	○ none ○ Single-Precision ◉ Double-Precision
Andes Cutsom Extension	○ yes ◉ no
Privilege Architecture	
Privilege Modes	◉ Machine ○ Machine + User
Physical Memory Protection Entries	○ 0 ○ 2 ○ 4 ○ 8 ◉ 16
Performance Monitors	○ yes ◉ no
Andes Vectored PLIC Extension	○ yes ◉ no
Andes StackSafe Extension	○ yes ◉ no
Andes PowerBrake Extension	○ yes ◉ no
Bus Interface	
Bus Type	○ ahb ◉ axi
BIU Two-port Structure	◉ yes ○ no

Configurable CPU Subsystem



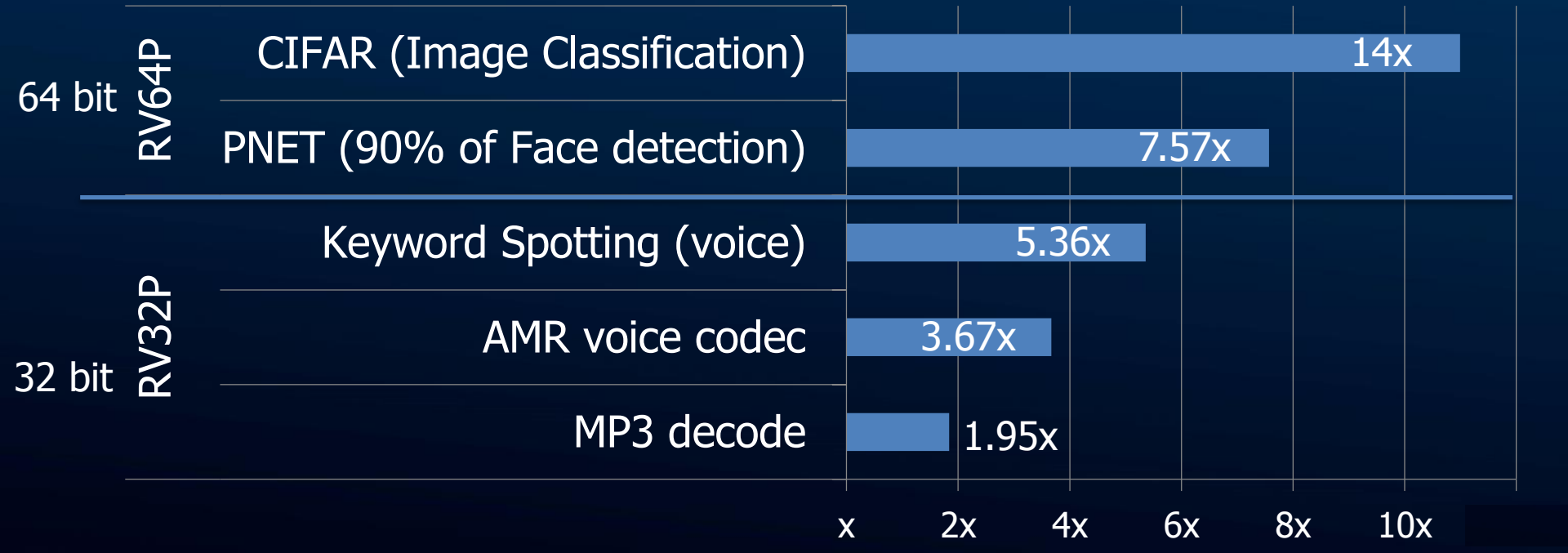
Easy SoC Integration





Speedup with DSP ISA on 25-Series

- **Real world speed up, using DSP extension**



DSP Support

- **DSP ISA**
  - The basis of RISC-V P-extension draft that Andes contributed.
  - 300 instructions derived and evolved from real use cases (over decades)
    - Support 32 bits and 64 bits
    - Support saturation and rounding
    - Cover SIMD, partial SIMD, bit manipulation and etc.
- **DSP intrinsic functions**
  - Users can use as C-like functions without bothering to program in assembly
- **DSP library**
  - >200 functions in 8 categories (basic, complex, controller, filtering, matrix, statistics, transform, utils)
- **Some DSP instructions are auto-generated by compiler to facilitate development**
- **Compatible with CMSIS-DSP library API**
  - By including an API wrapper header file
  - Microcontroller Software Interface Standard (CMSIS)

DSP Library Comparison with CPU A

- **RV32-P: Speedups over CPU A (with 3% larger code size)**

	Speedup	Basic	Cmplx	Ctlr	Filter	Matrix	Ststcs	Xform	Utils	ALL
Q	AVG	1.80	1.26	1.73	1.31	1.19	2.20	1.08	1.40	1.50
	MAX	6.94	1.80	2.17	2.63	1.77	6.75	1.31	2.77	6.94
F32	AVG	1.31	1.33	2.31	1.08	1.42	1.23	1.14	1.24	1.38
	MAX	1.42	1.64	2.55	2.09	1.78	1.35	1.39	2.05	2.55

- **RV32-P: Speedups over CPU A (with 32% smaller code size)**

	Speedup	Basic	Cmplx	Ctlr	Filter	Matrix	Ststcs	Xform	Utils	ALL
Q	AVG	1.45	1.11	1.54	1.28	1.03	1.93	1.07	1.30	1.34
	MAX	5.15	1.59	1.85	2.63	1.56	5.29	1.31	2.77	5.29
F32	AVG	1.01	1.13	1.74	1.03	1.16	1.12	1.13	1.02	1.17
	MAX	1.35	1.48	2.11	2.09	1.55	1.22	1.39	2.05	2.11

DSP Instruction Examples

Types	Instruction Operations	Cycles
SIMD	Four 8x8 multiplications: 16= 8x8; 16= 8x8; 16= 8x8; 16= 8x8 Two 16x16 multiplications: 32= 16x16; 32= 16x16	1
Partial SIMD	Four 8x8 multiplications with 32b accumulation: 32= 32 + 8x8 + 8x8 + 8x8 + 8x8; 32= 32 + 8x8 + 8x8 + 8x8 + 8x8 (2nd op: RV64 only) Two 16x16 multiplications with 32b accumulation: 32= 32 + 16x16 + 16x16; 32= 32 + 16x16 + 16x16 (2nd op: RV64 only)	2
RV64 Only	Two 32x32 multiplications with 64b accumulation: 64= 64 + 32x32 + 32x32	3

D25F vs. CPU A

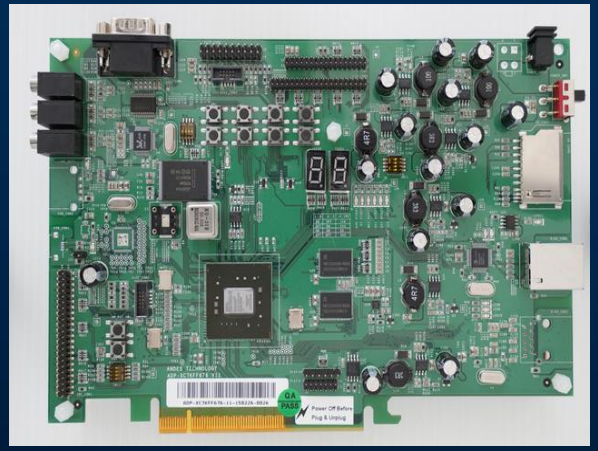
Features	D25F	CPU A
Custom Instruction	Andes Custom Extension™	No
Pipeline stages	5 stages	3 stages
Floating point	SP, DP, HP conv. at LD/ST, Background ÷√	SP only
DSP Extensions	SIMD-instructions with 8/16/32-bit element size Complex DSP instructions operating on 16/32/64-bit data	8/16-bit SIMD arithmetic
I/D Local Memory	4KB~16MB	Yes
L1 I/D Cache	8KB~64KB	No
SRAM Error Protection	ECC or Parity	No
Bus Interface	AHB32, AHB64, or AXI64	AHB Lite, APB
I/D Local Memory DMA	With AHB slave port	No
Pre-integrated Platform	AXI-based platform	No
Additional Features	CoDense™ code size reduction, StackSafe™ stack protection, PowerBrake & QuickNap™ power management	-
DMIPS/MHz	**1.96**	1.25
CoreMark/MHz	**3.58**	3.42

Note: N25F use AndeSight v3.1.0; DMIPS/MHz follows the ground rule with no-inline option.

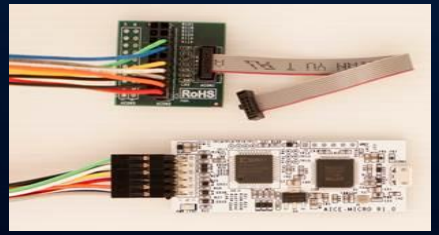
AndeShape™ and Comprehensive Kits

- **AndeShape™ Development Boards**
  - Full-Featured ADP-XC7K
  - Compact Corvette-F1 (Arduino-compatible)
    - With 802.15.4 and ICE on board
- **Debugging Hardware**
  - AICE-MINI+, AICE-MICRO
- **Near-Cycle Accurate Simulator**
- **Qemu Virtual Board**
  - AX25+AE350 SoC platform, booted U-Boot/Linux
  - openSUSE project used it for UEFI development
- **AndeSoft™ Software Stack**
  - Bare metal demo projects
  - RTOS'es: FreeRTOS, ThreadX, Contiki, more
  - Linux: RV32/RV64, UP and SMP
- **Rich Support from 3rd Parties**
  - IAR, Imperas, Lauterbach, Segger, UltraSoC, etc.

Corvette-F1



ADP-XC7K

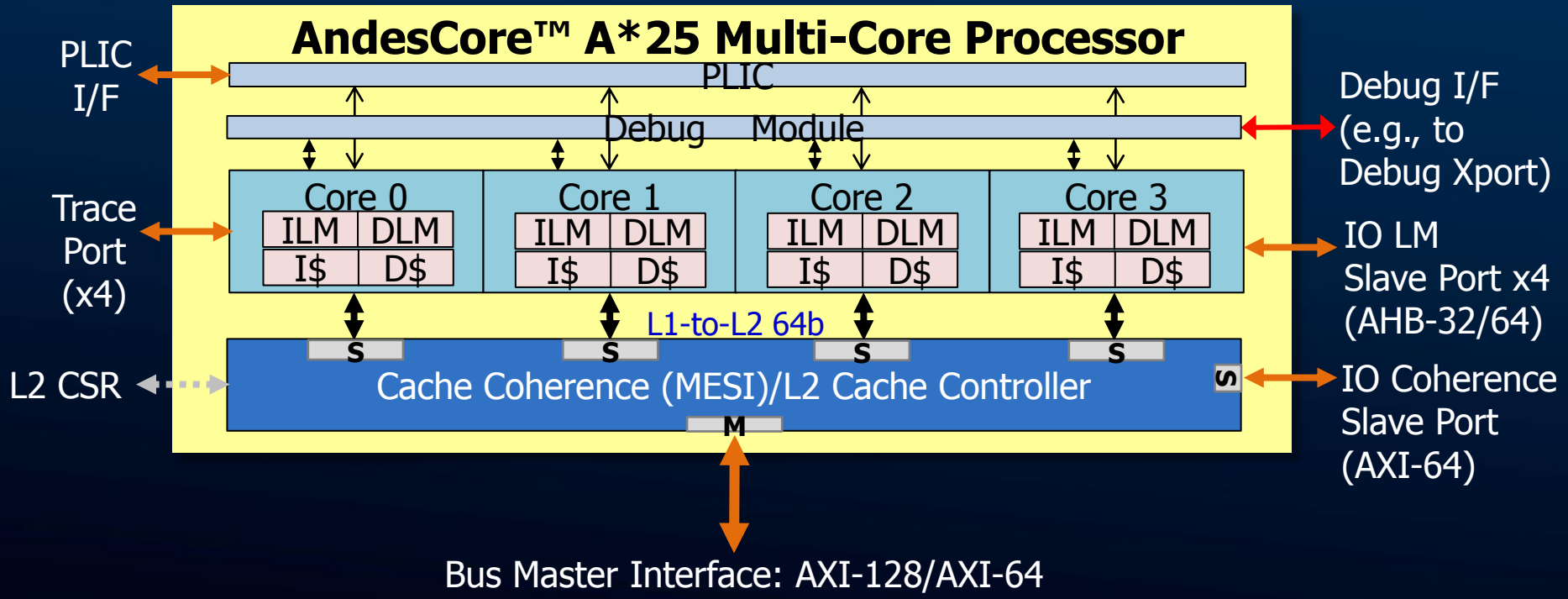


AICE-MICRO

AICE-MINI+

A25/AX25 Multi-Core Processor (1/2)

- Configurable L2 cache size of 0KiB, 128KiB, 256KiB, 512KiB, 1MiB and 2MiB



A25/AX25 Multi-Core Processor (2/2)

A25MP Multi-Core Benchmark on Linux			
Processors	Single-core	Dual-core	Quad-core
CoreMark	3.50	6.92	13.84

AX25MP Multi-Core Benchmark on Linux			
Processors	Single-core	Dual-core	Quad-core
CoreMark	3.45	6.90	13.80

Andes Custom Extension™ (ACE) Framework

- C code
- Verilog
- Attributes

- scalar/vector
- background
- wide operands

COPILOT

Custom-OPtimized Instruction deveLOpment Tools

Extended Tools + Compiler Asm/Disasm Debugger IDE

Extended ISS + CPU ISS (near-cycle accurate)

Extended RTL + CPU RTL

Extensible Baseline Components

Automated Env. For Cross Checking

Test Case Generator

Extended ISS

Extended RTL

Inner Product of Vectors with 64 8-bit Data

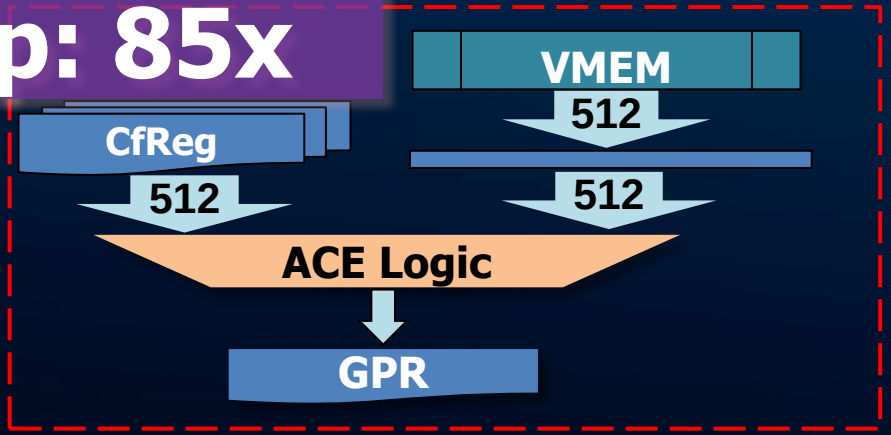
```
reg CfReg {                 //coef. Custom Register
    num= 4;
    width= 512;
}
ram  VMEM {                 //vector Custom Memory
     interface= sram;
     address_bits= 3;    //8 elements
     width= 512;
}
insn ip64B {
  operand= {out gpr IP,
                 in CfReg C, in VMEM V};
  csim= %{                  //multi-precision lib. used
    IP= 0;
    for(uint i= 0; i<64; ++i)
       IP+= ((C >>(i*8)) & 0xff) *
                ((V >>(i*8)) & 0xff);
  %};
  latency= 3;               //enable multi-cycle ctrl
};
```

ip64B.ace

```
//ACE_BEGIN: ip64B
assign IP= C[ 7:0]  * V[ 7:0]
           + C[15:8] * V[15:8]
              . . .
           + C[511:504] * V[511:504];
//ACE_END
```

ip64B.v

Speedup: 85x



Intrinsic: long **ace_ip64B**(CfReg_t, VMEM_t);

Madd32: Application C Code

Pure C Code

```
uint fir32(uint *C, uint *X, uint n) {
   uint  rslt= 0;
   for(int i=0; i<n; ++i)
      rslt+= (C[i] & 0xffff)*(X[i] & 0xffff);    //lower 16 bits
           + (C[i] >> 16)    *(X[i] >> 16);      //upper 16 bits
   return rslt;
}
```

With ACE

```
#include "ace_user.h"   //prototypes for generated intrinsic
 . . .
#ifdef USE_ACE
      rslt= ace_madd32(rslt, X[i],C[i]);     //invoke intrinsic
#else
       . . .
#endif
 . . .
```

out

in

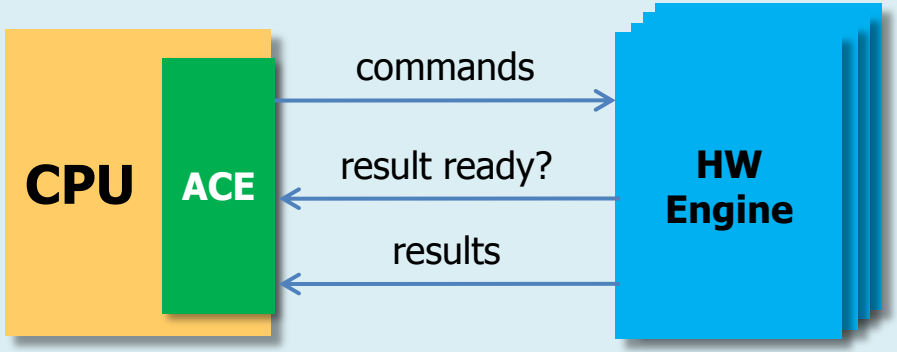
op= {io acc, in dat, in coef};

- Pure C**: 8 cycles**
- With ACE: 1 cycle
- **Speedup: 8x**

Custom Port (ACP) for Direct HW Engine Control

```
port command {      //a 90-bit output port to
                    // all 4 HW engines,
    width= 90;          //including a valid bit and
                    // a HW engine ID field
    io_type= out;
}
//4 HW engines
port ready {     //4 ready signals
    num=4;
    io_type= in;
}
port results {          //4 256-bit input ports
    num= 4;
    width= 256;
    io_type= in;
}
```

CPU controls 4 HW engines.

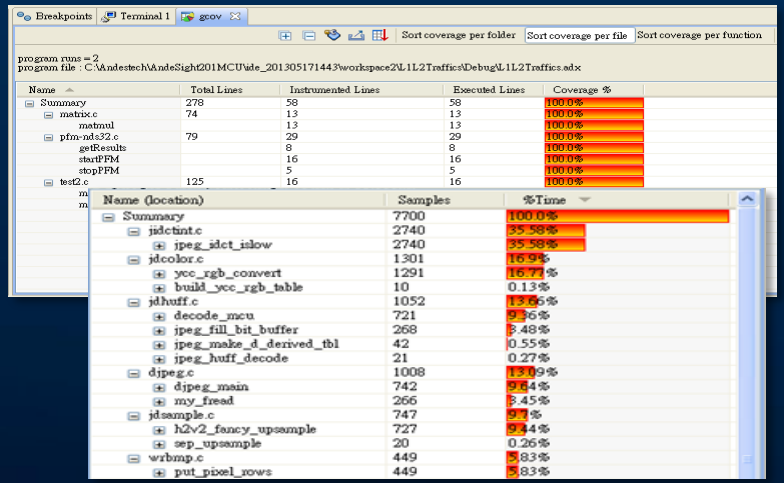


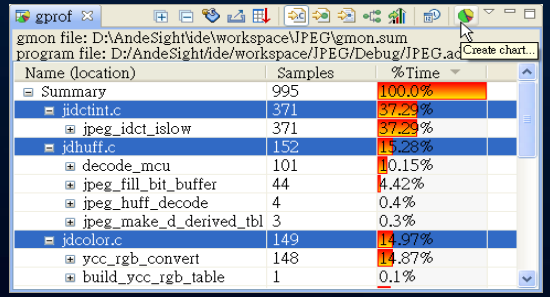
App. code sequence:

prepare command (say, thru ACR);
send command;
do other useful work;
wait for results to be ready;
get results;

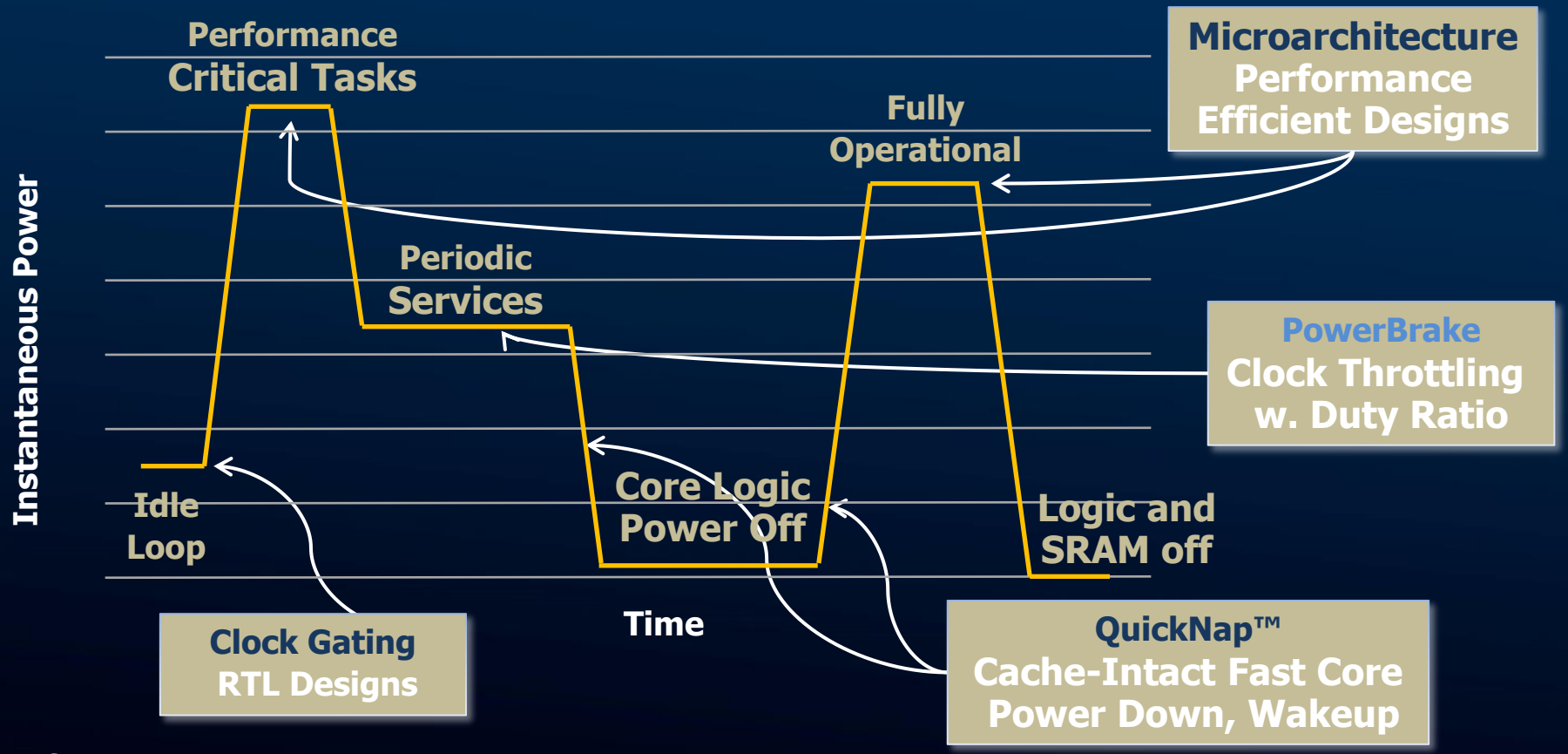
ACE Performance Profiling by AndeSight™

- **Eclipse-based**
- **Project Setup:**
  - **Linker Script Editor**
  - Flash ISP
- **Program Analysis**
  - Function Profiling
  - Performance Meter
  - Code Coverage
  - Function Code Size
  - (Static) Stack Size





Design for Energy Efficiency



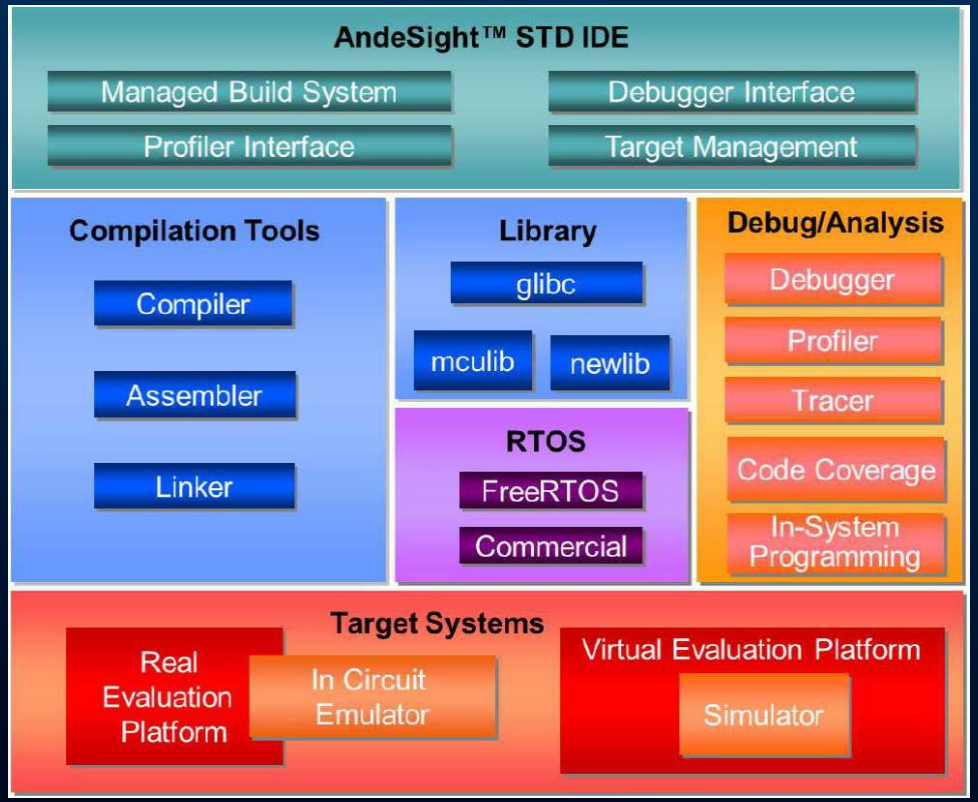
AndeSight™ IDE Overview

- **Three AndeSight™ Versions**

  STD
  - **Comprehensive with all features**

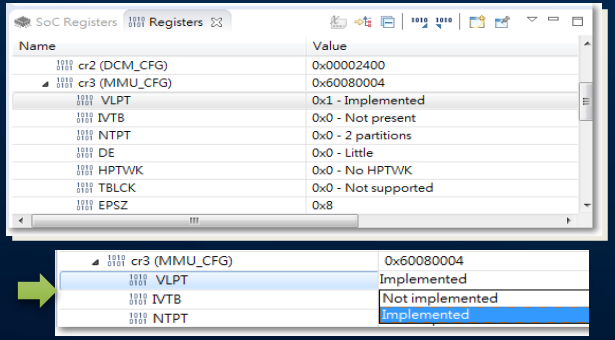
  RDS
  - **Customized for redistribution**

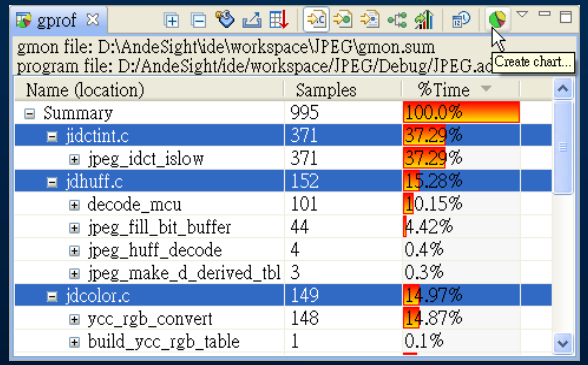
- **Comprehensive Features**
  - Eclipse-Based IDE
  - Streamlined GUI
  - Feature-rich Editor
  - Managed Build System
  - Optimized Toolchains
  - Source Level Debugger
  - Profiling Analysis
  - Extensive Demo Projects
  - Flash ISP - configured via GUI

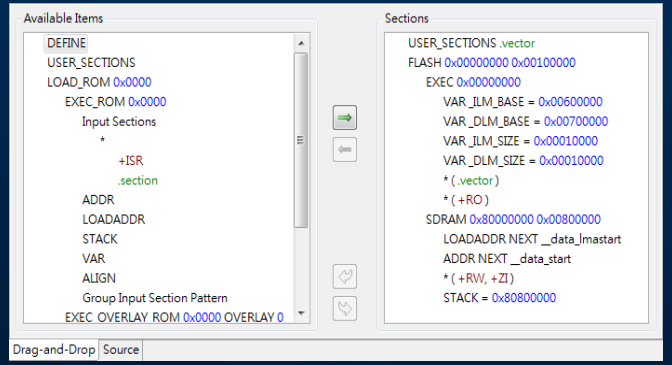


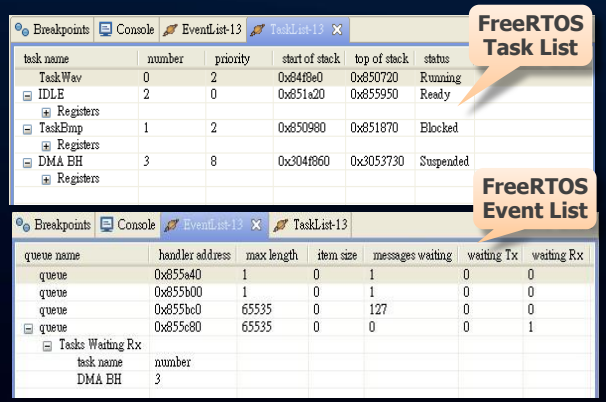
AndeSight™: Professional IDE

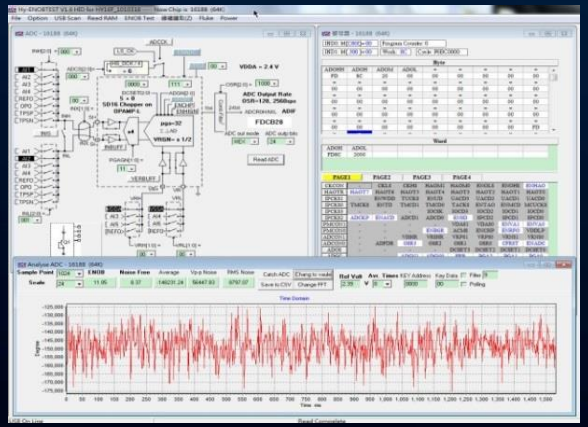
- Eclipse-based, enriched by 15-year effort

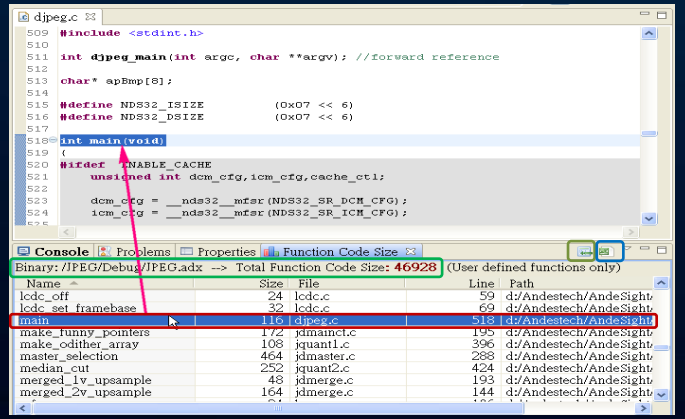










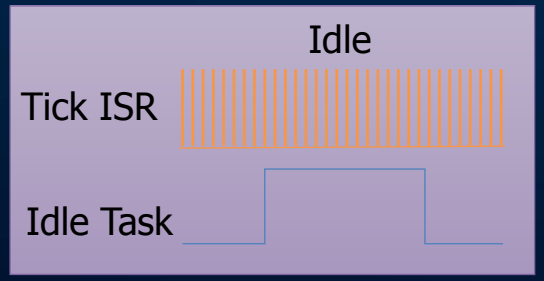


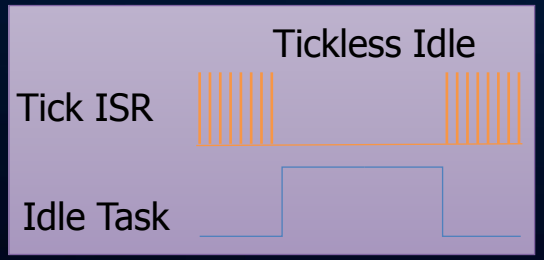
AndeSoft™: Bare Metal Support

- **Bare metal**
  - **Rich startup demo projects for Andes-specific features**
    - PLIC, CLIC
    - MMU, PMP, cache, ECC, bus matrix slave port
    - PowerBrake, hibernate, WFI CPU standby/resume
    - StackSafe™, performance monitor
    - DSP, printf UART redirect, C++ programming
  - **AMSI (Andes MCU Software Interface) driver APIs**
    - UART, GPIO, RTC, PWM, QSPI, I2C and WDT
  - **Easy to use and catch up**

AndeSoft™: RTOS Support

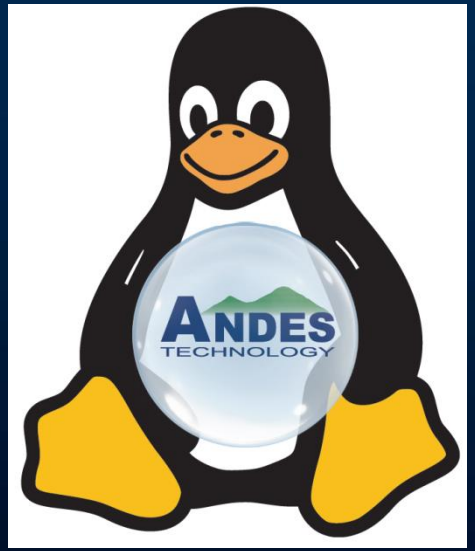
- **RTOS**
  - **FreeRTOS** (open source): 32/64 bits
  - **ThreadX** (from Express Logic): 32/64 bits
  - RISC-V ready: **Zephyr**, **RT-Thread**, SylixOS, µC/OS-[II/III], MyNewt, LiteOS, AliOS Things
- **FreeRTOS v10.0**
  - FreeRTOS test suite verified
  - Support AE350 (AXI/AHB) platform
  - Tickless idle
    - Reduce power consumption by stopping periodic tick interrupt in the idle mode
    - Based on RISC-V standard mtime/mtimecmp
  - RTOS-awareness debugging
    - AndeSight™
    - Lauterbach's Trace32®





AndeSoft™: Linux Support

- **Linux kernel:**
  - LTS 32/64 bits kernel : since 4.17
  - SMP support
  - Cache coherence and cache non-coherence support
  - Linux Test Projects (LTP) verified
  - Device drivers for AE350 platform
- **U-Boot**
  - RV32/RV64 port, maintainer and major contributor
  - SMP support
  - Supervisor mode support
  - Device drivers for AE350 platform
- **BBL**



AndeSoft™: Linux Support

- **Linux distribution:**
  - Fedora port ready
  - OpenWRT port for networking
- **Linux kernel tools**
  - strace/ftrace for developers to debug
  - Perf to evaluate the bottleneck of the whole system
  - Power management
    - Suspend2ram: suspended by sysfs and wakeup by RTC and UART interrupt
    - PowerBrake: power throttling mechanism controlled by sysfs
  - Kernel module support all relocation types for RV32 and RV64
- **Development tools:**
  - Linux awareness debugging
    - Lauterbach Trace32®

Open Source Contributions

- **Major contributor, some as maintainers**
- **GCC/Binutils**
  - RV32IE
  - Interrupt attribute
  - ELF attribute support
- **LLVM/LLD**
  - RV[32|64]IMAFDC code gen
  - Hard-float calling convention.
- **Debugging tools: GDB, OpenOCD**
- **Linux**
  - ftrace, Perf, kernel module, non-coherent support
  - Fedora port
- **u-Boot**
- **C library**
  - Glibc, RV32
  - Newlib

```
[root@fedora-riscv ~]# cat /proc/cpuinfo
hart     : 0
isa      : rv64i2p0m2p0a2p0f2p0d2p0c2p0xv5-0p0
mmu      : sv39

[root@fedora-riscv ~]# uname -a
Linux fedora-riscv 4.17.0-00250-gd63b2bc-dirty #4 PREEMPT
[root@fedora-riscv ~]#
```

Why Andes for RISC-V

Your Trusted RISC-V CPU Vendor

- Leading Commercial RISC-V CPU company
- CPU IPO company with 15-year history
- 350+ customers worldwide
- + 5 Bn shipping record
- Profession FAE team and support system
- Better code size and performance, mature tool

Thank You