Expanding the RISC-V Horizon and Beyond

Samuel Chiang
Deputy Technical Marketing Director
Andes Technology

Feb-22, 2023
Andes Technology Corporation

Who We Are

- **CPU**
  - Pure-play CPU *IP Vendor*
  - 18-year-old Public Company
  - Active Open-Source Contributor/Maintainer

Roles in RISC-V International (RVI)

- Founding & Premier Member
  - Frankwell Lin
    - Director of the Board
  - Charlie Su
    - Technical Steering Committee
  - Florian Wohlrab
    - Ambassador

Quick Facts

- **5th gen**
  - *AndeStar™ Architecture*
- **400** Employees, 80% R&D
- **300+** Worldwide Licensees
- **87K+** AndeSight IDE installations
- **12Bn+** Total shipment of Andes-Embedded™ SoC
RISC-V Is Everywhere – using Andes customers as examples

From the Edge, To the Cloud, Into the Space
AndesCore™ Lineup with Industry’s 1st RISC-V Cores

- D25F: with **SIMD/DSP capability** (P-extension, 32/64 bits)
- NX27V: with **Vector Processing Unit** (V-extension, up to 512 bits)
- N25F-SE: with ISO 26262 Full Compliance, not just Ready

<table>
<thead>
<tr>
<th>Categories</th>
<th>Embedded Control</th>
<th>DSP/Vector</th>
<th>Linux AP</th>
<th>FUSA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Entry Series</td>
<td>N22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>27 Series</td>
<td>NX27V</td>
<td></td>
<td>A27(L2)</td>
<td>AX27(L2)</td>
</tr>
<tr>
<td>45 Series</td>
<td>N45, NX45</td>
<td>D45</td>
<td>A45(MP)</td>
<td>AX45(MP)</td>
</tr>
</tbody>
</table>

References
- A53/55, R52/82, M7
- A5/7/35
- A5/7/35, R4/5, M4/33
- M0/0+/3/33/4
AndesCore™ Roadmap Processors

<table>
<thead>
<tr>
<th>AX60 Series</th>
<th>AX65</th>
<th>AX67</th>
<th>60-SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>13-stage OOO MP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Categories</td>
<td>Power-efficient</td>
<td>Mid-range</td>
<td>Extended</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AX45 Series</th>
<th>AX45MPV</th>
<th>45-SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-stage Superscalar</td>
<td>N45, NX45</td>
<td></td>
</tr>
<tr>
<td>Categories</td>
<td>Power-efficient</td>
<td>Mid-range</td>
</tr>
</tbody>
</table>

| AX27 Series | AX27(L2), AX27(L2) | |
|-------------|---------------------||
| 5-stage MemBoost | NX27V | |
| Categories | Power-efficient | Mid-range | Extended | FUSA |

| AX25 Series | AX25(MP), AX25(MP) | |
|-------------|---------------------||
| 5-stage Fast&Compact | N25F, NX25F | |
| Categories | Power-efficient | Mid-range | Extended | FUSA |

| AX22 Series | AX22(MP) | |
|-------------|---------||
| 5-stage Embedded | N22 | |
| Categories | Power-efficient | Mid-range | Extended | FUSA |

New Processors: AX65, AX45MPV, D23, D25F-SE

Safety Enhanced (SE) Series: at least one per year

References:
- A72~A76; N1/V1
- A53/55, R52/82, M7
- A5/7/35
- A5/7/35, R4/5, M4/33
- M0/0+/3/33/4

Note *: AX45MPV configured as one core
AndesCore™ AX65

Multicore Out-of-Order Superscalar Processor
The Andes AX60 Processor Series

A new generation of AndesCore™
- Advanced Performance 13-stage Out-of-Order Superscalar Multicore
- Latest RISC-V Architecture
- Supported by Andes Long-term Roadmap
  - AX65 as the first member of the AX60 series
  - More products based on the AX60 micro-architecture planned, including for automotive functional safety

AndesCore™ AX65
- Offering performance surpassing CA72
- > 2.5 GHz, > 2x per-GHz performance of AX45MP
- Engaging with early customers
AndesCore AX65: 1st Member of AX60-Series

- 64-bit, RV64GCBK
- 8-core Multiprocessor
- 13-stage OoO Pipeline
- 128-entry Reorder Buffer (ROB)
- 4-wide Frontend Decoder
- 8 Execution Pipeline engines
- 2-level Branch Target Buffer (BTB)
- TAGE-L Branch Predictor
- 1024-entry 4-way L2 TLBs
- 64 KB, 4-way Private I/D Caches
- 8 MB, 16-way Shared Cache
- 256-bit AXI4, MMIO and IOCP Buses

AX65 Multicore

- AX65core0
  - Private $0
- AX65core7
  - Private $7

Interrupt Controller

Debug Support

Coherence Manager (CM)

Shared Cache

MMIO

Memory

Coherent IO

IrQ’s

JTAG

Trace Ports

batch, fetch, align & buffer

decode, rename, dispatch

issue, register read

+br & misc

memory

floating point

WB

x3

x1

x2

x2

issue,

register

read
Preliminary Performance Results

<table>
<thead>
<tr>
<th>AndesCore</th>
<th>AX27L2</th>
<th>AX45MP (over AX27L2)</th>
<th>AX65 (over AX45MP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro-architecture</td>
<td>5 stage scalar in-order</td>
<td>8 stage dual-issue in-order</td>
<td>13 stage quad-issue OOO</td>
</tr>
<tr>
<td>Freq. (7nm)</td>
<td>~2 GHz</td>
<td>&gt;2 GHz</td>
<td>&gt;2.5 GHz</td>
</tr>
<tr>
<td>Coremark/MHz</td>
<td>3.55</td>
<td>5.64 (+59%)</td>
<td>9.17 (+63%)</td>
</tr>
<tr>
<td>Specint2k6/GHz</td>
<td>2.82</td>
<td>3.46 (+23%)</td>
<td>&gt; 7 (&gt;2x, target)</td>
</tr>
<tr>
<td>EEMBC FPMark/MHz</td>
<td>27.0</td>
<td>35.2 (+30%)</td>
<td>66.6 (+89%)</td>
</tr>
<tr>
<td>Linpack MFLOPS/MHz</td>
<td>0.130</td>
<td>0.220 (+69%)</td>
<td>0.613 (2.8x)</td>
</tr>
<tr>
<td>Mem Bandwidth(^1)/MHz</td>
<td>1.0x</td>
<td>1.47x</td>
<td>1.90x</td>
</tr>
</tbody>
</table>

1. Based on standard library memcpy
AndesCore™ AX45MPV
Multicore 1024-bit Vector Processor
AX45MPV: Linux Multicore Vector Processor

- A new member of popular AndesCore™ 45-series processors
  - Inherits all features of AX45MP and leverages 3+ years of field experience from NX27V vector engine
  - 64-bit 8-stage dual-issue processor
  - Up to 8 cores SMP supporting up to 8MB L2 cache
  - Dual-issue 1024-bit Vector Processing Unit (VPU) delivers up to 6 results per cycle

- AndesCore™ AX45MPV
  - Targets AI inference/training, ADAS, AR/VR, computer vision, multimedia
  - Engaging with early customers
AX45MPV: Core and Multicore Cluster

- **ISA:** RV64GCBP* + V
- **8-stage In-order dual-issue**
- **Scalar Unit:** configurable
  - MMU/SV48, M/S/U modes
  - FPU, DSP
  - I/D caches: 8K~64KB; Parity (I$) or ECC (both)
  - I/D LM: 0~16MB, dynamic wait-cycle, and ECC
  - Andes Custom Extension™ (ACE)
- **CM/L2$ subsystem**
  - 32KB to 8MB, 64B line, 16-way
  - Multi-cycle support for high-density SRAMs
  - Instruction/data prefetch, up to 64 outstanding requests
- **AXI Bus Interfaces**
  - Bus clock: N-to-1 or asynchronous
  - Width: 128/256/512 bits except 64-bit SPP

*P (draft)
AX45MPV: 1024-bit VPU

- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, bf16
  - VLEN/DLEN: 128~1024 bits, 1:1 or 2:1 ratio
  - Up to 5 DLEN results per cycle (6 with FMAC2)

- **Vector pipeline**
  - Up to 2 RVV instructions/cycle can enter VIQ in EX
  - Most functional Units are pipelined and chainable
    - INT: ALU, MUL/DIV, Permute
    - FP: FMAC1, FMAC2, FMISC
    - Others: LDST, ACE

- **ACE enables flexible compute and comm. to HWE**
  - Andes Streaming Port™ (ASP)
  - ACE-RVV: custom RVV instructions performed inside VPU

- **Performance Comparison with NX27V (when VLEN/DLEN are the same)**
  - Compute-bound loop: 20%~40% faster
  - Memory-bound loop: 30~50% faster
AndesCore™ D25F-SE / N25F-SE
Automotive Functional Safety (FUSA)
Andes is Driving Innovations in Automotive

with Industry’s 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar

CMOS Sensor

Auto TDDI

Auto MCU

Auto Storage
N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor

- ISO 26262 Certification for Development Process: ASIL-D
  - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- ISO-9001 QMS achieved and maintained since 2010
- ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE
  - ISO 26262-2, 4, 5, 8, 9
  - Covers all the sections applicable to CPU core
D25F-SE: FuSa processor with DSP/SIMD capability

CPU Core
- AndeStar™ V5 Instruction Set Architecture (ISA)
  - RISC-V 32-bit, RV32GC + Andes Extensions
  - RISC-V P(draft) and B extensions.
  - Machine+User (M+U) privilege levels
- Dynamic branch prediction with BTB, BHT, RAS
- CoDense™ code size reduction, StackSafe™ stack protection

Memory Subsystem
- Support I/D cache up to 32KB each
- Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses

Bus Interfaces
- AXI or AHB bus master port
- N:1 CPU clock vs. bus clock ratio

Others
- Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface

Safety Package including Safety Manual & FMEDA report
D25F-SE with DSP and Bit-manipulation

- **RVP**: Powerful DSP/SIMD instructions for audio/voice codec and endpoint AI/ML
- SIMD instructions such as a quad 8 x 8 accumulated into 32-bit data
- DSP library support of over 320 functions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Speedup of RVP over Baseline²</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP3 decoder</td>
<td>2.0x</td>
</tr>
<tr>
<td>AMR-WB voice codec</td>
<td>3.8x</td>
</tr>
<tr>
<td>EVS codec</td>
<td>4.8x</td>
</tr>
<tr>
<td>LC3plus codec</td>
<td>5.5x</td>
</tr>
<tr>
<td>ML-KWS (Keyword Spotting)</td>
<td>8.9x</td>
</tr>
</tbody>
</table>

- **RVB**: Efficient bit-manipulation operations for codes such as cryptographic & checksums
  - Latest RVB ISA-extension Ver 1.0.0, including:
    - address generation, basic bit-manipulation, carry-less multiplication and single-bit instructions
    - Accelerate Crypto calculations: 27% improvement on SHA256, 19% for AES, 16% for MD5
AndesCore™ D23
Compact, Secure, Low-Power Controller
D23: Compact, Secure Processor with Optional DSP

**ISA**
- Compliant with RISC-V GCBP, K (Scalar Crypto), CMO, Zce extensions
- Security - ePMP, sPMP, Programmable PMA, secure debug
- AndeStar V5 ISA extension - StackSafe™, CoDense™, PowerBrake, WFI/WFE
- Andes Custom Extension™ (ACE) support

**32-bit 3-stage pipeline CPU, some dual issue capability**
- Max freq: up to 800MHz (28nm), Gate count: <50K (for min. useful configuration)
- >4.1 Coremark/MHz and >2.0 DMIPS/MHz

**Configurable options**
- I & D Caches (up to 32KB) and local memories (up to 512MB)
- Memory soft error protection by parity or ECC
- Static or Dynamic branch prediction
- Multiplier optimized for performance or area

**SoC integration support**
- 4-wire JTAG or 2-wire serial debug; RISC-V Processor Trace v1.0
- Integrated Peripheral: Machine Timer + Debug Module
- CLIC and PLIC for interrupt handling

---

Andes Technology
Subject to change without notice
Copyright© 2021-2023 Andes Technology
Taking RISC-V® Mainstream

---

[Image of diagram showing processor components such asInterrupts, PMU, Debug Trace, CLIC, WFI/WFE, Debug & Trace I/F, 3-stage uCore, ePMP/sPMP/PMA, Timer, DSP, FPU, ACE, I$, Multiplier/Divider, DS, ILM, Br. Pred, DLM, LM Access Port, System Port, Peripheral Port, Lcw Latency Port, AHB-L, AHB-L, APB, AHB-L]
D23 Targets Diverse Embedded & IoT Applications

<table>
<thead>
<tr>
<th>Applications</th>
<th>D23 Capability fit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDI, TDDI</td>
<td>Small gate count</td>
</tr>
<tr>
<td>Wireless controller core</td>
<td>Security, small gate count</td>
</tr>
<tr>
<td>(WiFi, BT or others)</td>
<td></td>
</tr>
<tr>
<td>Smart Home Appliance</td>
<td>Security, performance, small gate count</td>
</tr>
<tr>
<td>Wearable</td>
<td>DSP (Edge AI), Security</td>
</tr>
<tr>
<td>E-Toys</td>
<td>DSP (Speech and Sound Processing)</td>
</tr>
<tr>
<td>RF Sensor control</td>
<td>DSP (Edge AI, Front-End Signal/Protocol Stack Processing)</td>
</tr>
<tr>
<td>MEMS/Sensor Fusion</td>
<td>DSP (Edge AI, Front-End Signal processing)</td>
</tr>
<tr>
<td>Battery or charging control</td>
<td>Performance</td>
</tr>
<tr>
<td>Advanced Motor Control</td>
<td>DSP</td>
</tr>
</tbody>
</table>
Expanding RISC-V Beyond the Horizon

- RISC-V is a leading choice of processors for SoCs and Computing Platforms
- Andes accelerates to bring to market more quality RISC-V solutions

<table>
<thead>
<tr>
<th>AX65</th>
<th>AX45MPV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multicore</td>
<td>Multicore</td>
</tr>
<tr>
<td>Out-Of-Order</td>
<td>1024-bit Vector</td>
</tr>
<tr>
<td>Application</td>
<td>Processor</td>
</tr>
<tr>
<td>Processor</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>D23</th>
<th>D25F-SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tiny and Secure</td>
<td>ISO 26262</td>
</tr>
<tr>
<td>Processor</td>
<td>Fully-Compliant</td>
</tr>
<tr>
<td></td>
<td>Processor</td>
</tr>
</tbody>
</table>

- Andes CPU cores, Tools and SW and partners are best to help customers succeed

~18 years, 300+ customers, 87K+ IDE users, 12B+ customers’ SoC
Thank You!
sales@andestech.com