Expanding the RISC-V Horizon and Beyond

Samuel Chiang
Deputy Technical Marketing Director
Andes Technology

Feb-22, 2023

Andes Technology Corporation

Who We Are

Pure-play CPU **IP Vendor**

18-year-old
Public Company

Active Open-Source Contributor/Maintainer

Hsinchu, TW (HQ)

Roles in RISC-V International (RVI)

Founding & Premier Member

Frankwell Lin
Director of the Board

Charlie Su
Technical Steering Committee

Florian Wohlrab
Ambassador

P-Extension TG

IOPMP TG

Fast Intr. TG

Quick Facts

5th gen
AndeStar™ Architecture

400
Employees, 80% R&D

300+
Worldwide Licensees

87K+
AndeSight IDE installations

12Bn+
Total shipment of Andes-Embedded™ SoC

RISC-V Is Everywhere – using Andes customers as examples

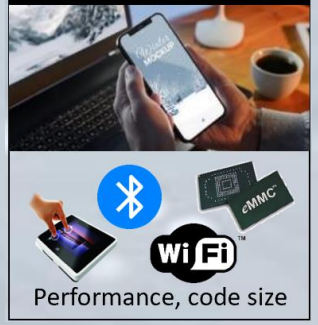
MPU/MCU/AIoT

D25F, D45, AX25MP, AX45MP

Storage

N25F, N45, AX45MP

Mobile



N25F, N45

From the Edge, To the Cloud, Into the Space

Cloud AI

NX27V, AX25, AX27, AX45MP, AX45MPV

Above Cloud

N25F

5G Networks

N25F, A25, A45MP, AX45MP

AndesCore™ Lineup with Industry's 1st RISC-V Cores

- **D25F:** with **SIMD/DSP capability** (P-extension, 32/64 bits)
- **NX27V:** with **Vector Processing Unit** (V-extension, up to 512 bits)
- **N25F-SE:** with **ISO 26262 Full Compliance**, not just *Ready*

45 Series 8-stage superscalar	N45, NX45	D45	A45(MP) AX45(MP)		A53/55, R52/82, M7
27 Series 5-stage MemBoost		**NX27V**	A27(L2) AX27(L2)		A5/7/35
25 Series 5-stage fast & compact	N25F, NX25F	**D25F**	A25(MP) AX25(MP)	**N25F-SE**	A5/7/35, R4/5, M4/33
Entry Series	N22				M0/0+/3/33/4
Categories	*Embedded Control*	*DSP/Vector*	*Linux AP*	*FUSA*	*References*

AndesCore™ Roadmap Processors

AX60 Series 13-stage OOO MP		AX65	AX67	60-SE	A72~A76; N1/V1
Categories	*Power-efficient*	*Mid-range*	*Extended*	***FUSA***	
45 Series 8-stage Superscalar	N45, NX45	NX45V* D45	AX45MPV A45(MP), AX45(MP)	45-SE	A53/55, R52/82, M7
27 Series 5-stage MemBoost		**NX27V**	A27(L2), AX27(L2)		A5/7/35
25 Series 5-stage Fast&Compact	N25F, NX25F	**D25F**	A25(MP), AX25(MP)	D25F-SE^{B} N25F-SE^{B}	A5/7/35, R4/5, M4/33
Entry Series	N22	D23		23-SE	M0/0+/3/33/4
Categories	*Embedded Control*	*DSP/Vector*	*Linux AP*	*FUSA*	*References*

*Note *: AX45MPV configured as one core*

- **New Processors:** AX65, AX45MPV, D23, D25F-SE
- **Safety Enhanced (SE) Series:** at least one per year

AndesCore™ AX65

Multicore Out-of-Order Superscalar Processor

The Andes AX60 Processor Series

A new generation of AndesCore™

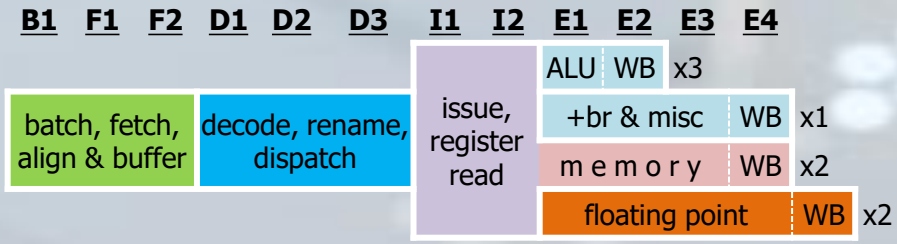
- Advanced Performance 13-stage Out-of-Order Superscalar Multicore
- Latest RISC-V Architecture
- Supported by Andes Long-term Roadmap
  - AX65 as the first member of the AX60 series
  - More products based on the AX60 micro-architecture planned, including for automotive functional safety

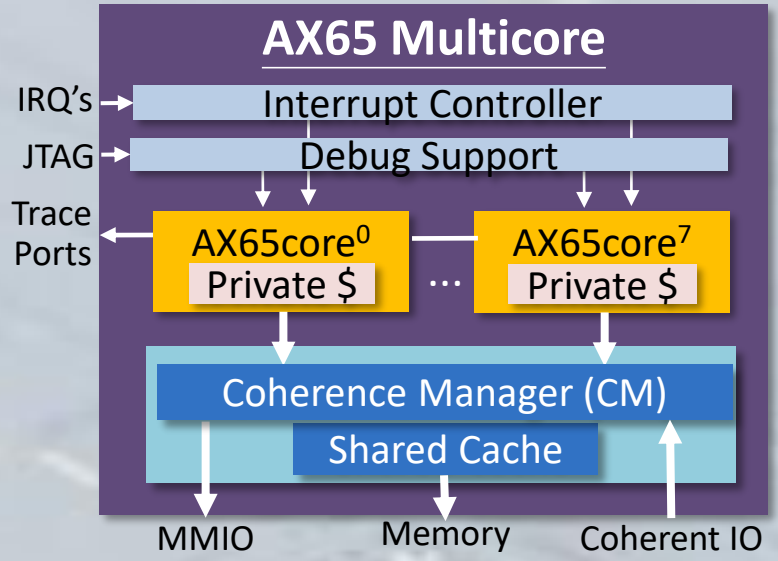
AndesCore™ AX65

- Offering performance surpassing CA72
- > 2.5 GHz, > 2x per-GHz performance of AX45MP
- Engaging with early customers

AndesCore AX65: 1st Member of AX60-Series

- 64-bit, RV64GCBK
- 8-core Multiprocessor
- 13-stage OoO Pipeline
- 128-entry Reorder Buffer (ROB)
- 4-wide Frontend Decoder
- 8 Execution Pipeline engines
- 2-level Branch Target Buffer (BTB)
- TAGE-L Branch Predictor
- 1024-entry 4-way L2 TLBs
- 64 KB, 4-way Private I/D Caches
- 8 MB, 16-way Shared Cache
- 256-bit AXI4, MMIO and IOCP Buses





Preliminary Performance Results

AndesCore	AX27L2	AX45MP (over AX27L2)	AX65 (over AX45MP)
Micro-architecture	5 stage scalar in-order	8 stage dual-issue in-order	13 stage quad-issue OOO
Freq. (7nm)	~2 GHz	>2 GHz	>2.5 GHz
Coremark/MHz	3.55	5.64 (+59%)	9.17 (+63%)
Specint2k6/GHz	2.82	3.46 (+23%)	> 7 (>2x, target)
EEMBC FPMark/MHz	27.0	35.2 (+30%)	66.6 (+89%)
Linpack MFLOPS/MHz	0.130	0.220 (+69%)	0.613 (2.8x)
Mem Bandwidth[1]/MHz	1.0x	1.47x	1.90x

1. Based on standard library memcpy

AndesCore™ AX45MPV

Multicore 1024-bit Vector Processor

AX45MPV: Linux Multicore Vector Processor

A new member of popular AndesCore™ 45-series processors

- Inherits all features of AX45MP and leverages 3+ years of field experience from NX27V vector engine
- 64-bit 8-stage dual-issue processor
- Up to 8 cores SMP supporting up to 8MB L2 cache
- Dual-issue 1024-bit Vector Processing Unit (VPU) delivers up to 6 results per cycle

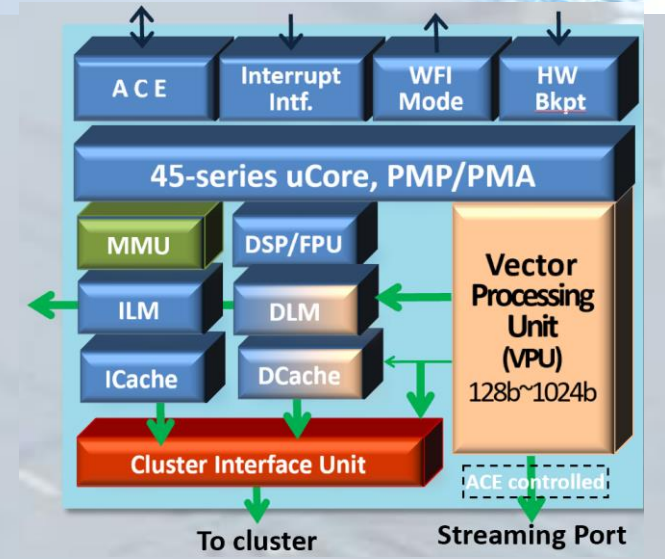
AndesCore™ AX45MPV

- Targets AI inference/training, ADAS, AR/VR, computer vision, multimedia
- Engaging with early customers

AX45MPV: Core and Multicore Cluster

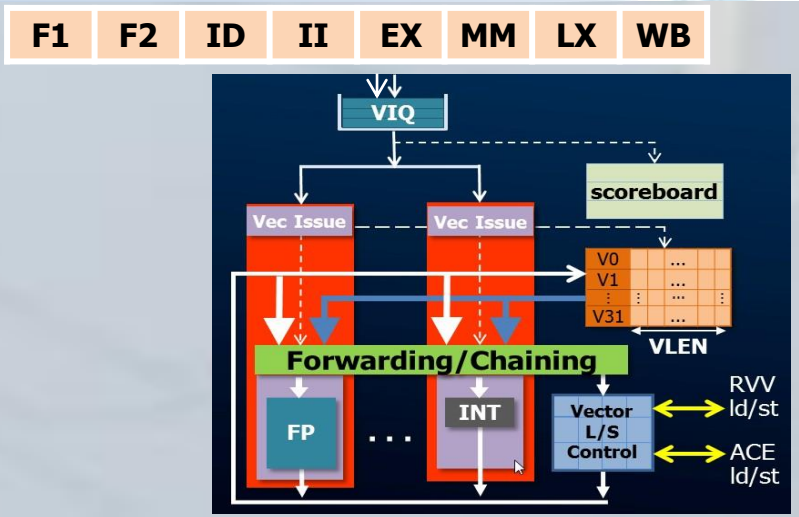
- **ISA: RV64GCBP* + V**
- **8-stage In-order dual-issue**
- **Scalar Unit: configurable**
  - MMU/SV48, M/S/U modes
  - FPU, DSP
  - I/D caches: 8K~64KB; Parity (I$) or ECC (both)
  - I/D LM: 0~16MB, dynamic wait-cycle, and ECC
  - Andes Custom Extension™ (ACE)
- **CM/L2$ subsystem**
  - 32KB to 8MB, 64B line, 16-way
  - Multi-cycle support for high-density SRAMs
  - Instruction/data prefetch, up to 64 outstanding requests
- **AXI Bus Interfaces**
  - Bus clock: N-to-1 or asynchronous
  - Width: 128/256/512 bits except 64-bit SPP

* P (draft)

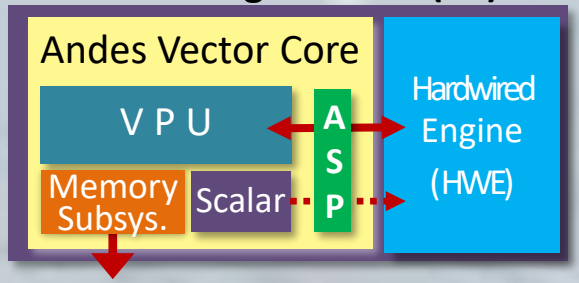


AX45MPV: 1024-bit VPU

- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, bf16
  - VLEN/DLEN: 128~1024 bits, 1:1 or 2:1 ratio
  - Up to 5 DLEN results per cycle (6 with FMAC2)
- **Vector pipeline**
  - Up to 2 RVV instructions/cycle can enter VIQ in EX
  - Most functional Units are pipelined and chainable
    - INT: ALU, MUL/DIV, Permute
    - FP: FMAC1, FMAC2, FMISC
    - Others: LDST, ACE-RVV
- **ACE enables flexible compute and comm. to HWE**
  - Andes Streaming Port™ (ASP)
  - ACE-RVV: custom RVV instructions performed inside VPU
- **Performance Comparison with NX27V (when VLEN/DLEN are the same)**
  - Compute-bound loop: 20%~40% faster
  - Memory-bound loop: 30~50% faster



Processing Element (PE)



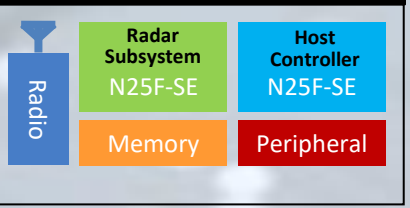
AndesCore™ D25F-SE / N25F-SE

Automotive Functional Safety(FUSA)

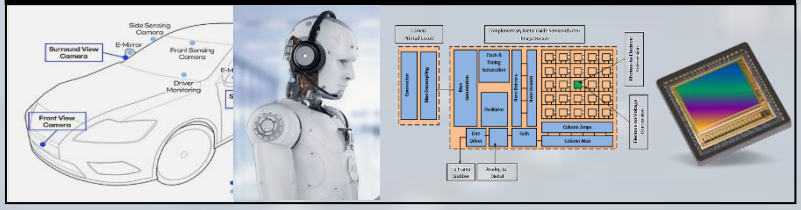
Andes is *Driving* Innovations in Automotive

with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

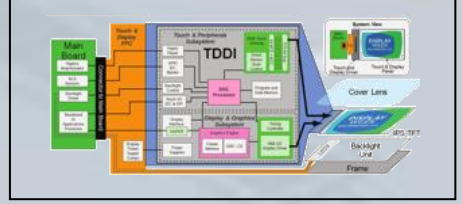
In-Cabin Radar



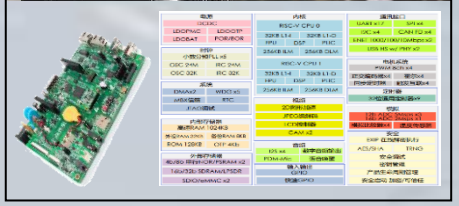
CMOS Sensor



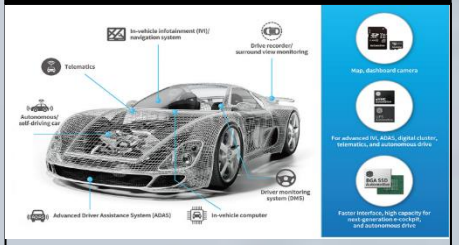
Auto TDDI

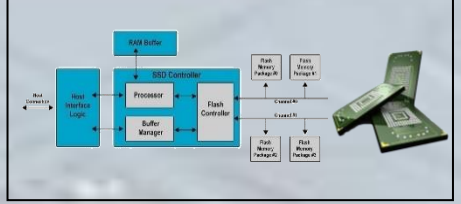


Auto MCU



Auto Storage





N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/20/0639 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY
TAIWAN R.O.C 30069

Project-No/-ID	LICENSED TEST MARK	Report No.
P30L	SGS TÜV SAAR FUNCTIONAL SAFETY APPROVED	P30L0001

Tested according to	ISO 26262:2018
Certified Process	Development process for Functional Safety related components up to ASIL D Version V1.0/202011
Technical Data/Parameter	The audited development process complies with the ISO 26262 standard part requirements

ISO 26262-2:2018 ISO 26262-6:2018
ISO 26262-4:2018 ISO 26262-8:2018
ISO 26262-5:2018 ISO 26262-9:2018

Specific Requirements	The certificate is created for the purpose of providing conformity of the development and support process in accordance with ISO 26262. Changes which are not covered in the Audit Report have to be reconsidered.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

Munich, December 22nd, 2020

Marcus Rau

The test mark regulation is an integral part of this certificate.

SGS-TÜV Saar GmbH, Hohenzollernstr. 59, D-81379 München, Deutschland / Germany
Website: www.sgs-tuv-saar.com/fs E-Mail: fs@sgs.com

CERTIFICATE

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID	LICENSED TEST MARK	Report No.
S280	SGS TÜV SAAR ASIL B COMPLIANT Functional Safety ISO 26262 www.sgs-tuv-saar.com	S2800001

Tested according to	ISO 26262:2018 (Parts 2, 4 partly, 5, 8, 9)
Certified Product(s)	CPU IP "N25F-SE" Version: R320
Technical Data/Parameter	The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance **with ASIL B** requirements.
Specific Requirements	The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval. The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

Munich, October 28th, 2022

Marcus Rau

The validation status is documented via SGS Certification Database

The test mark regulation is an integral part of this certificate.

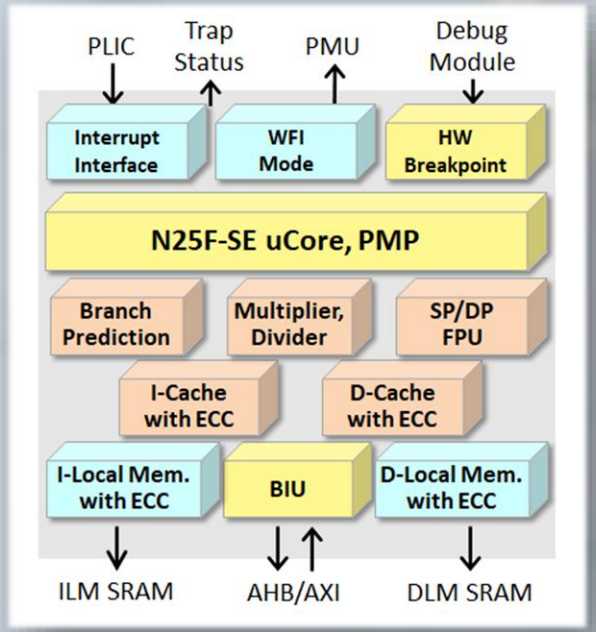
SGS-TÜV Saar GmbH, Hohenzollernstr. 59, D-81379 München, Deutschland / Germany
Website: www.sgs-tuv-saar.com/fs E-Mail: fs@sgs.com

CERTIFICATE

- **ISO 26262 Certification for Development Process: ASIL-D**
  - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- **ISO-9001 QMS achieved and maintained since 2010**
- **ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE**
  - ISO 26262-2,4,5,8,9
  - Covers all the sections applicable to CPU core

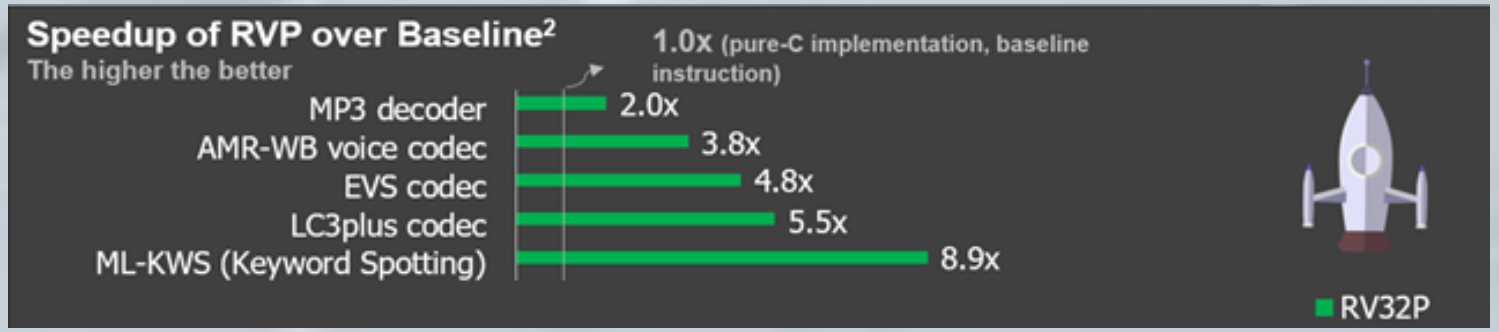
D25F-SE: FuSa processor with DSP/SIMD capability

- **CPU Core**
  - AndeStar™ V5 Instruction Set Architecture (ISA)
    - RISC-V 32-bit, RV32GC + Andes Extensions
    - RISC-V P(draft) and B extensions.
    - Machine+User (M+U) privilege levels
  - Dynamic branch prediction with BTB, BHT, RAS
  - CoDense™ code size reduction, StackSafe™ stack protection
- **Memory Subsystem**
  - Support I/D cache up to 32KB each
  - Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses
- **Bus Interfaces**
  - AXI or AHB bus master port
  - N:1 CPU clock vs. bus clock ratio
- **Others**
  - Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface
- **Safety Package including Safety Manual & FMEDA report**



D25F-SE with DSP and Bit-manipulation

- **RVP: Powerful DSP/SIMD instructions for audio/voice codec and endpoint AI/ML**
- **SIMD instructions such as a quad 8 x 8 accumulated into 32-bit data**
- **DSP library support of over 320 functions**



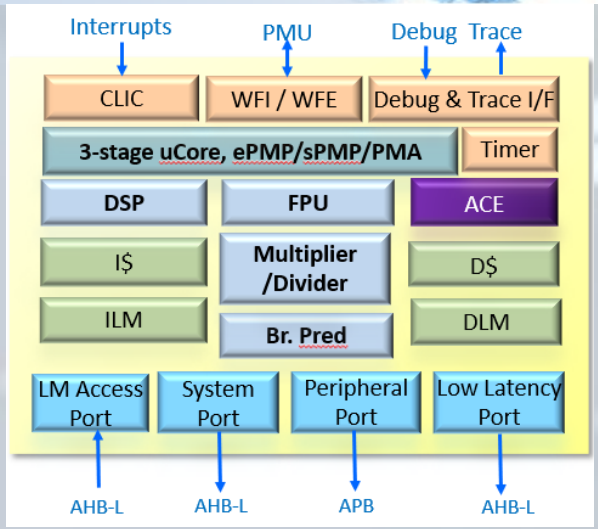
- **RVB: Efficient bit-manipulation operations for codes such as cryptographic & checksums**
  - Latest RVB ISA-extension Ver 1.0.0, including:
    - address generation, basic bit-manipulation, carry-less multiplication and single-bit instructions
    - Accelerate Crypto calculations: **27%** improvement on SHA256, **19%** for AES, **16%** for MD5

AndesCore™ D23

Compact, Secure, Low-Power Controller

D23: Compact, Secure Processor with Optional DSP

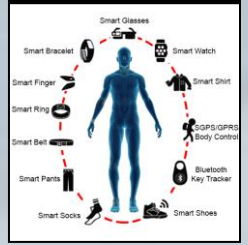
- **ISA**
  - Compliant with RISC-V GCBP, K (Scalar Crypto), CMO, Zce extensions
  - Security - ePMP, sPMP, Programmable PMA, secure debug
  - AndeStar V5 ISA extension - StackSafe™, CoDense™, PowerBrake, WFI/WFE
  - Andes Custom Extension™ (ACE) support
- **32-bit 3-stage pipeline CPU, some dual issue capability**
  - Max freq: up to 800MHz (28nm), Gate count: <50K (for min. useful configuration)
  - >4.1 Coremark/MHz and >2.0 DMIPS/MHz
- **Configurable options**
  - I & D Caches (up to 32KB) and local memories (up to 512MB)
  - Memory soft error protection by parity or ECC
  - Static or Dynamic branch prediction
  - Multiplier optimized for performance or area
- **SoC integration support**
  - 4-wire JTAG or 2-wire serial debug; RISC-V Processor Trace v1.0
  - Integrated Peripheral: Machine Timer + Debug Module
  - CLIC and PLIC for interrupt handling



D23 Targets Diverse Embedded & IoT Applications

DDI/TDDI

Wearable

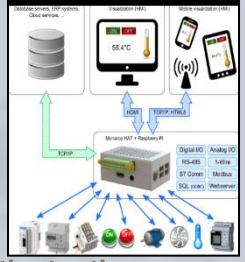


Smart Home

Motor Control

Connectivity

Embedded controller



Applications	D23 Capability fit
DDI, TDDI	Small gate count
Wireless controller core (WiFi, BT or others)	Security, small gate count
Smart Home Appliance	Security, performance, small gate count
Wearable	DSP (Edge AI), Security
E-Toys	DSP (Speech and Sound Processing)
RF Sensor control	DSP (Edge AI, Front-End Signal/Protocol Stack Processing)
MEMS/Sensor Fusion	DSP (Edge AI, Front-End Signal processing)
Battery or charging control	Performance
Advanced Motor Control	DSP

Expanding RISC-V Beyond the Horizon

- RISC-V is a leading choice of processors for SoCs and Computing Platforms
- Andes accelerates to bring to market more quality RISC-V solutions

AX65	AX45MPV
Multicore Out-Of-Order Application Processor	Multicore 1024-bit Vector Processor
D23	**D25F-SE**
Tiny and Secure Processor	ISO 26262 Fully-Compliant Processor

- Andes CPU cores, Tools and SW and partners are best to help customers succeed

Andes Embedded™

~18 years, 300+ customers, 87K+ IDE users, 12B+ customers' SoC

Thank You !

sales@andestech.com

ANDES
TECHNOLOGY