

# IAR Embedded Workbench for RISC-V

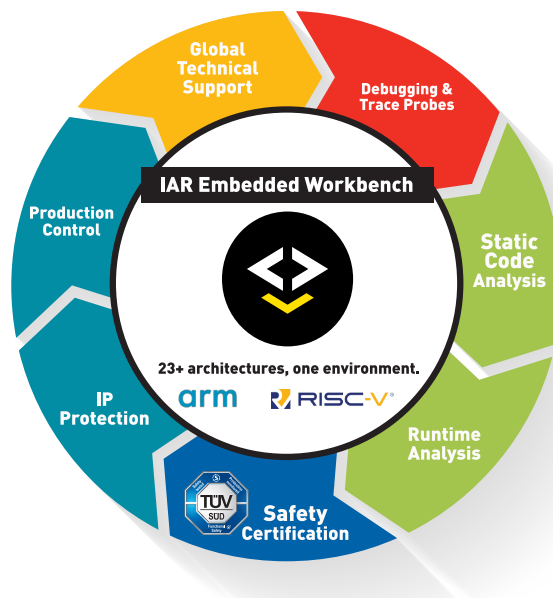
## Taking RISC-V to the next level!

As the leading commercial tools vendor for RISC-V, IAR Systems is able to provide stable and future-proof technology as well as global technical support. IAR Embedded Workbench for RISC-V is a complete toolchain offering excellent optimization technology to ensure developers that the application fits the required needs and optimizes the utilization of on-board memory and necessary speed. For safety-critical development, a functional safety edition of toolchain is available.

### What's included?

- Complete C/C++ compiler and debugger toolchain with integrated code analysis tools
- Outstanding performance through sophisticated optimization technology
- Extensive debugging capabilities through the state-of-the-art debugger C-SPY
- Integration with our feature-rich debugging probe I-jet
- Custom extensions support
- Stack protection
- User-friendly features for a streamlined workflow
- Support for the RV32I and RV32E base instruction sets and extensions such as M, A, F, D, C, P
- Easy-to-use example projects to get up and running on hardware in just a few minutes

### More than an ordinary toolbox.



### Future-proof tools in a fast-moving market

The RISC-V Foundation is moving fast with optional additions to the instruction set, debug and trace infrastructure and other aspects of the architecture. We have been part of the foundation since 2018, participating in selected working groups and committed to support standardized functionality relevant for embedded systems. Examples are 64-bit support and instruction set extensions V (vector) and B (bit manipulation), as well as additional debug and trace functionality.

We are continuously adding support for new devices and extensions in IAR Embedded Workbench for RISC-V. In addition, future releases will offer 64-bit support and security solutions.

# Powerful solutions for the RISC-V tools community

## Integrated static analysis

The static analysis tool C-STAT is integrated in IAR Embedded Workbench and helps to find potential issues in the code by doing an analysis on the source code level. C-STAT is covering the SEI CERT C Coding Standard, which provide rules for developing safe, reliable and secure systems in the C programming language. C-STAT also checks compliance with rules as defined by coding standards including MISRA C:2004, MISRA C++:2008 and MISRA C:2012, as well as hundreds of rules based on CWE (the Common Weakness Enumeration).

## Customized instructions

The standardized ability to extend the base instruction set with your own customized instructions is a prominent feature of the RISC-V instruction set. This ability can be used in innovative ways to tailor your own SoC design to specific workloads, to for example balance energy, speed and code size requirements. IAR Embedded Workbench for RISC-V lets you add support for such customized extensions in an easy and intuitive way.

## Functional safety and security

IAR Embedded Workbench for RISC-V is available in a functional safety edition, certified by TÜV SÜD according to the requirements of IEC 61508, ISO 26262, IEC 62304, EN 50128, EN 50657, IEC 60730, ISO 13849, IEC 62061, IEC 61511 and ISO 25119. The standardization of security features is an ongoing work in the RISC-V foundation and we are committed to supporting features relevant for embedded systems.

## Advanced debugging and trace capabilities

By making use of the advanced debugging tools, you can optimize the working time of your team when investigating issues and testing your application. The modern I-jet debug probe facilitates surprisingly advanced visualization of the application behavior.

In addition, the advanced I-jet Trace probe enables powerful code coverage and profiling data capabilities in IAR Embedded Workbench and traces every single executed instruction in your application. Many standards require code coverage and trace in order to prove that you have executed every line of code that is essential for the testing matrix.

The screenshot displays the IAR Embedded Workbench interface. The top window shows the source code for a Fibonacci sequence simulation. The middle window displays the assembly code for the same function, with instructions like 'c.jal', 'c.lui', and 'c.lui'. The bottom window shows a detailed execution trace with columns for Timestamp, Trace, Read Addr, Read Data, Write Addr, and Write Data. The trace shows the execution of instructions over time, with a focus on the 'DoforegroundProcess'.

## Professional technical support

We have global processes in place to ensure we deliver an efficient and smooth experience. With a Support and Update Agreement (SUA), you get access to technical support centers and customer care in multiple time zones globally, as well as the latest updates and features for your IAR Embedded Workbench license.