AndesCore™ NX27V Processor

64-bit CPU with RISC-V Vector Extension

Benefits

Performance

- AndeStar™ V5 Instruction Set Architecture (ISA), compliant to RISC-V technology
- Vector Processing Unit (VPU) boosts the performance of AI, AR/VR, computer vision, cryptography, and multimedia processing
- Separately licensable Andes Custom Extension™ (ACE) for customized acceleration
- 64-bit CPU architecture, enabling software to utilize the memory spaces far beyond 4G bytes imposed by 32-bit CPUs
- 16/32-bit mixable instruction format for compacting code density
- Branch predication to speed up control code
- Return Address Stack (RAS) to speed up procedure returns
- Physical Memory Protection (PMP) and Programmable Physical Memory Attributes (PMA)
- MemBoost for heavy memory transactions
- Flexibly configurable Platform-Level Interrupt Controller (PLIC) for supporting wide range of system event scenarios
- Enhancement of vectored interrupt handling for real-time performance
- Advanced CoDense™ technology to further reduce code size on top of “C” extension
- Up to 16 outstanding cached/uncached data accesses
- Large cache size support for vector performance enhancement

Flexibility

- Easy arrangement of preemptive interrupts
- StackSafe™ hardware to help measuring stack size, and detecting runtime overflow/underflow
- ECC or Parity check on level-one memories for fault protection
- Several configurations to tradeoff between core size and performance requirements

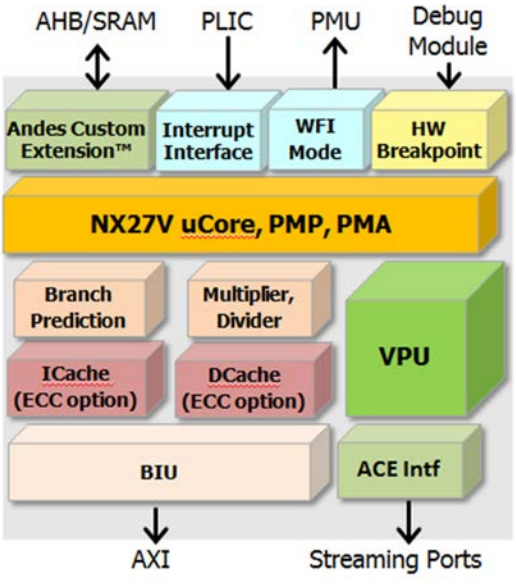
Power Management

- PowerBrake, QuickNap™ and WFI (Wait For

General Descriptions

The 64-bit NX27V is a vector processor with 5-stage scalar pipeline that supports the latest RISC-V specification, including the IMAFD standard instructions, “C” 16-bit compression instructions, “P” DSP extension instructions, “V” vector extension instructions and “N” for user-level interrupts. It brings enhanced performance in memory subsystem with higher memory bandwidth and memory latency reduction by supporting multiple outstanding data access. NX27V features branch prediction, instruction and data caches, local memories, ECC error protection, and Andes Custom Extension™ (ACE) to add proprietary instructions to accelerate performance/power consumption critical spots. It also includes vectored and preemptive interrupts to serve diversified system events. AXI data bus for wide data access, PowerBrake and WFI mode for rich power management, and JTAG debug interface and trace interface for software development support. NX27V contains a powerful Vector Processing Unit (VPU). It is ideal for applications with large arrays of data such as machine/deep learning, AR/VR, cryptography, multimedia processing, networking and scientific computing.

Functional Blocks



Key Features

CPU Core

- AndeStar™ V5 64-bit architecture
  - V5 state-of-the-art ISA. Little endian
  - RISC-V RV64GCNP support
  - RISC-V V-extension vector instructions with Andes extensions
  - Machine(M), User(U) privileges
- 5-stage pipeline with a full-cycle reserved for critical SRAM accesses
- PMP and PMA both up to 16 entries
- Multiplier options of pipelined 2-cycle multiplier or multiplier producing 1, 2, 4, or 8 bits per cycle
- Optional Dynamic Branch Prediction with
  - 32 to 256-entry Branch Target Buffer (BTB)
  - 256-entry Branch History Table (BHT)
  - 4-entry Return Address Stack (RAS)

Vector Processing Unit (VPU)

- Support RISC-V V-extension spec. Instructions including vector loads and stores, vector integer arithmetic, vector fixed-point, vector floating-point, vector reduction operations, vector mask, vector permutation, vector dot-product and Andes extended instructions for formats bfloat16 and int4.
- 32 vector registers
- Data formats:
  - SEW supported: int8, int16, int32, int64, fp16, fp32, fp64
  - Andes-extended formats: bfloat16 and int4
- Support LMUL 1, 2, 4, 8, 1/2, 1/4, 1/8
- Configurable VLEN, SIMD and Memory Width: combinations of 128-bit, 256-bit, 512-bit
- Functional units chainable, most fully pipelined
- Independent memory access paths for RVV load/store and ACE Streaming Port load/store

Memory Subsystem

- Instruction and Data Cache
  - Size separately configurable
    - I Cache: 8KB to 64KB
    - D Cache: 8KB to 512KB
  - 2-way (I Cache) or 4-way set associate (I & D-Cache)
  - Optional Parity or ECC (I Cache) error protection
- I/D prefetch
- Outstanding accesses
- Streaming Port: high performance data port for external coprocessor or intelligent memory

Bus Interfaces

- AXI bus with data width matching configurable
- Memory Width

Power Management

- PowerBrake technology to reduce peak power
- QuickNap™ for fast logic power-down and SRAM in retention
- WFI (Wait for Interrupt) instruction for software controlled stalls

Platform-Level Interrupt Controller (PLIC)

- Up to 1023 interrupt sources
- Up to 255 interrupt priority levels
- Up to 16 interrupt targets
- Enhanced Interrupt Features
  - Vectored interrupt dispatch
  - Priority-based preemption
  - Selectable edge trigger or level trigger

Trace Encoder Interface

- Support RISC-V Trace TG standard

External Debug Module

- JTAG debug interface with up to 8 triggers
- Exception redirection handling

Development Tools

- AndeSight™ IDE (Eclipse-based)
  - Compiler, Debugger, Profiler, Register Bit-field Display/Update, RTOS Awareness, and more
  - Tested platforms: Windows and Linux.
- Andes BSP
  - Vector Assembler and Debugger
  - Demo examples and sample projects
- RTOSes
  - Open-source: FreeRTOS, Zephyr, RT-Thread
  - Commercial: ThreadX, µC/OS-II
- COPILOT: Custom-OPtimized Instruction deveLOpment Tool for ACE (separately licensable)
- FPGA Development Boards
  - Support XILINX VCU118
- Debugging Hardware
  AICE-MICRO

Product Packages

- AndesCore™ NX27V Single Core Processor with AE350 Platform
  - Pre-integrated RTL with CPU subsystem (including PLIC, Timer and Debug Module) and AXI platform

AE350 Platform Pre-integrated with NX27V

Benefits

Convenience

- A rich collection of high-quality and configurable AXI/AHB/APB IPs required by most embedded systems
- Pre-integrated platform to jump-start designs
- System Management Unit as a reference for subsystem power management

Flexibility

- Scalability of AXI Bus Matrix and AHB/APB Bus Bridge to connect various AMBA components
- Configurable Platform-Level Interrupt Controller to simplify SoC integration

Efficiency

- Low latency level-one memories for best CPU performance
- Bus matrix to allow simultaneous transfers of independent transactions
- DMA controller for fast data movement without software's intervention
- System Management Unit for subsystem power management design reference

General Descriptions

The AE350 platform pre-integrated with NX27V CPU is a system design that serves various purposes such as to explore the product features, to evaluate the performance indexes and to determine the configuration options.

It is architected as the CPU/Local memories/Interrupt controller subsystem interfaced to AXI Bus Matrix and AHB/APB Bus Bridge with Platform IP components attached.

Design support includes such as scripts and test cases for integration, simulation, emulation and prototyping. This pre-integrated platform is ideal for minimizing development efforts by providing a verified reference which is both performance optimized and feature ready for majority of the embedded applications.

Platform IP Components

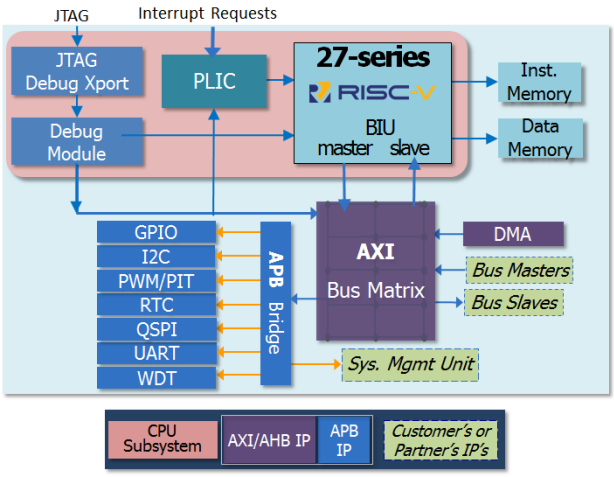
Bus Controller/Bridge

atcbmc300	AXI Bus Matrix Controller
atcaxi2ahb100	Sync. AXI-to-AHB Bridge
atcaxi2ahb200	Async. AXI-to-AHB Bridge
atcbusdec200	AHB Bus Decoder
atcapbbrg100	AHB-to-APB Bridge

Bus Components

atcdmac300	DMA Controller (DMAC)
atcuart100	UART Controller
atcspi200	Quad speed SPI Controller
atciic100	I2C Controller (IIC)
atcgpio100	GPIO
atcpit100	Programmable Interval Timer (PIT)/PWM
atcwdt200	Watchdog Timer (WDT)
atcrtc100	Real Time Clock (RTC)
atcsmu100	System Management Unit

Functional Blocks



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