

AndeStar™ AX45MPV Vector Processor

64-bit RISC-V Multicore Processor with 1024-bit Vector Extension

Benefit

Performance

- ◆ 64-bit in-order dual-issue 8-stage CPU core with up to 1024-bit Vector Processing Unit (VPU)
- ◆ Level-2 cache and coherence support
- ◆ AndeStar™ V5 Instruction Set Architecture (ISA)
 - Compliant to RISC-V GCBP**V extensions
 - Andes performance extension
 - Andes CoDense™ extension for further compaction of code size
- ◆ Separately licensable Andes Custom Extension™ (ACE) for customized scalar and vector acceleration
- ◆ 64-bit architecture for memory space over 4GB
- ◆ Branch predication to speed up control code
- ◆ Linux-capable Memory Management Unit (MMU)
- ◆ Physical Memory Protection (PMP) and programmable Physical Memory Attribute (PPMA)
- ◆ Andes-enhanced Platform-Level Interrupt Controller (PLIC) for a wide range of system events and real-time performance
- ◆ Andes Streaming Port and High-Bandwidth Vector memory support to overcome memory bottleneck.
- ◆ Full-arithmetic BF16 vector/scalar instructions with mode bit control*

Flexibility

- ◆ Multiprocessing up to 8 cores with hardware managed data coherence
- ◆ Configurable VPU vector length (VLEN) and datapath length (DLEN)
- ◆ Easy arrangement of preemptive interrupts
- ◆ ECC or Parity for SRAM error protection
- ◆ StackSafe™ hardware to help measuring stack size, and detecting runtime overflow/underflow
- ◆ Versatile configurations to tradeoff between core size and performance requirements

Power Management

- ◆ PowerBrake and WFI (Wait For Interrupt) for different power saving occasions

Applications

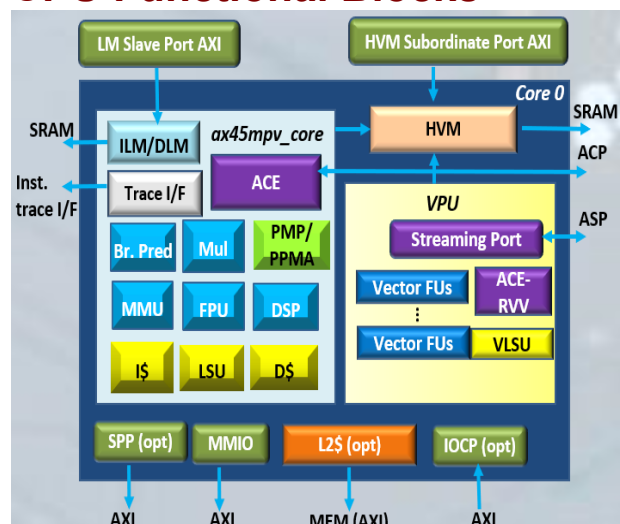
- ◆ Computer Vision and Image Processing
- ◆ Digital Signal Processing
- ◆ Machine/Deep Learning Acceleration

Scientific Computing

General Descriptions

AndeStar™ AX45MPV 64-bit multicore CPU IP is an 8-stage superscalar processor with Vector Processing Unit (VPU) based on AndeStar™ V5 architecture. It supports RISC-V standard “G (IMA-FD)”, “C” 16-bit compression, “B” bit manipulation, DSP/SIMD ‘P’ (draft), “V” (vector) extensions, and Andes performance enhancements, plus Andes Custom Extension™ (ACE) for user-defined instructions. It features MMU for Linux based applications, dynamic branch prediction for efficient branch execution, dual-issue of common instruction pairs, level-1 private instruction/data caches and local memories for low-latency accesses. The AX45MPV symmetric multiprocessor supports up to eight cores and a shared level-2 cache controller with instruction and data prefetch. Coherence Manger ensures data coherence among CPU accesses and IO transactions from cacheless bus masters. The AX45MPV contains a powerful VPU with up to 1024-bit VLEN/DLEN, is excellent for computations involving large arrays of data such as computer vision, image processing, machine/deep learning, and scientific computing. Other features include ECC for level-1/2 memory soft error protection, Platform-Level Interrupt Controller (PLIC) with enhancements for vectored dispatch and priority-based preemption, CoDense™, StackSafe™ for software quality improvement, PowerBrake and WFI for power management.

CPU Functional Blocks



Key Features

Scalar Unit

- ◆ 8-stage in-order dual issue pipeline
- ◆ AndeStar™ V5 64-bit architecture
 - RISC-V RV64 GCBPV, little endian:
 - ◆ RVGC: integer, FP and 16-bit extensions
 - ◆ RVB: bit manipulation extension
 - ◆ RVP: DSP/SIMD instructions extension (draft)
 - ◆ RVV: Vector extension
 - Andes V5 performance/code size extensions
- ◆ Machine (M), Supervisor (S), User (U) privileges
- ◆ MMU and Sv39/Sv48 virtual memory translation
- ◆ PMP up to 32 regions and programmable PMA up to 16 regions
- ◆ Multiplier options for sequential 1/2/4/8-bit per cycle or fast pipelined 2 cycles
- ◆ Optional branch prediction with Branch Target Buffer (BTB) and Return Address Stack (RAS)

Vector Processing Unit (VPU)

- ◆ RISC-V V-extension (RVV) 1.0 spec.
 - In-order, dual-issue
 - Data formats:
 - ◆ Standard: int8/16/32/64, fp16/32/64, bf16**
 - ◆ Andes extended: int4
 - Andes extended instructions
 - ◆ Vector Int4 load
 - ◆ Vector Dot Product
 - Custom RVV instructions based on ACE-RVV
 - Vector Unit-Stride, Strided, Indexed, Segment Load/Store
- ◆ LMUL supporting 1, 2, 4, 8, 1/2, 1/4, 1/8
- ◆ Configurable VLEN/DLEN from 128 to 1024 bits with 1:1 or 2:1 ratio
- ◆ Multiple chainable parallel functional units
- ◆ Independent memory access paths for RVV load/store and Andes Streaming Port (ASP) load/store

Andes Custom Extension™ (ACE)

- ◆ Customized instructions for acceleration (separately licensable)
- ◆ Instruction feature highlights
 - All instructions executing in background
 - Standard and custom-defined operands
 - Vector instructions with RVV formats
- ◆ Design support
 - Design using standard languages (C, Verilog)
 - Automatic opcode assignment
 - Automatic generation of housekeeping RTL
 - Automated instruction function verification

Level-1 Memory Subsystem

- ◆ Instruction and Data Caches
 - Separately configurable from 8KB up to 64KB
 - Direct-mapped, 2-way or 4-way set associative
 - Optional Parity (for Instruction cache) or ECC (instruction and data) error protection
- ◆ High-Bandwidth Vector local Memory (HVM)
 - Configurable from 4KB to 4GB
 - Accessible by both scalar unit and VPU
 - DLEN-wide data width for vector loads/stores
 - Optional ECC error protection
 - Subordinate port for external accesses
- ◆ Instruction and Data Local Memory (ILM/DLM)
 - Separately configurable from 4KB up to 16MB
 - Accessible by scalar core only
 - Optional ECC error protection
 - Local Memory Access port allows accesses from bus masters
- ◆ MemBoost - Enhanced Memory Performance
 - Data cache write-around
 - Instruction and data prefetch
 - Multiple outstanding D-Cache misses

Level-2 Cache Controller

- ◆ Configurable cache size, up to 8MB
- ◆ 64-byte cache line size, 16-way, pseudo random cache line replacement policy
- ◆ Up to 64 outstanding transactions
- ◆ 2 tag banks, 2 data banks with bank interleaving
- ◆ Multi-cycle control to match SRAM timing
- ◆ Optional ECC error protection
- ◆ Instruction and Data Prefetch

Multicore Cache Coherence

- ◆ Support up to 8 cores
- ◆ Coherence among L1 data caches and IO Coherent Port transactions

Bus Interfaces

- ◆ All configurable data width from 128 to 512 bits except 64-bit SPP
- ◆ Synchronous N:1 core-to-bus clock ratios or Asynchronous bus clock
- ◆ Memory port for cacheable accesses
- ◆ MMIO port for non-cacheable accesses
- ◆ IOCP (IO Coherence Port) for cacheless bus masters
- ◆ Local Memory Access Ports for ILM/DLM/HVM accesses
- ◆ Shared Peripheral Port (SPP) for external peripherals

Power Management

- ◆ PowerBrake technology to reduce peak power consumption
- ◆ WFI (Wait for Interrupt) instruction for software controlled stalls

Platform-Level Interrupt Cont. (PLIC)

- ◆ Over 1000 PLIC interrupt sources
- ◆ Up to 255 PLIC interrupt priority levels
- ◆ Up to 16 PLIC interrupt targets
- ◆ Enhanced interrupt features
 - Vectored interrupt dispatch
 - Priority-based preemption
 - Selectable edge trigger or level trigger

External Debug Module

- ◆ Secure debug
- ◆ RISC-V Debug 1.0 JTAG debug interface with up to 8 triggers
- ◆ Exception redirection handling

Trace Interface

- ◆ RISC-V Trace 1.0 Instruction Trace interface

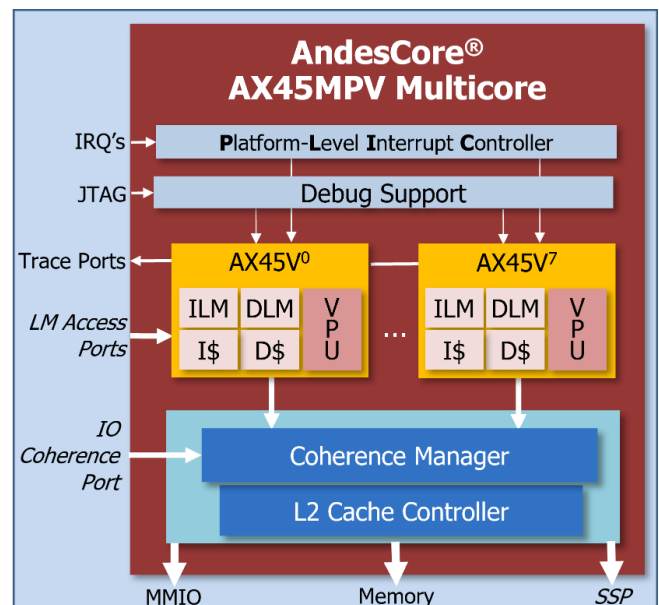
Development Tools

- ◆ AndeSight™ IDE (Eclipse-based)
 - Project Management, Streamlined GUI, Feature-rich Editor, Optimized Toolchains, Source Level Debugger, Profiling Analysis, Flash ISP, RTOS Awareness, and more
 - Tested platforms: Windows and Linux
 - Demo examples and sample projects
 - RTOS: FreeRTOS, Zephyr
 - Linux SMP kernel and platform drivers
 - Optimized compute library: DSP, Vector
 - Peripheral drivers for AndeShape™ platform
 - Near cycle-accurate simulator
- ◆ FPGA Development Boards
 - AndeShape™ Board Farm
- ◆ Debugging Hardware
 - AICE-MINI+, AICE-MICRO
- ◆ COPILOT: automation tool for ACE

Product Packages

- ◆ AndesCore™ AX45MPV with 1, 2, 4 or 8-cores and AE350 AXI Platform
 - Pre-integrated AX45MPV CPU subsystem, PLIC, Debug Module, and AXI Platform

Multicore Functional Block Diagram



* Full-arithmetic BF16 mode is Andes proprietary implementation

**P(DSP) and bf16 extensions are RISC-V draft

AXI-Based Platform Pre-integrated with AX45MPV

Benefit

Convenience

- ◆ A rich collection of high-quality and configurable AXI/AHB/APB(AE350) IPs required by most embedded systems
- ◆ Pre-integrated platform to jump-start designs
- ◆ AXI exclusive accesses to implement the atomic operations to non-cacheable AXI spaces

Flexibility

- ◆ Scalability of AXI Bus Matrix and AHB/APB Bus Bridge to connect various AMBA components
- ◆ Configurable PLIC to simplify SoC integration

Performance

- ◆ Low latency level-one memories for best CPU performance
- ◆ Bus matrix to allow simultaneous transfers of independent transactions
- ◆ DMA controller for fast data movement without software's intervention

General Descriptions

The AXI-based platform pre-integrated with AX45MPV is a system design that serves various purposes such as to explore the product features, to evaluate the performance indexes and to determine the configuration options.

It contains the CPU subsystem, including CPU, Local Memories and PLIC, interfaced to AXI Bus Matrix and AHB/APB Bus Bridge with Platform IP components attached.

Design support includes scripts and test cases for integration, simulation, emulation and prototyping. This pre-integrated platform is ideal for minimizing development efforts by providing a verified reference which is both performance optimized and feature ready for most embedded applications.

Platform IP Components

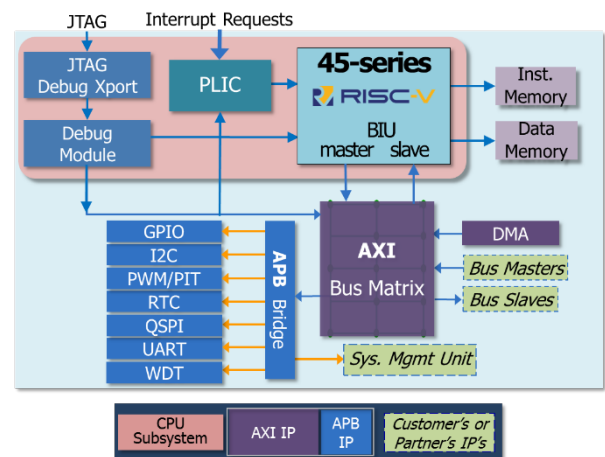
Bus Controller/Bridge

- ◆ atcbmc300 AXI Bus Matrix Controller
- ◆ atcaxi2ahb100 Sync. AXI-to-AHB Bridge
- ◆ atcaxi2ahb200 Async. AXI-to-AHB Bridge
- ◆ atcbusdec200 AHB Bus Decoder
- ◆ atcapbbrg100 AHB-to-APB Bridge
- ◆ atcsizedn300 AXI Downsizer

Bus Components

- ◆ atcdmac300 DMA Controller (DMAC)
- ◆ atcuart100 UART Controller
- ◆ atcspi200 Quad speed SPI Controller
- ◆ atciic100 I2C Controller (IIC)
- ◆ atcgpio100 GPIO
- ◆ atcpit100 Programmable Interval Timer (PIT)/PWM
- ◆ atcwdt200 Watchdog Timer (WDT)
- ◆ atrrtc100 Real Time Clock (RTC)
- ◆ atcexmon300 AXI Exclusive Accesses

Functional Blocks



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