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ANDES in Sight

ANDES TECHNOLOGY Newsletter

Contents

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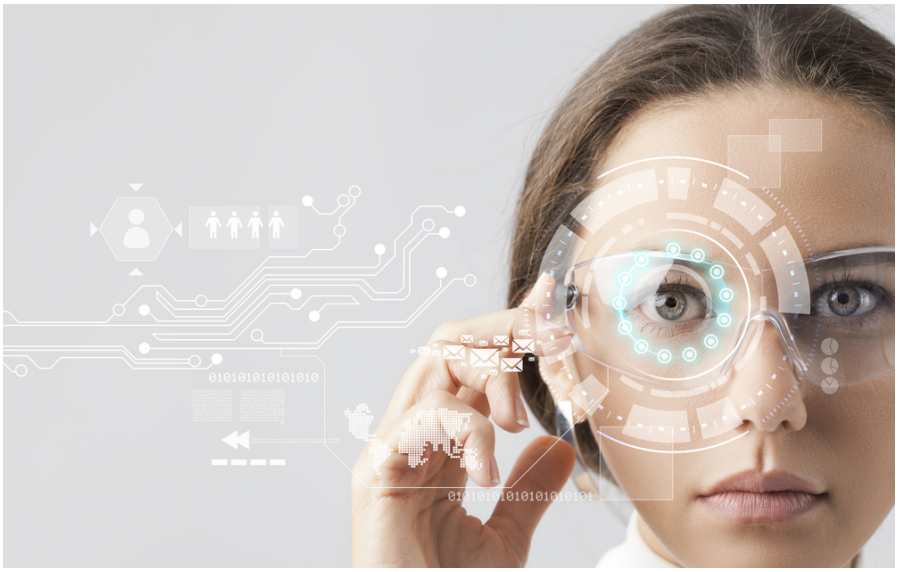


Andes New Quick-Start Design Package Cuts SoC Designs' Time to Market

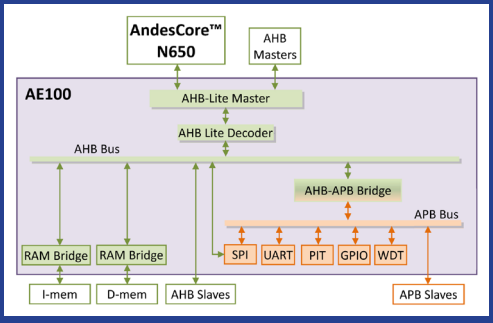
In June, Andes Technology Corporation announced the **Quick-Start Design Package**, a complete solution that reduces SoC designs' risk and time to market. Designers spend time and resources developing and verifying state machines and glue logic to handle the control and status signals of peripherals in a design and risk the design spin of an error in this hardware. By pre-integrating and pre-verifying processor, fabric, and peripherals, the Quick-Start Design package jump-starts customer's SoC projects with a solid foundation and reduces custom glue logic designers need to create. Instead of hardwired control logic, customers can develop software with AndeSight IDE to control its peripherals and debug the SOC.

Available in September but ready for early engagement now, the package includes the new AndesCore™ N650 CPU IP, AndeShape™ AE100 Platform IP, and AndeSight™ IDE software development environment. The new compact N650 CPU is optimized for performance-efficiency needed for entry-level SoC, and the new Platform IP offers several highly-optimized peripherals and the bus fabric that SoCs require to surround and enable a customer's design.

"Time-to-market is a major concern for every SoC design," said Frankwell Jyh-Ming Lin, President of Andes Technology Corp. "One task that slows design progress is writing RTL code for integrating standard IP blocks and spending 70 percent additional effort in verification. The Quick-Start Design Package provides an optimized plug-and-play solution that saves effort developing functionality not providing significant value to the final design. Using software to control the peripherals minimizes risk for SOC designs by reducing this RTL logic."

"Running control software on the new Andes N650 CPU IP, designers reduce risk considerably and shorten their silicon development schedule," said Charlie Hong-Men Su, Ph.D., Andes Technology CTO and Senior Vice President of R&D. "For example, it's a simple software revision to change the configuration of PCIe, DDR boot sequence, and other functions post-silicon. Besides facilitating software development and optimization, the AndeSight IDE allows access to the entire system for chip-level debugging through the JTAG interface. By re-using the production-quality processor and peripheral controllers, and extensible bus fabric, the Quick-Start Design Package reduces design teams' risk of a silicon respin."

Elements of Andes Quick-Start Design Package Solution



The elements of the Quick-Start Design Package—new AndesCore™ N650 CPU IP, AndeShape™ AE100 Platform IP, and AndeSight™ IDE software development environment—each has unique features. The new N650 CPU core has a 3-stage pipeline with 16 general-purpose registers and multiply and divide instructions. It delivers 25 percent better DMIPS/MHz performance and 40 percent better DMIPS/mW power efficiency than competitive offerings in the TSMC 90LP process.

The N650 CPU IP core has memory mapped I/O, a 32-bit wide AHB-Lite bus, up to 32 vectored interrupts, 4-priority nested interrupts, and power management instructions—essential for power sensitive designs. The core comes with Embedded Debug Module, 2-wire Serial Debug Port and up to 8 breakpoints/watchpoints.

The new AE100 Platform IP features a new AHB Configurable Fabric with 24-bit address width and 32-bit data width. It supports up to 8 AHB masters, up to 30 AHB slaves and up to 31 APB slaves. Components of the fabric include AHB-Lite master multiplexer, AHB-Lite decoder and AHB-to-APB bridge. Other peripherals included are a Low-latency RAM Bridge, SPI controller, general purpose I/O (GPIO), watchdog timer, programmable interval timer and UART.

The AndeSight Eclipse-based IDE offers a fully functional Andes C and C++ integrated development environment that enables managed build system. It comes with a profiler, code coverage, code size analysis, chip profile, in-system programming, and advanced debugging. The tool chain has a highly-optimized compiler as well as assembler, linker, loader, libraries, and debugger. A core simulator, pre-defined models of AndeShape SOC platform, and external plugin APIs are also provided.

Andes Wins ITE Tech. Inc. IT835X Series Sensor Hub Design Targeting the High Growth Wearable & IOT Market

Andes Technology Corporation announced in June that its N801 CPU core has been designed into the IT835X sensor hub chip from ITE Tech. Inc. based in Hsinchu, Taiwan. The Andes N801 32-bit CPU core executes ITE's sensor fusion algorithm for accelerometer, gyroscope, and magnetometer-core elements found in most wearable devices. Andes N801's best in class MIPS/mW specification enables the IT835X to achieve reduced power consumption while providing the high performance the sensor fusion algorithm demands.

Source: Jawbone

"We're very proud of our sensor hub system-on-chip (SoC)," stated Mr. Lawrence Liu, General Manager-Business Division at ITE Tech. Inc. "Soon after we launched the chip, it won several OEMs' design for mobile device application. Our choice of the Andes N8 CPU core with its small gate count and superior MIPS-per-mWatt performance helps make the IT835X sensor hub chip a competitive offering to win customers in the fast growing sensor hub market. With the Andes N8 32-bit MCU, the IT835X operates independently to integrate sensing information and significantly reduces the burden on the system CPU to achieve the low-power requirements of smartphones, tablets and wearable devices."

"We are extremely pleased that ITE Tech chose the N801 as the central processor in their IT835X sensor hub chip," said Al Kuo-Chi Lin, Vice President of Andes Technology Corp. "Sensor hubs are key elements in wearable electronics to help reduce the applications processor's load. The AndesCore™ series offer many features for wearable electronics. They include CoDense™ for very compact code size; StackSafe for automatic detection of stack overflow; PowerBrake for a purely digital way to scale frequency and power without a clock divider; FastWakeUp for Automatic CPU state save/restore for fast power-down/power-up; and FlashFetch, which is separate IP to speed up internal Flash and allow execute-in-place external Flash support. Andes Custom Extension (ACE) provides programmable acceleration and energy reduction through the use of custom instructions."

Wearable Application

In the **paper** "ZOE: A Cloud-less Dialog-enabled Continuous Sensing Wearable Exploiting Heterogeneous Computation," Nicholas D. Lane, et al detail a match-box sized lapel-worn sensor that continuously senses data to determine three major variables: Personal Sensing-physical activity, transport (car, train, etc.), and stress; Social Sensing-conversations with others; and Place Sensing-work or home. Zoe is built around three processors: an applications processor running the algorithms that analyze data from the accelerometer and gyroscope sensor hub (an IT835X with Andes N8) that provides personal sensing, the microphone sensor that provides social sensing, and place sensing. The design goal for ZOE is to operate all day on a single battery charge. In the paper, the authors observe that the three-processor approach achieves this goal, providing a 30 percent increase in system operation as contrasted with running the three discrete functions on the one applications processor.

About the AndesCore™ Family of Processors

AndesCore comprises a series of high performance 32-bit CPU core families targeting different emerging embedded applications markets. The small gate count and highly power-efficient 2- and 3-stage N705 and N801 families are replacing 8-bit/16-bit microcomputer in consumer applications. The N705 and N801 families deliver better power efficiency (DMIPS/mW) than competing 32-bit processors. Security extensions of AndeStar™ architecture in the AndesCore™ S801 secure processor core family provides code and data protection from physical attacks and malicious debugging. This makes the S801 family ideal for secure cards, IoT, and device authentication applications.

Andes E801 family targets Internet of Things (IoT) applications with the unique Andes Custom Extension™ (ACE). ACE enables designers to specify custom instructions to raise the performance-efficiency an order of magnitude higher to meet the extreme low power requirement of IoT applications. With Andes' Custom-OPtimized Instruction deveLOpment Tools (COPILOT™), designers can easily create such custom instructions that differentiate their design from competitive offerings based on standard instruction set processors. By adding special instructions, not easily discoverable by hackers, ACE also provides stronger security to a design. ACE also simplifies the verification task by automatic generation of test cases and comparison between the instruction semantics and its implementation.

Evaluate Andes IP Cores

Andes has over 100 licensees and Andes-embedded products are shipping in more than 1.4 billion devices around the globe from licensees in Taiwan, Japan, Korea, China, Europe, and USA. The company is expanding into the Americas.

If you have an SOC design in need of a low power, low cost CPU with full toolchain and peripheral support, contact us to arrange a free evaluation. Let us help with your next design. E-mail us at **info@andestech.com**.
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Over 100 Andes' Customers have Cumulative shipped 1.4 Billion AndesCores Worldwide

Andes Technology Corporation announced at the end of March that its customer base of 100 licensees have cumulative shipped over 1.4 billion SoCs containing AndesCore 32-bit CPUs as of October 2015. Last year the company recorded over 390 million SoCs shipments with AndesCore 32-bit CPUs, an amount double the total reported by the 2014 Linley Group Report "A Guide to CPU Cores and Processor IP." In addition, the company's **AndeSight** Eclipse-based integrated development environment (IDE) continues widespread adoption, reaching 10,000 installations globally at the start of 2016.

"Ongoing adoption of the AndesCore architecture continues to rise and we expect the 2016 shipments to go well beyond the 390 million shipments in 2015," stated Andes Technology Corporation President, Frankwell Jyh-Ming Lin. "By leveraging the AndesCore architecture's high performance, low-power, and small size, our licensees are developing unique applications in brushless DC motors, touch panel displays, automotive back-up cameras and many more. The architecture is ideally suited for the increasing number of designs targeting the Internet of Things."

"As a result of the increased shipment volume of chips containing AndesCore CPUs, the AndeSight™ software integrated development environment (IDE) has seen steady shipment growth reaching a cumulative 10,000 seats at the end of 2015," stated Charlie Su, Ph.D. Andes Technology Corporation CTO and Senior Vice President of R&D. "The AndeSight IDE implements a high efficiency compiler that allows compiled code to deliver best-in-class performance and compactness. Besides program development, code upgrading, and debugging, AndeSight also provides numerous advanced features. These include code coverage analysis, function profiling, performance meter, and a simple interface for customers to hook up their SoC-dependent GUI. AndeSight serves both IC design houses and system companies, enabling the former faster time to market and allowing the latter to facilitate their market development."

Andes Technology Corp.

Founded in March 2005, **Andes Technology Corporation** headquartered in SiSoft Research Center, Hsinchu, Taiwan is a leading Taiwan CPU intellectual property (IP) supplier, with over 100 licensees in Taiwan, Japan, Korea, China, Europe, and USA that have shipped over a half billion units. Its products range from the entry level **N7** and **E8**, **S8** and **N8** with 2- and 3-stage pipelines, to the high-end **N13** with 8-stage and longer pipelines. The mid-range **N9** has the highest customer shipping volume while the mid-range **N10**, **D10**, and high-end **N13** support Linux and floating-point coprocessor. Configurable and extensible Andes cores enable designers to create unique designs.
AndeSight™ IDE enable customers to efficiently develop, debug, tune and regress their software. **AndeSoft™** provides customers optimized fundamental software such as OS, drivers, standard C libraries, middleware, etc. for rapid application development. The company has sales offices throughout Asia and the U.S.

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