



ANDES in Sight

ANDES TECHNOLOGY Newsletter, US Edition

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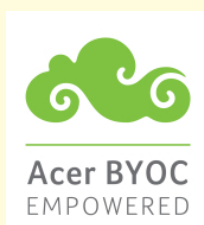
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Andes and Acer BYOC™ Support Inter-Platform IoT SoC Cloud Design Solutions

Andes Technology Corporation, the leading Asia-based supplier of small, low-power, high performance 32-bit embedded **CPU cores**, and Acer BYOC™ (Build Your Own Cloud™) today announced plans to support each other's Internet-of-Things cloud service solutions for SoC Design. Andes and **Acer BYOC** will each develop technology offerings that will enable SoC engineering design teams to build IoT SoCs with Acer cloud services using Andes Knect.me ecosystem resources. Andes will support Acer BYOC's open platform and help expand Internet-of-Things cloud ecosystem to the level of IC and SoC design. Acer BYOC will grow the vertical coverage of Andes' CPU

IP and IoT **Knect.me** ecosystem on their expanding cloud service platform.



Courtesy Acer Inc.

"Both Acer and Andes offer complementing IoT solutions to the global market," said Maverick Shih, President of BYOC Business Group at Acer Inc. "By offering inter-platform compatibility, we hope to create a mutually beneficial ecosystem for our joint customers."

"We admire how Acer has studied the progress of the IoT market trend over the long-term and devoted itself early on to building up cloud technology," Frankwell Jyh-Ming Lin, President of Andes Technology Corporation, stated. "Our collaboration with Acer BYOC will enable Andes customers that design hardware and develop software for IoT SoCs the convenience of obtaining cloud service solutions plus underlying building blocks from Knect.me, our IoT ecosystem providing open-source and commercial solutions for modern connected devices based on the highly performance-efficient AndesCore™ processors. Customers will derive great benefit through this technology and business relationship."

BYOC™ Cloud Service Platform And IoT Computing



Acer BYOC
EMPOWERED

Courtesy Acer Inc.

Emerging services and innovative applications are raised by the development of ubiquitous computing and IoT devices. Equipped with sensing, connectivity, and intelligence, connected IoT devices change the computing paradigm. Legacy resources, such as storage and computation, are migrating from computing devices to the cloud for emerging networked applications. In addition to storage capacity and computing power, SoC designers for IoT applications also face the daunting task of integrating silicon intellectual property and software stacks as well as easy access to cloud services to complete real world usages of the IoT computing. The example of a fitness wearable illustrates how the cloud becomes a component of an SoC design. The SoC controls an intelligent sensor, but the cloud provides the sensor output.

The challenge is to build both device and service infrastructure. The inter-platform support of Andes and Acer BYOC combines the market proven elite software stack and hardware platform from Andes **Knect.me** ecosystem with the cloud service open platform from **Acer BYOC**. The Acer BYOC platform provides modular services such as music, file storages, media and document applications, and it also allows developers to rapidly bring new and innovative applications to IoT devices. By introducing such a flexible cloud platform on top of the rich device hardware-software framework, Andes and Acer BYOC enable developers to quickly bring smart connected applications to reality.

Adapting to the Seismic Shift in the Semiconductor Industry

By: Emerson Hsiao, Senior VP Andes Technology Corp.

Today's Internet-of-Things device needs embedded processing capability that can deliver low cost, low power consumption and high security. Older 8-bit CPUs lack the processing power and architectural features to efficiently deliver these critical IoT functions. Furthermore, many 32-bit embedded cores designed for server and smart phone applications cannot deliver them either. Only the **AndesCore** series of high performance 32-bit CPU cores, designed in the past decade, have all these IoT demanded elements included.

Andes CPU cores, AndesCore, has been designed into IoT devices, which need to have years of battery life. The architecture enabling enormous power savings while providing high performance, and hacker resistant security includes such features as frequency throttling, patented memory architecture, and custom instructions.

Andes **PowerBrake** is a low-cost means to achieve CPU frequency scaling without changing the PLL clock. This is needed for intelligent sensors, which spend so much time waiting for an input, brief periods of complex computation, short periods of compressing data and communicating it to an external device. PowerBrake allows 16 different performance scales so the processor can throttle up or down to accommodate different computing requirements.

The major performance bottleneck in an IoT device is the flash memory containing its program. Andes **FlashFetch** breaks the bottleneck using a small amount of cache—tiny cache—and a prefetch SRAM buffer. Running the Coremark and DMIPS benchmarks with FlashFetch can boost the score

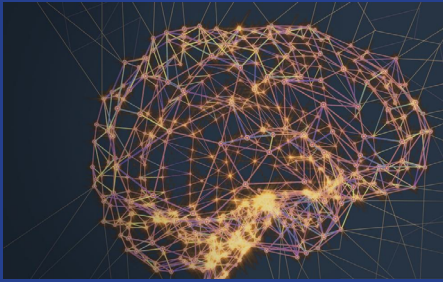
from 30 to 80 percent.

A custom instruction in the **Andes Custom Extension** (ACE) framework to accelerate compute intensive tasks is another Andes architectural contribution. A custom instruction to accelerate a FIR filter can boost performance and reduce power consumption as much as an order of magnitude. Custom instructions are not new, but Andes' contribution is a powerful tool that facilitates creating the instruction and incorporating it into existing software development tools with quick turnaround. In addition, the ACE logic of the instruction is verified against its semantics automatically in the flow.

Architectural elements added for physical security include secure interrupt with hardware memory stacking, data and address scrambling, and differential power analysis protection. The first protects the CPU states of secure software from attack via a malicious ISR (interrupt service routine) without compromising the real-time response of cooperative ISR's. Scrambling defends against attacks to the interface between CPU and memory. Power analysis protection guards observing the power use signature of the CPU. This is achieved by scrambling the power profile of the CPU to make it unintelligible to an attacker.

Another security vulnerability is the debug port on most chips for software upgrade and maintenance during design and for bug fixes in the field. Many SoC designs remove the debug port before final silicon. However, Andes architecture provides a secure embedded debug module that allows designers to fix software in the field while guarding against physical attacks.

Enabling the Next Wave of Machine Learning Acceleration



Wave is a systems startup that has developed a low power, high-performance data flow computing platform to accelerate critical applications such as machine learning (CNN/DNN/AI), national/cyber security, unstructured search and big data analytics. Wave is developing a family of compute acceleration hardware ranging from OCP mezzanine to 1U appliances, all based on their proprietary Byte-Fabric™ programmable SOC's. By placing special emphasis on low-power computing, Wave offers best-in-class performance as measured in operations/Watt. The company is venture-backed (Tallwood and Southern Cross) and staffed with a cadre of industry veterans and entrepreneurs.

www.wavesemi.com

Evaluate Andes IP Cores

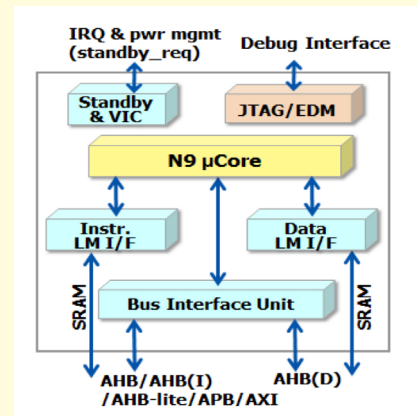
Andes has over 100 licensees and Andes-based products are shipping in more than a 1.4 billion devices around the globe from licensees in Taiwan, Japan, Korea, China, Europe, and USA. The company is expanding into the Americas.

If you have an SOC design in need of a low power, low cost MCU/CPU with full toolchain and peripheral support, contact us to arrange a free evaluation. Let us help with your next design. E-mail us at info@andestech.com. Andes Technology USA Corporation 2375 Zanker Road, Suite 210, San Jose California 95131

Wave Semiconductor Selects Andes' 5-stage Pipeline N9 CPU to Use in Its Embedded Core

Andes Technology Corporation, the leading Asia-based suppliers of small, low-power, high performance 32-bit embedded CPU cores, today announced that **Wave Semiconductor** has licensed **Andes low power, N9** 32-bit, 5-stage pipeline CPU core and **Andes AE210P** peripherals for a new chip design. Wave selected the Andes core to provide boot-time configuration and continuous monitoring of Wave's SoC operation. The ease of integrating the Andes N9 and peripherals into its larger SoC design, the native AXI4 support, high performance at low power consumption, and small silicon footprint contributed to Wave's decision.

"We are pleased with our choice of the Andes N9 CPU core for our next SoC design," said Richard Terrill, Vice President of Marketing at Wave Semiconductor. "We needed a small but powerful CPU to manage critical tasks at power-up boot and on-going observation of chip operation. The N9's programming tools and support of the AXI bus interface fit our requirements nicely. Its straightforward synthesis made for integration into our larger



design and its small silicon footprint provided an added bonus."

"Andes is thrilled that Wave Semiconductor chose our N9 CPU core for their new SoC design," said Frankwell Lin, President of Andes Technology Corporation. "The N9 delivers high performance in a small gate count and on a low power budget. Its ability to provide low-latency vectored interrupt makes it very efficient for high performance real time monitoring. The N9's ability to mix 16- and 32-bit instruction format enables compact code and the five-stage clock-gated pipeline contributes to the core's 3.43 CoreMark/MHz performance, while its power management instructions conserve power."

Andes Technology Corp.

Founded in March 2005, **Andes Technology Corporation** headquartered in SiSoft Research Center, Hsinchu, Taiwan is a leading Taiwan CPU intellectual property (IP) supplier, with over 100 licensees in Taiwan, Japan, Korea, China, Europe, and USA that have shipped over a half billion units. Its products range from the entry level **N7** and **E8**, **S8** and **N8** with 2- and 3-stage pipelines, to the high-end **N13** with 8-stage and longer pipelines. The mid-range **N9** has the highest customer shipping volume while the mid-range **N10**, **D10**, and high-end **N13** support Linux and floating-point coprocessor. Configurable and extensible Andes cores enable designers to create unique designs.

AndeSight™ IDE enable customers to efficiently develop, debug, tune and regress their software. **AndeSoft™** provides customers optimized fundamental software such as OS, drivers, standard C libraries, middleware, etc. for rapid application development. The company has sales offices throughout Asia and the U.S.

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