October 2015 **Volume 1, No. 4**

ANDES in Sight

ANDES TECHNOLOGY Newsletter, US Edition

Contents

ANDES Technology USA

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Publisher: Andes Technology Corporation
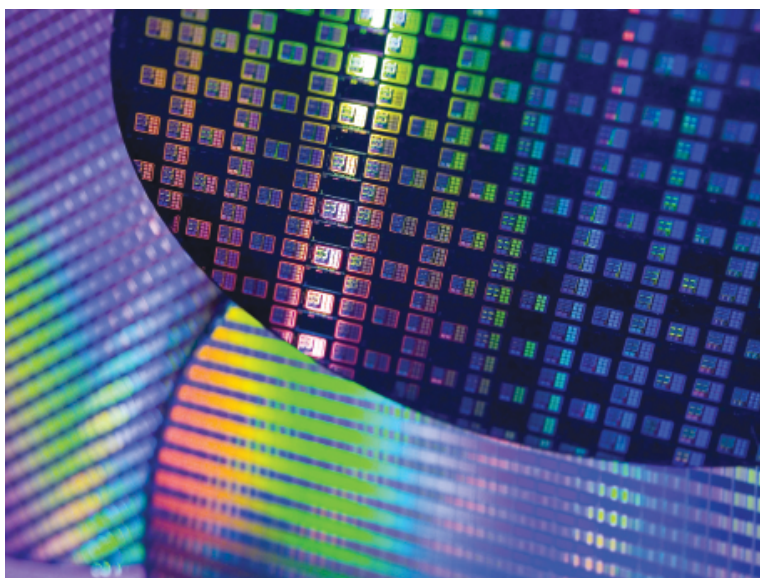**Chief Editor: Jonah McLeod**

Photo: Courtesy Taiwan Semiconductor Manufacturing Company Limited

Andes Technology Corp. Receives TSMC 2015 Partner of the Year Honor

Andes Technology Corporation, Asia's leading supplier of small, low-power, high performance 32-bit embedded CPU cores, announced that it has been awarded TSMC's 2015 Partner of the Year award for New IP. Emerson Hsiao, Senior VP of Andes Technology USA Corporation was presented the award during TSMC's recent Open Integration Platform Ecosystem Forum that brought together TSMC's design ecosystem partners and customers to share solutions to today's design challenges.

"We are extremely proud that TSMC has honored Andes Technology Corporation with its 2015 Open Innovation Platform Partner of the Year," Hsiao said. "The CPU architecture that Andes Technology Corporation

developed less than 10 years ago by its world class computer and software architects and engineers is shipping in over 700 million System on Chips, the vast

majority of which have been fabricated at TSMC's leading edge foundry. We have worked closely with TSMC to ensure our IP can leverage the foundry's low power

Photo: Courtesy TSMC Ltd

and high performance processes to help achieve the best power/performance results for our mutual customers."

"Andes Technology Corporation has developed into a valued TSMC partner," declared Suk Lee, Senior Director of TSMC's Design Infrastructure Marketing Division. "As TSMC has evolved to serve emerging markets such as the Internet of Things, we have expanded our ecosystem to support new products and customers. Having an emerging partner developing CPU IP to meet the low power needs of rapidly growing applications like IoT helps us serve this next generation of chip designs."

Markus Levy, EEMBC President


CORE**MARK**®
An EEMBC Benchmark

"Andes is the first EEMBC member to have all of its processor cores certified for the CoreMark benchmark," said Markus Levy, EEMBC President. "As designers increase the number of cores going into embedded applications, especially the ultra low-power Internet of Things, CoreMark becomes less a measure of brute force performance and more a measure of the right amount of performance for a specific design goal."

Developing an Ultra Low Power Processor for IoT Applications
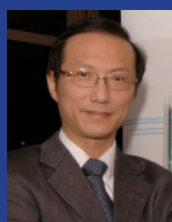
By: Frankwell Lin, President, Andes Technology

IoT devices may need to last for years on a single battery charge. Conventional techniques provide some power savings, but custom instructions to accelerate compute-intensive tasks provide greater improvements in performance and power efficiency. KNECT.ME is a multi-company initiative to promote best-in-class IP that enables designers to achieve the full measure of their IoT product specification. This (youtube) presentation describes a smart solution for an IoT device including a high-performance processor core with low power and low cost (small silicon footprint).

Providing a Better Metric for Measuring Performance and Power in IoT SoCs

By: Emerson Hsiao, Senior VP Andes Technology Corp.

The problem confronting chip designers developing IoT SoCs is the need for high computer performance and low power consumption. This is especially true for SoCs being developed for devices required to operate for years on a battery. One example is the new generation of electronic shelf label (ESL) with a requirement of 5 years. The ESL receives central server pricing updates along with a few words of text that can occur as frequently as hourly. How does a design team select an embedded processor for such an application? One way is to use a benchmark that specifies some metric per MHz, such as the EEMBC CoreMark® to better evaluate alternative solutions.

Embedded processor for IoT devices, such as the ESL, is expected to provide security, communications, sensing and control, and power management. Robust security is essential to prevent network attacks, physical attacks and, to protect against software/firmware theft. Because IoT devices operate autonomously and provide data to remote clouds, low-power communications requires the processor to compute proprietary or standard protocols such as RFID, 802.15.4, Bluetooth Smart, Bluetooth 4.1, WiFi 802.11ah, and LTE Cat-0. Processing a variety of sensor data coming from the control interface requires versatile DSP capabilities. And power management is essential to enable months to years of operation on small batteries or harvested energy, thus demanding processors with efficient power management for long sleep cycles, fast power-up/power-down, and the ability to operate at varying clock frequencies—to sip energy rather than full-on or full-off. The EEMBC benchmark provides guidance on how well an embedded core will meet these requirements.

Built upon objective, clearly defined, application-based criteria, the EEMBC CoreMark benchmark reflects real-world applications and tests a processor's basic pipeline structure, as well as the ability to test basic read/write operations, integer operations, and control operations. Over time, CoreMark has replaced Dhrystone MIPS as the industry standard for measuring processor, DSP, and compiler performance.

Andes Technology Corporation has taken the step of having all its processors certified to the EEMBC CoreMark® to provide designers a comparison metric to use in evaluating processors for their design. This month the company announced that the EEMBC Technology Center (ETC) has officially certified CoreMark results for the Andes' entire CPU product line. EEMBC certification ensures that scores are repeatable, accurate, obtained fairly, and derived according to EEMBC's rules. This certification is the most extensive carried out by any EEMBC member and ranges from the 2-stage pipeline Andes N705 CPU core, which achieved a CoreMark/MHz score of 3.32 to the 8-stage pipeline Andes N1337 CPU core that achieved a CoreMark/MHz score of 3.13 (see table below). The measurement of CoreMark/MHz can provide a good initial comparison of performance-efficiency among different cores with similar pipeline.

Processor	Pipeline Stages	CoreMark /MHz
Andes N705	2	3.32
Andes N801	3	3.05
Andes E801	3	3.51
Andes N968A	5	3.43
Andes N1068A	5	3.75
Andes N1337	8	3.13

Jim Lipman, Marketing Director
Sidense Corp.

Sidense's Split-Channel antifuse-based 1T-OTP bit cell has the inherent security required in the Smart Connect Universe. The security of 1T-OTP macros has been confirmed by multiple independent analysis teams. The state of a 1T-Fuse™ bit cell is virtually impossible to detect using chemical etching, SEM and other conventional reverse engineering methods and a bit-cell state is not dependent on any charge storage. When programmed, a bit-cell undergoes a permanent structural change in a few atomic layers that cannot be altered by exposure to high temperature, voltage or radiation.

Sidense's Split-Channel Antifuse Bit Cell
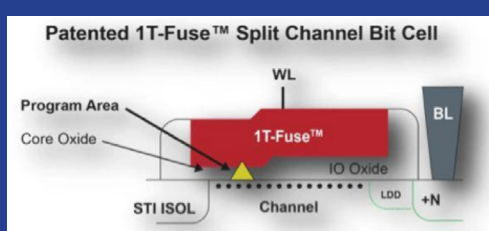
The combination of antifuse-based OTP macros designed for applications requiring very secure stored data, efficient and low power processor cores, and other anti-hacking IP can substantially reduce the susceptibility of Smart Connected devices to security breaches.

Security a Priority in a Smart Connected World

By: Jim Lipman Marketing Director, Sidense Corp.

In the increasingly interconnected world that we are experiencing, fueled largely by the evolving IoT ecosystem, data and IP security is rapidly being recognized as a critical consideration for IoT-targeted devices and systems. In an ecosystem where everything is interconnected, each device must be highly secure, since a security breach on even one simple edge device can conceivably propagate to any other device on the network.

Sidense uses the term "Smart Connected Universe" as a compilation of traditional market segments, including mobile computing, IoT, wearables, automotive, industrial and medical, where a collection of devices are connected via a common network. Achieving the necessary level of security in the Smart Connected Universe requires the cooperative efforts of several types of semiconductor and silicon IP companies that contribute sensor, memory, communication core, cryptography and Trusted Execution Environment (TEE) technology, among others.

The memory technology these devices use must be both physically secure and tied in to proven cryptographic and other security technology, either intrinsically implemented or through the addition of third-party software and hardware. The end-game for all of the contributors to a secure Smart Connected device is to provide an environment that is safe from the many types of security attacks that exist both now and in the future.

As a provider of one-time programmable (OTP) memory, Sidense recognizes the important role secure memory plays working with a processor company such as Andes. Secure NVM performs multiple tasks at a processor-based IoT node, which includes sensor hubs and smart edge devices. The NVM technology must be highly secure when storing processor code, custom processor instructions and encryption keys. This requires an NVM technology that not only meets IoT requirements of low power and small footprint, but also provides a data-in-place environment that is secure against hacking and malicious content extraction and modification.

Secure storage of custom processor instructions is of particular interest to processor developers. These instructions can not only be used for product differentiation and performance enhancement, but may also be employed to implement security features in a device, such as running encryption/decryption algorithms, which cannot be exposed to hackers.

An antifuse-based OTP memory that does not depend on charge storage has many attributes that makes it a good candidate for one-time and few-time programmable uses in Smart Connected devices. A programmed antifuse bit cell cannot be un-programmed with voltage, temperature or radiation. Beyond the intrinsic security of the antifuse-based bit cell, in which it is almost impossible to detect whether a bit cell is programmed or not, the bit-cell-based OTP macros must also be designed to defeat hacking attempts.

Such design techniques include fully differential data storage and differential read modes, along with leakage compensation for un-programmed cells or for leakage induced by current and temperature manipulation, to prevent successful side-channel attacks. Another security feature is no power signature on charge-sensing read circuitry to prevent differential power analysis attacks. Furthermore, covering IO and memory array areas with metal layers that render the OTP dysfunctional when removed prevents visual detection of OTP properties by attacks utilizing process layer removal followed by scanning and inspection.

About the D1088

Tightly integrated Integer and DSP processor architectures are not new, but most were designed for applications where power was not as much a constraint as it is today. The new D1088 was designed with low

AndesCore™ D1088 CPU+DSP Delivers Better Performance, Uses Less Power and Half the Code Size of Competitive Offerings

power in mind. It contains functionality to enhance efficiency and reduce application code size to lower both power and cost. For example, to significantly boost the computational efficiency in matrix, filtering, Fourier Transform, and statistics functions, it can execute 4-way 8-bit, or 2-way 16-bit SIMD instructions in a single-cycle latency. In addition, for multimedia applications, the D1088 also supports 64-bit add, subtract, and multiply mixed computation.

For voice application, the D1088 offers left shift, right rounding and shift, most significant word, 32x32 multiply and specially designed 32-bit instructions to replace lengthy 64-bit computation. To reduce code size and increase efficiency, the D1088 provides a Zero Overhead Loop instruction to offload loop branching. To enhance parallel computational capacity, the D1088 provides left and right shift, minimum, maximum, and absolute value, besides traditional SIMD instructions such as add, subtract, and multiply.

Andes Launches New DSP+CPU Core Offering 134% Higher Performance than Competing Alternatives

This month, Andes Technology Corporation, the leading Asia-based supplier of high-volume, low-power 32-bit embedded CPU cores, announced the D1088, a 5-stage pipeline processor with integrated DSP that offers 130 SIMD (single instruction, multiple data) instructions. When implemented in a 90nm low power process, the D1088 delivers 588 DMIPS, 134% higher than competing offerings. Measured using the popular Whetstone floating-point benchmark, the D1088 achieves 92% better performance. When running popular and comprehensive (over 200) DSP libraries, the D1088 is 116% faster with half the code size than alternative cores. Even with the above advantages, the D1088 still achieves smaller die area and less power per MHz than competing offerings.
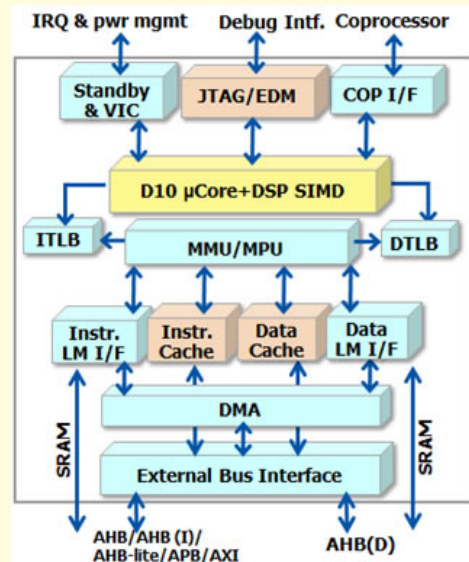
"We're proud of the results achieved with the D1088 DSP+CPU core," said Dr. Charlie Su, Chief Technology Officer and Senior VP of R&D at Andes Technology. "With the increasing numbers of designs performing signal processing for smart sensors, image processing, motion detection, audio and video, the D1088 will provide a wide range of benefits, including better compute performance and power savings, as well as additional functionality. The D1088 easily interfaces with both AHB and AXI bus for simplified use in SOC devices. It comes with an optional memory management unit to support the Linux OS and an optional memory protection unit to support real time operating systems (RTOS)."

Evaluate Andes IP Cores

Andes has over 80 licensees and Andes-based products are shipping in more than a half a billion devices around the globe from licensees in Taiwan, Japan, Korea, and China. The company is expanding into the Americas.

If you have an SOC design in need of a low power, low cost MCU/CPU with full toolchain and peripheral support, contact us to arrange a free evaluation. Let us help with your next design. E-mail us at info@andestech.com. Andes Technology USA Corporation 2375 Zanker Road, Suite 210, San Jose California 95131

Andes Technology Corp.

Founded in March 2005, Andes Technology Corporation headquartered in SiSoft Research Center, Hsinchu, Taiwan is a leading Taiwan CPU intellectual property (IP) supplier, with over 80 licensees in Taiwan, Japan, Korea, and China that have shipped over a half billion units. Its products range from the entry level N7 and N8 with 2- and 3-stage pipelines, to the high-end N13 with 8-stage and longer pipelines. The mid-range N9 has the highest customer shipping volume while the mid-range N10 and high-end N13 support Linux and floating-point coprocessor. Configurable and extensible Andes cores enable designers to create unique designs. AndeSight™ IDE enable customers to efficiently develop, debug, tune and regress their software. AndeSoft™ provides customers optimized fundamental software such as OS, drivers, standard C libaries, middleware, etc. for rapid application development. The company has sales offices throughout Asia and the U.S.

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