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ANDES in Sight

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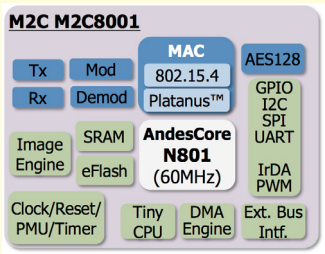
Extensible CPU Cores Exploit Vast Potential in the IoT

By: Charlie Su, Ph.D. Andes Technology Corp. CTO and Senior VP of R&D

Embedded computer requirements for IoT devices, like the electronic shelf label (ESL), include security, communications, sensing and control, and power management. Security is essential to prevent network attacks as well as physical attacks and to protect against software/firmware theft. Communications requires megabytes of processing to handle proprietary or standard protocols such as RFID, 802.15.4, Bluetooth Smart, Bluetooth 4.1, WiFi 802.11ah, and LTE Cat-0. Processing a variety of sensor data coming from the control interface requires versatile DSP capabilities. And power management is essential to enable months to years of operation on small batteries or harvested energy, thus demanding processors with efficient power management for long sleep cycles, fast power-up/power-down, and the ability to operate at varying clock frequencies—to sip energy rather than running full-on or full-off.



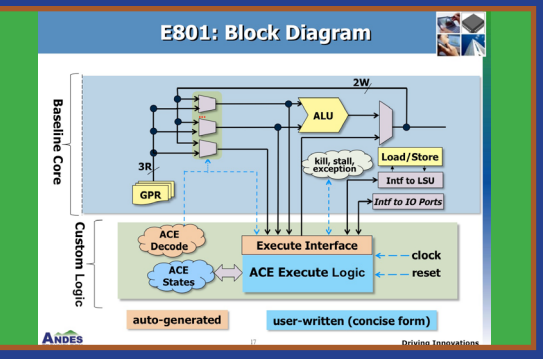
To serve this range of requirements, embedded processors need to provide general-purpose computing with high performance-efficiency and flexible power consumption. They must offer DSP computing capabilities such as SIMD (single instruction multiple data) processing to efficiently handle the wide range of sensors operating with these IoT devices. Finally, these embedded processors need to be extensible to allow application specific acceleration and added security. This is the architecture Andes created in its new generation of embedded processors developed in 2006 and enhanced over time since then to adapt to IoT application needs.

The low power 32-bit AndesCores™ architecture provides cores with pipelines from 2 to 8 stages long. At 28nm process, these cores operate from 500 to 1500 MHz but can be throttled to a few 10s of MHz for ultra low power operation. They achieve from 1.53 up to 2.41 DMIPS per MHz of performance while operating on 2.1 to 26 µW/MHz of power. And they occupy miniscule silicon area from 0.007 to 0.102 mm2.

To read the complete article see EETimes Europe June 2015.

Configurations[a]	Optimized C Code	Optimized C Code with CRC Table	ACE CRC32 Instruction
ROM size	190[b]	32[b]+1024[c]	6
Extra gates	0	0	475
Total area overhead, Ratio	475, 0.97x	2640, 5.4x	490, 1x
Cycles, Ratio	277, 92x	45, 15x	3, 1x
Dynamic power[d] (uW/MHz), Ratio	20.6, 1.33x	20.8, 1.34x	15.5, 1x
Energy consumption Improvement	114x	19x	1x

Most designs approach the polynomial using optimized C code. A second more power efficient method is to add a CRC table to the optimized C code. The table details these two methods in comparison to using a custom instruction to solve the polynomial in a custom engine. The approach of combining a CRC table with optimized C code uses 19 times the energy required to perform the polynomial using the custom engine. Using only optimized C code to perform the polynomial requires 114 times the energy of the custom engine. Any system performing compute-intensive tasks such as a DSP function or a system performing data encryption and decryption will not only perform the function faster, but consume orders of magnitude less power than performing the functions in optimized C code.



The Andes Technology E801 embedded core in Figure 2 contains a custom engine to solve the CRC polynomial. The internal pipeline of the CPU is outside the CPU data path, where the custom instruction logic can be added. This involves creating an execute interface to the CPU's pipeline. Thus, the designer can focus on new logic to implement the custom instruction. The Andes Custom Extension™ (ACE) framework makes this customization easier than other CPU cores offering custom instructions. With the easy-to-use ACE language, SoC designers can create instructions specific to their applications and optimize the performance and power consumption in a much shorter timeframe.

Custom Instructions Enable 10-Fold Power Savings for IoT Applications

By: Emerson Hsiao, Senior VP Andes Technology Corp.

One element that distinguishes devices for the emerging IoT market from the mobile devices of the mature handheld market is power. Specifically, while the latter can accept a battery recharge cycle of days, the former demands years between battery recharge/replacement. Where the two devices resemble one another is their need for high performance. While embedded CPU cores have concentrated on conventional techniques to save power—power islands and the like, another method that meets the power and performance requirement is the use of custom instructions to accelerate compute-intensive tasks. While some embedded CPU cores allow for custom instructions, the hurdle that has kept them from being developed is the engineering overhead in accommodating the custom logic with the software and hardware verification process.

Less than ten years ago, Andes Technology Corporation developed a new CPU architecture that overcomes this problem. This article will illustrate the effectiveness of custom instructions in saving power and explain how the barrier to incorporating a customized embedded core has been broken. The example chosen to illustrate the power of custom instructions is the CRC 32 polynomial commonly used in communications applications. (see table above left).

The extensible processor E801 (figure at left) allows SoC developers to incorporate functionalities and increase flexibility for SoC optimization. Through the Andes Custom Extension™ (ACE) framework language and COPILOT™ tool (Custom-OPtimized Instruction deveLOpment Tools), SoC developers can define custom instructions with ease and simplify the design process of extending RTL and simulation, thus allowing the instruction creation while avoiding tedious and error-prone design verification work. Custom instructions allow performance efficiency and provide protection for proprietary software IP. The ACE framework can be used in applications from DSP acceleration and high-volume data processing to emerging applications whose features and specifications are still evolving such as IoT, wearables, smart sensors, medical devices, storage, packet processing, intelligent household appliances, touch panels, wireless charging, fingerprint identification, SSD and encryption security chips.

The ACE framework language and COPILOT™ tools simplify the instruction design process. COPILOT also provides optional performance enhancement features, such as branch prediction, return address stack, and 3Read2Write register port. ACE supports instructions with either single- or multi-cycle latency and allows logic sharing among custom instructions to reduce cost.

Based on ACE descriptions, COPILOT generates the corresponding extended RTL, verification environment and relevant extension modules to be used with Andes standard development tools, simulator and AndesCore RTL. For SoC developers who need programmability and efficiency, ACE directly addresses their needs. Another benefit of using custom instructions is it increases the security of the chip by having proprietary hardware and software. Without knowing the implementation of the custom instructions, it is much harder for hackers to reverse or attack the hardware and software. For a presentation on the methods Andes employs for power savings, please view the video of a recent webinar on the topic.

Andes Technology Forms Knect.me™ New IoT Community to Provide Open-Source and Commercial IoT Solutions

This May, Andes Technology Corporation announced Knect.me, the new Internet of Things community that provides open-source, commercial solutions for connected devices. Knect.me community partners provide SoC IP platforms, software stacks, development boards, and development tools SoC developers need to build highly competitive IoT products to meet narrow, fast moving product windows.

"In the past year, many companies approached Andes seeking a partnership," said Charlie Hong-Men Su, Ph.D. Andes Technology CTO and Senior Vice President of R&D. "Because we understand that it takes multiple companies cooperating to fully exploit a market potential, Andes wanted to contribute to the expansion of the IoT market by providing enabling resources for developers. With this motivation in mind, we created a new website: knect.me. The site will connect chip vendors, partners, applications developers, and system vendors related to IoT. Knect.me will also bring together solutions for silicon IP, software stacks, tools, applications, system to help develop products that will connect to the world."

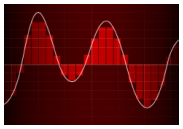
Andes is also creating the "IoT League." It will showcase successful products developed through the Knect.me community. "We're inviting Andes' customers to provide information on their products," said Frankwell Jyh-Ming Lin, Andes Technology President. "In return, IoT League participants will receive greater exposure and enhanced reputation in the IoT market. By showcasing a broad expanding array of applications, new prospects will be attracted to adopt products and solutions from Andes customers."

Knect.Me IoT Solutions

Andes and partners provides 4 key elements for Knect.me IoT solutions. The knect.me SoC IP Platform provides SoC developers with a complete solution and is comprised of the AndesCore™ and Andes platform IP along with partners' IP. The Knect.me Software Stack includes choices of open source software, and production-proven, certified and optimized software by Andes partners to fulfill a wide range of smart products and emerging applications development requirements. The Knect.me Development Boards include both flexible FPGA based boards with comprehensive functionality and interfaces, and compact chip-based Arduino-compatible boards with rich Arduino shields for extension capabilities. The Knect.me Development Tools include the AndeSight™ Lite IDE and Arduino IDE, plus the open source GNU toolchain for AndesCores. AndeSight Lite is a compact version of the Eclipse-based AndeSight IDE for free download. A no-cost evaluation version comes with all major functionality up to a code size of 32KB.

Evaluate Andes IP Cores

Andes has over 80 licensees and Andes-based products are shipping in more than a half a billion devices around the globe from licensees in Taiwan, Japan, Korea, and China. The company is expanding into the Americas.



If you have an SOC design in need of a low power, low cost MCU/CPU with full toolchain and peripheral support, contact us to arrange a free evaluation. Let us help with your next design. E-mail us at info@andestech.com.
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Andes Technology Corp.

Founded in March 2005, Andes Technology Corporation headquartered in SiSoft Research Center, Hsinchu, Taiwan is a leading Taiwan CPU intellectual property (IP) supplier, with over 80 licensees in Taiwan, Japan, Korea, and China that have shipped over a half billion units. Its products range from the entry level N7 and N8 with 2- and 3-stage pipelines, to the high-end N13 with 8-stage and longer pipelines. The mid-range N9 has the highest customer shipping volume while the mid-range N10 and high-end N13 support Linux and floating-point coprocessor. Configurable and extensible Andes cores enable designers to create unique designs. AndeSight™ IDE enable customers to efficiently develop, debug, tune and regress their software. AndeSoft™ provides customers optimized fundamental software such as OS, drivers, standard C libaries, middleware, etc. for rapid application development. The company has sales offices throughout Asia and the U.S.

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