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ANDES in Sight

ANDES TECHNOLOGY Newsletter

Contents

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Andes and SiFive are jointly promoting RISC-V

Two Leading RISC-V Suppliers Agree to Cooperate to Further Promote RISC-V Adoption while Continuing to Aggressively Expand the RISC-V Ecosystem. The two companies will each contribute their unique expertise in CPU development and support to expand the ecosystem for the RISC-V instruction set architecture (ISA) to enable a new era of processor innovation through open standard collaboration. **Design & Reuse** May 17, 2018 **Click to read more.**

Andes Technology Corporation Records a Cumulative 2.5 Billion SoC Shipments Containing Its CPU IP Since Inception

Andes Technology Corp., the leading Asia-based supplier of small, low-power, high performance 32/64-bit embedded CPU cores, announced that at the end of 2017, it has recorded a cumulative total of 2.5 billion SoCs containing its CPU IP. In 2017, the company said 590 million SoCs shipped worldwide containing its CPU IP. The 2017 shipments represented nearly 2.4 percent of the cumulative total SoCs shipped. **Design & Reuse** May 15, 2018 **Click to read more**

"Andes Preps RISC-V Core for Linux"

"In December, Taiwan-based IP provider Andes announced a technology transition of its own — to the emerging RISC-V architecture. Chief executive Frankwell Lin used his **keynote** at the event (**SOI Silicon Valley Symposium**) to announce that the company will release in July a version of its RISC-V-based N25 core for Linux." **Rick Merritt EETimes** April 27, 2018. **Click to read more**

Andes Teams with Imperas and UltraSoC for RISC-V

Ahead of the RISC-V Workshop in Barcelona May 7, 2018, Andes Technology inked deals with two suppliers to help support SoC development. Andes has picked UltraSoC for trace and debug technology and extended its relationship with simulation specialist Imperas Software. By Chris Edwards May 1, 2018 **Tech Design Forum** **Click to read more**