



ANDES in Sight

ANDES TECHNOLOGY Newsletter

Contents

- Andes Goes IPO, March 2017...P.1
- Andes New 64bit CPU IP.....P.2
- 1st Major CPU IP with RISC-V....P.2
- 2.0 Billion SoCs shipped.....P.3

ANDES Technology USA

2375 Zanker Road, Suite 210,
San Jose California 95131
Business: info@andestech.com

Publisher: Andes Technology Corporation
Chief Editor: Jonah McLeod



Andes Technology Corporation Files IPO On the Taiwan Stock Exchange

Andes Technology Corporation, the leading Asia-based supplier of small, low-power, high performance 32-bit embedded CPU cores, today filed an initial stock listing of 40,611,915 shares at a price of NT\$65.10 per share. The shares began trading on the Taiwan Stock Exchange Corporation (TWSE)—the driving engine of Taiwan's economic growth—on March 14, 2017, under the TWSE ticker symbol "6533.TW." Proceeds from the offering will be used to expand the company's R&D effort to fuel Andes' international expansion into the U.S. and Europe, and to increase its competitiveness in China, Korea, and Japan.

"In its short history, Andes Technology Corporation has reached a major milestone with its listing on the Taiwan Stock Exchange," stated Andes Chairman, Ming-

Kai Tsai. "Reaching this landmark is not an easy task, although from the beginning we knew it required patience in IP product and business development. I am glad to see Andes has now achieved initial success in the embedded processor IP industry." Andes President, Frankwell Jyh-Ming Lin declared, "Andes has several sources of revenue, including, among others, license fees to acquire the rights to use our CPU IP and royalty income on the sale of all semiconductor devices containing our IP. While the number of licensees has grown steadily since our founding, the increase in royalties has been significant, growing 10 fold from 2013 to 2016 and increasing 60 percent in the last quarter of 2016. This reflects our customers' success with their products containing our IP."

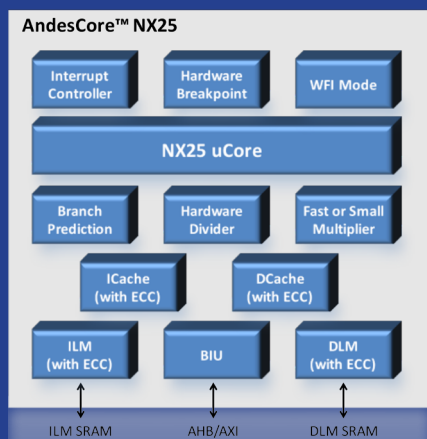
The company must have successfully developed a product or a technology

with market potential, and it must have obtained an appraisal opinion from Industrial Development Bureau in Taiwan, R.O.C. It must also have at least six months of proven trading records. This is accomplished by listing its shares on the TPEx Emerging Stock Board (ESB), where Andes has been trading since 2015. The company must be recommended in writing by a reputable securities underwriter. For the Andes IPO Horizon Securities Corporation provided this service.

In addition, the company must appoint independent directors, not less than two in number and not less than one-fifth of the total number of directors. Finally, company financial reporting must comply with the International Financial Reporting Standards (IFRSs).

Differentiation of AndeStar™ V5 Solution

Fully compliant with RISC-V, the AndeStar™ V5 architecture brings superset features unique to Andes and provides full support of the AndeSight IDE development tools. The Andes Custom Extension™ (ACE) environment simplifies the task of extending application-accelerating instructions for V5 by automatically generating all necessary development tools and housekeeping RTL code, and automatically verifying custom logic against its defined behavior. Products based on AndeStar™ V5, will support the extensive line of silicon-proven Andes SoC peripherals including



the Andes System Control Platform and have the benefit of Andes extensive validation for use with industry-standard EDA tool and libraries. AndeStar™ V5 provides support for address range over 4GB, AXI 64-bit interface, GCC compiler and GDB debugger—validated by strict industrial and Open Source test suites. AndeStar™ V5 is the comprehensive solution for customers to achieve optimum performance for their products and to shorten their development cycle.

The AndeStar™ NX25, based on AndeStar™ V5, will be available the third quarter this year. Also available will be the AndeSight™ integrated development environment for AndeStar™ V5-based SoC, pre-integrated System Control Processor platform with configurable interrupt controller supporting 1023 interrupt sources, Andes ADP-XC7 FPGA development board, and Andes Service and Support.

Andes Technology Corp. the First Mainstream CPU IP Provider to Adopt RISC-V Offers New 64bit Processor IP

Andes Technology Corporation, the leading Asia-based supplier of high performance, low-power, small embedded CPU cores serving 2-billion SoCs, today announced a new generation of the AndeStar™ architecture. In the process, Andes becomes the first mainstream CPU IP provider to adopt RISC-V, the open RISC Instruction Set Architecture (ISA) developed at the University of California

with area of only 67K gates and with power consumption as little as 17 μ W/ MHz in a TSMC 28nm process.



“Time-to-market is a major concern in every SoC design and one task that slows design progress is writing RTL code simply to integrate a collection of standard



Berkeley. Andes ISA, called AndeStar™ V5, supports 64-bits and the widely known RISC-V ISA as its subset and will bring the open, compact, and modular RISC-V into mainstream SoC applications.

The AndeStar infrastructure, evolved over the past 12 years includes advanced features such as CoDense™, PowerBrake, and StackSafe™, and application-specific architecture extensions such as Custom Extensions, DSP Extensions and Security Extensions, in addition to strong compiler optimizations for the optimal performance and code size. Adding 64-bit capabilities to Andes existing families of IP cores will satisfy new SoC's requirement for addressing memory over 4GB in applications such as high capacity storages, large-scale networks, deep learning and AI systems.

Leveraging Andes' history of industry leading performance-to-power ratio, SoCs with AndeStar™ V5 based cores will be able to run efficiently at high frequency. For example, the new V5 AndeStar™ NX25 in a typical configuration will deliver over 1GHz (in “worst case” conditions)

IP blocks and then spending an equal or greater amount of time verifying the new code” said Charlie Hong-Men Su, Ph.D., Andes Technology CTO and Senior Vice President of R&D. “With the new AndeStar™ V5 architecture, we provide a complete solution for 64-bit embedded SoC designs by bringing RISC-V compliance together with Andes' successful line of AndeStar™ V3 IP cores, convenient features (such as CoDense, PowerBrake and StackSafe) and architecture extensions (such as Custom Extensions, DSP Extensions and Security Extensions), standard Andes IDE software toolchain with comprehensive extended features, SoC peripherals, hardware developing platforms, service and support. Collectively, this helps to satisfy needs of design teams by significantly improving the product quality and reducing time-to-market and risk for production-ready 64-bit SoC designs. When Andes started to plan AndeStar™ V5, we considered the full scope of supporting an extended ISA, enabling customers to leverage fertile RISC-V ecosystem while maintaining the strengths we accumulated over time.”

Andes RISC-V Advanced 64-bit NX25 CPU Announced at Andes Embedded Forum Shanghai

Andes introduced its new NX25 64-bit CPU based on the innovative V5 instruction set architecture (ISA) at the Andes Embedded Forum being held at the Parkyard Hotel in Shanghai on May 10th. The new 64-bit V5 ISA provides a significant performance advance to address high end applications such as enterprise-class servers, routers, switches, WLANs, data center storage, artificial intelligence (Deep Learning), advanced driver assist systems (ADAS), AR/VR imaging, industrial automation and other high performance applications. The 64-bit architecture enables a vastly expanded address space of over 18 exabytes demanded by these applications.

"In its 12th year, the long-running, very successful Andes Embedded Forum is the venue for major announcements from Andes and its partners," said Andes President, Frankwell Jyh-Ming Lin.

"The forum begins in Shanghai at the Parkyard Hotel on May 10th, then travels to Beijing on May 12th and finally to Hsinshu, Taiwan on May 18th." Andes introduced its most innovative ISA thus far in its history and became the first major CPU IP vendor to adopt RISC-V. The 64-bit ISA will deliver impressive performance at a high clock rate while still taking up a small number of gates compared with other offerings in its class. Most importantly, it will consume much less power per MHz than alternatives on the market.

Evaluate Andes IP Cores

Andes has over 120 licensees and in 2016 Andes-embedded products shipped in more than 430 million devices around the globe from licensees in Taiwan, Japan, Korea, China, Europe, and USA. The company is expanding into the Americas.

If you have an SOC design in need of a low power, low cost CPU with full toolchain and peripheral support, contact us to arrange a free evaluation. Let us help with your next design. E-mail us at info@andestech.com. Andes Technology USA Corporation 2375 Zanker Road, Suite 210, San Jose California 95131

Andes Technology Corp. Records a Cumulative 2.0 Billion SoC Shipments Containing Its CPU IP Since Inception

Andes Technology Corporation (TPE:6533), the leading Asia-based supplier of small, low-power, high performance 32-bit embedded CPU cores, today announced that up to the end of

2016, the company has recorded a total of 1.9 billion SoCs containing its CPU IP. As of today, this number has already grown to above 2.0 billion. In 2016, the company reported

430 million SoCs shipped worldwide containing its CPU IP. The 2016 shipments alone represented over 20 percent of the total SoCs shipped. From 2013 to 2016, the company has enjoyed a 10 fold growth in shipment volume of IP cores in SoC devices.

Andes President, Frankwell Jyh-Ming Lin declared, "after several years of steadily increasing unit shipments growth, our customers are now in large volume production. More importantly, they continue to license our IP for next generation versions of their designs. The result is that Andes is seeing steadily increasing growth in royalty income and expect this trend to continue going forward. Andes' customers' SoCs are

shipping in a wide range of very high volume applications including WiFi, Bluetooth, touch screen controller, sensor hub, MCU, SSD controller, USB3.0 storage, and more."



Andes is also making inroads into the next generation of high volume designs now coming onto the market. These include automotive IoT and Innovative ADAS (Advanced Driver Assistance Systems). The company is targeting other

markets including robotics, augmented/virtual reality (AR/VR), voice recognition and deep learning, where the company reported last year a design win with innovative deep-learning start-up Wave Computing of Campbell, California.

Since 2005, Andes Technology has steadily developed highly efficient, low-power 32-bit embedded processors and associated SoC development platforms to shorten its customers time to market. In addition, the company continues to innovate next generation CPU architectures driven by existing and new customers' requirements and functionality demanded by rapidly evolving applications such as AR/VR, ADAS, and deep learning.

Andes Technology Corp.

Founded in March 2005, **Andes Technology Corporation** headquartered in SiSoft Research Center, Hsinchu, Taiwan is a leading Taiwan CPU intellectual property (IP) supplier, with over 120 licensees in Taiwan, Japan, Korea, China, Europe, and USA that have shipped over 2.0 billion units. Its products range from the entry level **N7** and **E8, S8** and **N8** with 2- and 3-stage pipelines, to the high-end **N13** with 8-stage and longer pipelines. The mid-range **N9** has the highest customer shipping volume while the mid-range **N10, D10**, and high-end **N13** support Linux and floating-point coprocessor. Configurable and extensible Andes cores enable designers to create unique designs.

AndeSight™ IDE enable customers to efficiently develop, debug, tune and regress their software.

AndeSoft™ provides customers optimized fundamental software such as OS, drivers, standard C libraries, middleware, etc. for rapid application development. The company has sales offices throughout Asia and the U.S.

2F, No.1, Li-Hsin First Road
Science-Based Industrial Park
Hsin-Chu City, Taiwan 300 R.O.C.

