



ANDES in Sight

ANDES TECHNOLOGY Newsletter

Andes Technology RISC-V Con in Santa Clara Sold out Success

Andes Technology Corp. sponsored [RISC-V Con](#) held on October 15 in Santa Clara, California was a sold-out success. Attendees received the first market analysis of the



significant potential the open-source RISC-V architecture affords from Jim Feldhan, Phoenix, Arizona-based market research firm President. The event began with Andes President Frankwell Lin detailing the fast-paced

growth of Andes RISC-V offering in the U.S. and the future potential the CPU ISA provided the company. CTO Charlie Su detailed the expanding Andes RISC-V product line and ease with which designers can optimize the ISA for accelerating functions, especially in AI applications. Vin Sharma, Head of Engineering for Amazon SageMaker Neo, AWS AI described how extensible AI Compiler SageMaker Neo makes it easy for developers to train machine learning models once and run them on various hardware platforms in the cloud and at the edge. Imperas Vice President Sales, Larry Lapidés described software-driven hardware design and verification for RISC-V processors and SoCs. VP of Field Application and Marketing, Kyle Weng, described Farada'sy RISC-V based ASIC Solution for Edge AI and IoT SoCs. The event concluded with a spirited panel discussion involving all the presenters and moderated by Jim Feldhan.

**Be on Hand at the RISC-V Summit when Andes Technology
Reveals its Latest RISC-V Innovations**



Be sure to join Andes Technology Corp. for the Annual [RISC-V Summit](#), December 10 - 12, 2019 at the San Jose Convention Center in San Jose, California. Charlie Su, CTO and EVP at Andes Technology Corp. will present "Andes RISC-V Processor Solutions: From MCU to Datacenters" at 4:10 PM on Tuesday December 10th. Andes Technology Managing



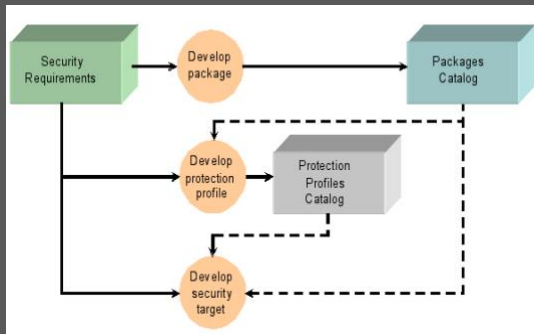
Director, Chuan-Hua Chang will be featured in the Poster Gallery on Expo Floor on Monday at 11:00 AM. On Tuesday, December 12, be sure to be in the Grand Ballroom 220-A at 2:30 PM for the Processor IP



Showcase with Kevin Chen, Senior Architect at Andes Technology.

Andes Technology and Tiempo Secure Announce Strategic Partnership to Enhance RISC-V Platform Security up to CC EAL5+ Certification

Andes Technology Corporation, a leading supplier of outstanding efficiency, low-power, high performance 32/64-bit embedded CPU cores, including a broad family of RISC-V cores, has entered into a strategic partnership with Tiempo Secure, a unique supplier of ISO/IEC 15408 standard CC (Common Criteria) EAL5+ (Evaluation Assurance Level) grade secure element IP, to bring the RISC-V based security solution up to CC EAL5+ certification. According to recent [Ericsson research](#), by 2024, there will be more than 22 billion connected IoT devices. While security based on separation mechanism is commonly deployed, it is admitted that there is some limitation in term of security certification. Furthermore, security integration into the IoT ecosystem could become complex.



The alternative is to enable security from tamper-resistant and certified hardware as a

security enclave (Secure Element IP) into the MCU or SoC design. Tiempo Secure has developed a Secure Element IP (TESIC) as a hard macro integrating CC EAL5+ grade state-of-the-art security countermeasures and security sensors against side-channel and intrusion attacks. The integration of this Secure Element IP into a RISC-V SoC will bring the security of this SoC up to CC EAL5+ security, without compromising on power consumption.

Andes and Dover Microsystems Partner to Deliver Professional Network Security Solution for RISC-V

Andes Technology and Dover Microsystems, the first company to immunize processors against entire classes of network-based attacks, announced a strategic partnership to deliver



The RWX micropolicy provides fine-grained access control by tagging each word in memory with metadata that defines read, write, and execute permissions.

professional network security solution for RISC-V. [Dover's CoreGuard® technology](#) is the only

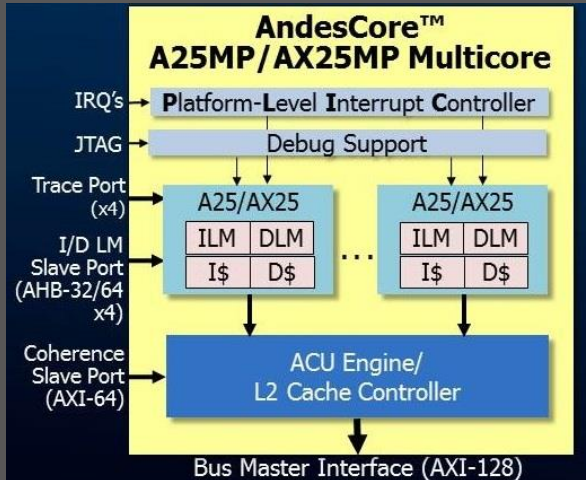
solution for embedded systems that prevents the exploitation of software vulnerabilities.

Dover's CoreGuard silicon IP integrates with Andes RISC-V processors to protect against 94 percent of known software vulnerabilities, including 100% buffer overflows, code injection, and data exfiltration as well as safety violations.

Dover Microsystems' CoreGuard silicon IP acts as a bodyguard to the host processor, monitoring every instruction executed to ensure that it complies with a defined set of security, safety, and privacy rules - called micropolicies - that precisely define allowed versus disallowed behavior. CoreGuard maintains micropolicy-relevant metadata about every word in memory, and then uses this metadata to crosscheck each instruction processed against the installed set of micropolicies. If an instruction violates any micropolicy, CoreGuard Policy Enforcer hardware stops it from executing before any damage is done. CoreGuard Policy Enforcer RTL is licensed and delivered as a set of hardware SystemVerilog design files. Dover includes the base set of CoreGuard micropolicies that protect all embedded systems.

Andes Technology Features 32-bit A25MP and 64-bit AX25MP RISC-V Multicore Processors with Andes Custom Extension at TSMC 2019 Open Innovation Platform® Ecosystem Forum

At the TSMC 2019 Open Innovation Platform® Ecosystem Forum, on September 26, 2019 at the Santa Clara Convention Center, Andes Technology featured its latest



generation 32-bit A25MP and 64-bit AX25MP RISC-V Multicore Processors with Andes Custom Extensions, that allows designers to create special instructions to accelerate compute intensive functions, a capability highly desired in AI and ADAS designs. The cache coherent A25MP and AX25MP RISC-V multicore processors are the company's first with comprehensive DSP instruction extension based on the RISC-V P-extension draft Andes donated to the RISC-V Foundation.

“The A25MP and AX25MP have already achieved major design wins in high-performance artificial intelligence applications and the product family has seen strong interest from Fortune 500 companies,” said Andes Technology Corp. President, Frankwell Lin. “Multiple processor cores extended with Andes Custom Extensions working in parallel enable computation-intensive applications, such as artificial intelligence and Advanced Driver-Assistance Systems (ADAS) to significantly boost their performance. Furthermore, the DSP/SIMD ISA, executing the CIFAR-10 dataset (Canadian Institute For Advanced Research) image classification benchmark for machine learning achieved an order of magnitude performance boost. It also achieved 7 times acceleration in the PNET for MtCNN (Multi-task Cascaded Convolutional Networks) face detection and alignment algorithm.”

SEGGER Makes Its Entire Ecosystem of Tools Available for AndesCores

SEGGER, a leading supplier of software libraries, development tools, debug probes and flash programmers, together with Andes Technology, a founding member of the RISC-V Foundation and a leading supplier of 32/64-bit embedded CPU cores, today announced their collaboration to support the complete development process of embedded systems based on Andes RISC-V CPUs with easy to use, efficient and reliable, tools and libraries.



The entire palette of [SEGGER software libraries](#), from the RTOS embOS to file system, compression, graphics library, security, communication and IoT, as well as SEGGER's integrated development environment Embedded Studio, already support all of Andes RISC-V processors. SEGGER's J-Link debug probes and Flasher flash programmers currently support Andes RISC-V 32-bit CPU cores, including N25F, D25F, and A25, with support for 64-bit CPU cores in the works.

"We are excited to cooperate with Andes," says Ivo Geilenbrügge, Managing director of SEGGER. "Our software tools and libraries, especially J-Link and Embedded Studio, significantly enhance the Andes RISC-V ecosystem. We offer a comprehensive one-stop solution for firmware and application developers."

"We are excited to partner with SEGGER and have their entire product palette available to our RISC-V cores," comments Dr. Charlie Su, CTO and Executive VP, Andes Technology Corporation. "SEGGER provides a complete ecosystem for all embedded needs. With J-Link and Embedded Studio, Andes now has the leading development solution. Fast and powerful: It simply works. Together, we offer powerful solutions for Andes V5 RISC-V extended ISA to serve diversified SoCs from our customers."
