Andes Technology Corp.
Investor Conference Report
Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
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03 Product Applications
04 New Products and Ecosystems
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Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Nearly 400 people, 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)
- EE Awards - “Taiwan-Product Award” & ”Asia-Company Award” (2021)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning
Business Status Overview

- **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed

- **AndeSight™ IDE:**
  - **24,000+** installations

- **Eco-system:**
  - **500+** partners

- **12B+** Accumulative SoC Shipped
2022 Revenue Analysis

YoY
+13.7%

(NT$ thousands)

Q1-Q4 2021: 819,778
Q1-Q4 2022: 931,821
2022 Top 10 Customers Analysis by Revenue

Top 10 Customer Contributed 58% Revenue

(NT$ thousands)
2022 Royalty Analysis

YoY -1.7%

(NT$ thousands)

Q1-Q4 2021: 233,676
Q1-Q4 2022: 229,725
2022 Top 10 Royalty Contributors Analysis by Application

Top 10 Royalty Customers Contribution Analysis: 86%

(NT$ thousands)
2022 Revenue Analysis by Payment Model

- License Fee: 60%
- Running Royalty: 24%
- Maintenance: 15%
- Others: 1%
2022 Revenue Analysis by Region

- Taiwan: 36%
- USA: 32%
- China: 25%
- Korea: 4%
- Europe: 2%
- Japan: 1%
2022 Revenue Analysis by Product

- RISC-V: 34%
- V3: 66%

Other product segments include N25, N8, N9, AX45, AX545, ACE, A45, Customized IP, NX27, N13, D25, N45, D45, N10, NX25, D10, AX25, E8, LLVM, AE250, A27, and OTHERS.
2022 Q1-Q4 Net Income Analysis

2022 EPS: 7.03
2021 EPS: 3.59

YoY +120.2 %

(Unit: NT$K)

Q1-Q4 2021: 161,665
Q1-Q4 2022: 355,937

RISC-V
Historical Revenue Analysis

License

Royalty

(NT$)
Product Applications

http://www.andestech.com
V5 Adoptions: From MCU to Datacenters

- **Edge to Cloud**
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)
- **40nm to 5nm**
- **Many in AI**

- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells
Andes RISC-V Cores Adopted in SoC

- single core
- 2-8 cores
- > 30 cores
- > 100 cores
- > 1000 cores
Andes RISC-V Product Roadmap

**RV32/RV64**
- **A25MP**
- **AX25MP**

**Cache-Coherent 1-4 Cores**

**Linux with FPU/DSP**
- **A25**
- **AX25**

**Fast/Compact with FPU/DSP**
- **N25F**
- **D25F**
- **NX25F**
- **N25F-SE**
- **D25F-SE**

**5-stage (1.1 GHz)**

**Vector Ext. MemBoost**
- **NX27V**
- **A27/AX27**
- **A27L2/AX27L2**

**5-stage (1.1 GHz)**

**27-Series: Vector Ext. MemBoost**

**Superscalar**
- **45-Series: Dual Issue Vector Ext. MemBoost**
- **N45/NX45/D45**
- **A45/AX45**
- **A45MP/AX45MP**
- **NX45V, AX45MPV** (1024-bit VPU, 1-8 Cores)

**8-stage (1.2 GHz)**

**Out of Order**
- **60-Series:**
  - > 2.5 GHz
  - > 2x per-GHz performance of 45-Series
  - **AX65**

**Leading positions:**
- The 1st company offering commercial RVP DSP CPU
- The 1st company offering the most updated spec of commercial RVV vector processor
- The 1st RISC-V core certified with ISO 26262 full compliance
- Tools for RISC-V custom extension: ACE

**NEW**
AX45 Can Do More (vs. 64bit A-series)

**A53**
- 8-stage In-Order Dual Issue
- Widely adopted by industries in many applications

**AX45**
- 8-stage In-Order Dual Issue
- **Performance is better!**
  - Coremark/MHz: 1.35x
  - Dhrystone/MHz: 1.42x
Target Applications for 27 & 45-Series

- AI/Deep Learning
- AR/VR
- 5G
- Networking
- Storage
- Video Surveillance
- ADAS
- V2X (Vehicle to Everything)
- IVI (In-Vehicle-Infotainment)

Metaverse and more...
Toward 2023: New Products and Ecosystems

http://www.andestech.com
**AndesCore™ Lineup** with Industry’s 1st RISC-V Cores

- **D25F**: with **SIMD/DSP capability** (P-extension, 32/64 bits)
- **NX27V**: with **Vector Processing Unit** (V-extension, up to 512 bits)
- **N25F-SE**: with **ISO 26262 Full Compliance**, not just *Ready*

<table>
<thead>
<tr>
<th>Categories</th>
<th>Embedded Control</th>
<th>DSP/Vector</th>
<th>Linux AP</th>
<th>FUSA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>45 Series</strong></td>
<td>N45, NX45</td>
<td>D45</td>
<td>A45(MP)</td>
<td>AX45(MP)</td>
</tr>
<tr>
<td>8-stage superscalar</td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>27 Series</strong></td>
<td></td>
<td>NX27V</td>
<td>A27(L2)</td>
<td>AX27(L2)</td>
</tr>
<tr>
<td>5-stage MemBoost</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-stage fast &amp; compact</td>
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<tr>
<td><strong>Entry Series</strong></td>
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<table>
<thead>
<tr>
<th>References</th>
<th>A53/55, R52/82, M7</th>
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</thead>
<tbody>
<tr>
<td><strong>27 Series</strong></td>
<td>A5/7/35</td>
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<tr>
<td>5-stage MemBoost</td>
<td></td>
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<tr>
<td><strong>25 Series</strong></td>
<td>A5/7/35, R4/5, M4/33</td>
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<tr>
<td>5-stage fast &amp; compact</td>
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<td><strong>Entry Series</strong></td>
<td>M0/0+/3/33/4</td>
</tr>
<tr>
<td><strong>Categories</strong></td>
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# AndesCore™ Roadmap Processors

<table>
<thead>
<tr>
<th>Series</th>
<th>Categories</th>
<th>13-stage OOO MP</th>
<th>8-stage Superscalar</th>
<th>5-stage MemBoost</th>
<th>5-stage Fast&amp;Compact</th>
<th>5-stage</th>
<th>Safety Enhanced (SE) Series: at least one per year</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>AX60 Series</strong></td>
<td>Power-efficient</td>
<td>AX65</td>
<td>AX67</td>
<td>60-SE</td>
<td>45-SE</td>
<td>25-SE</td>
<td><strong>New Processors:</strong> AX65, AX45MPV, D23, D25F-SE</td>
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<td><strong>45 Series</strong></td>
<td>Power-efficient</td>
<td>AX45, NX45</td>
<td>NX45V*</td>
<td>AX45MPV</td>
<td>A53/55, R52/82, M7</td>
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<tr>
<td><strong>27 Series</strong></td>
<td>Power-efficient</td>
<td>NX27V</td>
<td>A27(L2), AX27(L2)</td>
<td>A5/7/35</td>
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<tr>
<td><strong>Entry Series</strong></td>
<td>Power-efficient</td>
<td>N22</td>
<td>D23</td>
<td>M0/0+/3/33/4</td>
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<tr>
<td><strong>Categories</strong></td>
<td>Power-efficient</td>
<td>Mid-range</td>
<td>Extended</td>
<td><strong>References</strong></td>
<td><strong>FUSA</strong></td>
<td><strong>Note:</strong> AX45MPV configured as one core</td>
<td></td>
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</tbody>
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New Processors: AX65, AX45MPV, D23, D25F-SE

Safety Enhanced (SE) Series: at least one per year
AndesCore™ AX65
Multicore Out-of-Order Superscalar Processor
The Andes AX60 Processor Series

■ A new generation of AndesCore™
  ● Advanced Performance 13-stage Out-of-Order Superscalar Multicore
  ● Latest RISC-V Architecture
  ● Supported by Andes Long-term Roadmap
    – AX65 as the first member of the AX60 series
    – More products based on the AX60 micro-architecture planned, including for automotive functional safety

■ AndesCore™ AX65
  ● Offering performance surpassing CA72
  ● > 2.5 GHz, > 2x per-GHz performance of AX45MP
  ● Engaging with early customers
## Preliminary Performance Results

<table>
<thead>
<tr>
<th>AndesCore</th>
<th>AX27L2</th>
<th>AX45MP (over AX27L2)</th>
<th>AX65 (over AX45MP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro-architecture</td>
<td>5 stage scalar in-order</td>
<td>8 stage dual-issue in-order</td>
<td>13 stage quad-issue OOO</td>
</tr>
<tr>
<td>Freq. (7nm)</td>
<td>~2 GHz</td>
<td>&gt;2 GHz</td>
<td>&gt;2.5 GHz</td>
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<tr>
<td>Coremark/MHz</td>
<td>3.55</td>
<td>5.64 (+59%)</td>
<td>9.17 (+63%)</td>
</tr>
<tr>
<td>Specint2k6/GHz</td>
<td>2.82</td>
<td>3.46 (+23%)</td>
<td>&gt; 7 (&gt;2x, target)</td>
</tr>
<tr>
<td>EEMBC FPMark/MHz</td>
<td>27.0</td>
<td>35.2 (+30%)</td>
<td>66.6 (+89%)</td>
</tr>
<tr>
<td>Linpack MFLOPS/MHz</td>
<td>0.130</td>
<td>0.220 (+69%)</td>
<td>0.613 (2.8x)</td>
</tr>
<tr>
<td>Mem Bandwidth(^1)/MHz</td>
<td>1.0x</td>
<td>1.47x</td>
<td>1.90x</td>
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</tbody>
</table>

1. Based on standard library memcpy
AndesCore™ AX45MPV
Multicore 1024-bit Vector Processor
AX45MPV: Linux Multicore Vector Processor

- A new member of popular AndesCore™ 45-series processors
  - Inherits all features of AX45MP and leverages 3+ years of field experience from NX27V vector engine
  - 64-bit 8-stage dual-issue processor
  - Up to 8 cores SMP supporting up to 8MB L2 cache
  - Dual-issue 1024-bit Vector Processing Unit (VPU) delivers up to 6 results per cycle

- AndesCore™ AX45MPV
  - Targets AI inference/training, ADAS, AR/VR, computer vision, multimedia
  - Engaging with early customers
AndesCore™ D25F-SE / N25F-SE

Automotive Functional Safety (FUSA)
Andes is *Driving* Innovations in Automotive

with Industry’s 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

- **In-Cabin Radar**
  - Radar Subsystem: N25F-SE
  - Host Controller: N25F-SE
  - Memory: Peripheral

- **CMOS Sensor**

- **Auto TDDI**

- **Auto MCU**

- **Auto Storage**
## ISO 26262 Certification for Development Process: ASIL-D
- In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH

## ISO-9001 QMS achieved and maintained since 2010

## ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE
- ISO 26262-2,4,5,8,9
- Covers all the sections applicable to CPU core

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### General Information

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### Certificate Details

<table>
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<tbody>
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</table>

### Technical Data/Parameter

- **ASIL B Compliant Certification for N25F-SE**
- **N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor**

### Process Details

- **Development process for Functional Safety related components up to ASIL D**
- **Version V1.0 (202011)**

### Specific Requirements

- **Technical Data/Parameter**
- **ASIL B requirements**

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### ISO 26262-2,4,5,8,9

- Covers all the sections applicable to CPU core
D25F-SE: FuSa processor with DSP/SIMD capability

- **CPU Core**
  - AndeStar™ V5 Instruction Set Architecture (ISA)
    - RISC-V 32-bit, RV32GC + Andes Extensions
    - RISC-V P(draft) and B extensions.
    - Machine+User (M+U) privilege levels
  - Dynamic branch prediction with BTB, BHT, RAS
  - CoDense™ code size reduction, StackSafe™ stack protection

- **Memory Subsystem**
  - Support I/D cache up to 32KB each
  - Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses

- **Bus Interfaces**
  - AXI or AHB bus master port
  - N:1 CPU clock vs. bus clock ratio

- **Others**
  - Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface

- **Safety Package including Safety Manual & FMEDA report**
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**Safety Package including Safety Manual & FMEDA report**
D25F-SE with DSP and Bit-manipulation

- RVP: Powerful DSP/SIMD instructions for audio/voice codec and endpoint AI/ML
- SIMD instructions such as a quad 8 x 8 accumulated into 32-bit data
- DSP library support of over 200 functions

![Speedup of RVP over Baseline](chart)

- RVB: Efficient bit-manipulation operations for codes such as cryptographic & checksums
  - Latest RVB ISA-extension Ver 1.0.0, including:
    - address generation, basic bit-manipulation, carry-less multiplication and single-bit instructions
    - Accelerate Crypto calculations: 27% improvement on SHA256, 19% for AES, 16% for MD5
AndesCore™ D23
Compact, Secure, Low-Power Controller
D23 Targets Diverse Embedded & IoT Applications

<table>
<thead>
<tr>
<th>Applications</th>
<th>D23 Capability fit</th>
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<tbody>
<tr>
<td>DDI, TDDI</td>
<td>Small gate count</td>
</tr>
<tr>
<td>Wireless controller core (WiFi, BT or others)</td>
<td>Security, small gate count</td>
</tr>
<tr>
<td>Smart Home Appliance</td>
<td>Security, performance, small gate count</td>
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<tr>
<td>Wearable</td>
<td>DSP (Edge AI), Security</td>
</tr>
<tr>
<td>E-Toys</td>
<td>DSP (Speech and Sound Processing)</td>
</tr>
<tr>
<td>RF Sensor control</td>
<td>DSP (Edge AI, Front-End Signal/Protocol Stack Processing)</td>
</tr>
<tr>
<td>MEMS/Sensor Fusion</td>
<td>DSP (Edge AI, Front-End Signal processing)</td>
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<tr>
<td>Battery or charging control</td>
<td>Performance</td>
</tr>
<tr>
<td>Advanced Motor Control</td>
<td>DSP</td>
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RISC-V: 2022 Toward 2023 & Beyond
- New Application Market

http://www.andestech.com
## RISC-V Technology 2022 to 2023
- Drive Progression and Closure on Specs and Technical Deliverables

<table>
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<th>Item</th>
<th>2022</th>
<th>2023</th>
<th>% change</th>
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<td>TGs</td>
<td>33</td>
<td>40</td>
<td>25%</td>
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<tr>
<td>SIGs</td>
<td>23</td>
<td>28</td>
<td>25%</td>
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<tr>
<td>ISA Spec Ratifications</td>
<td>2</td>
<td>20</td>
<td>1000%</td>
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<tr>
<td>non-ISA Spec Ratifications</td>
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<td>11</td>
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<tr>
<td>Profiles</td>
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<td>6</td>
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<tr>
<td>Platforms</td>
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Google Announced

Android RISC-V Support

Date: 2023-01-07
2023 & Beyond

- Google Android will be ported to RISC-V
- The ecosystem will get more mature in 3 years
- Andes is committed in making its high end RISC-V CPU running Android in quality
  - For example, 45 series AX45MP, 60 series AX65, and more higher end RISC-V cores
- ChatGPT is hot yet “mainframe” style deployed, OpenAI put it in one neuro-network type of AI system
  - Future trend is to make AI “edge” style or “personal” style, which will lead to further Edge AI revolution, SoC is still solution for future deployment
- Andes will deliver such solution in terms of core hardware, developing platform, and software ported
Thank You

http://www.andestech.com
+886-3-5726533