



# Andes Technology Corp. Investor Conference Report



# Safe Harbor Notice

---

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.



# Table of Contents



**01**

**Company Overview**



**02**

**Operation Results**



**03**

**Product Applications**



**04**

**New Products and Ecosystems**



**05**

**Concluding Remarks**



# Company Overview

<http://www.andestech.com> 

## Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Nearly 400 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)
- EE Awards - “Taiwan-Product Award” & “Asia-Company Award” (2021)

## Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

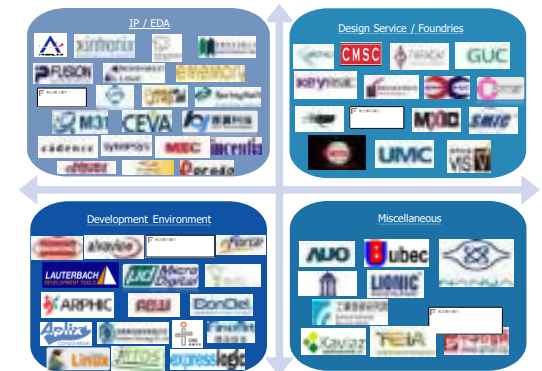
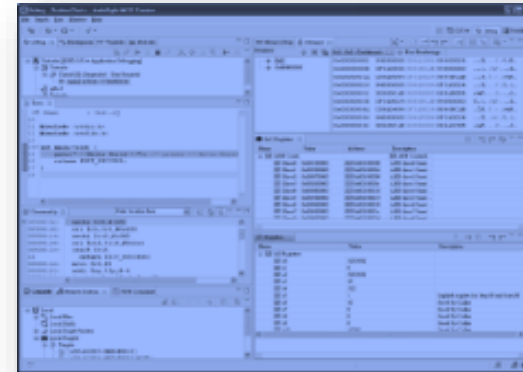
## Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning



# Business Status Overview

- ❖ **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed
- ❖ AndeSight™ IDE:
  - **24,000+** installations
- ❖ Eco-system:
  - **500+** partners
- ❖ **12B+** Accumulative SoC Shipped



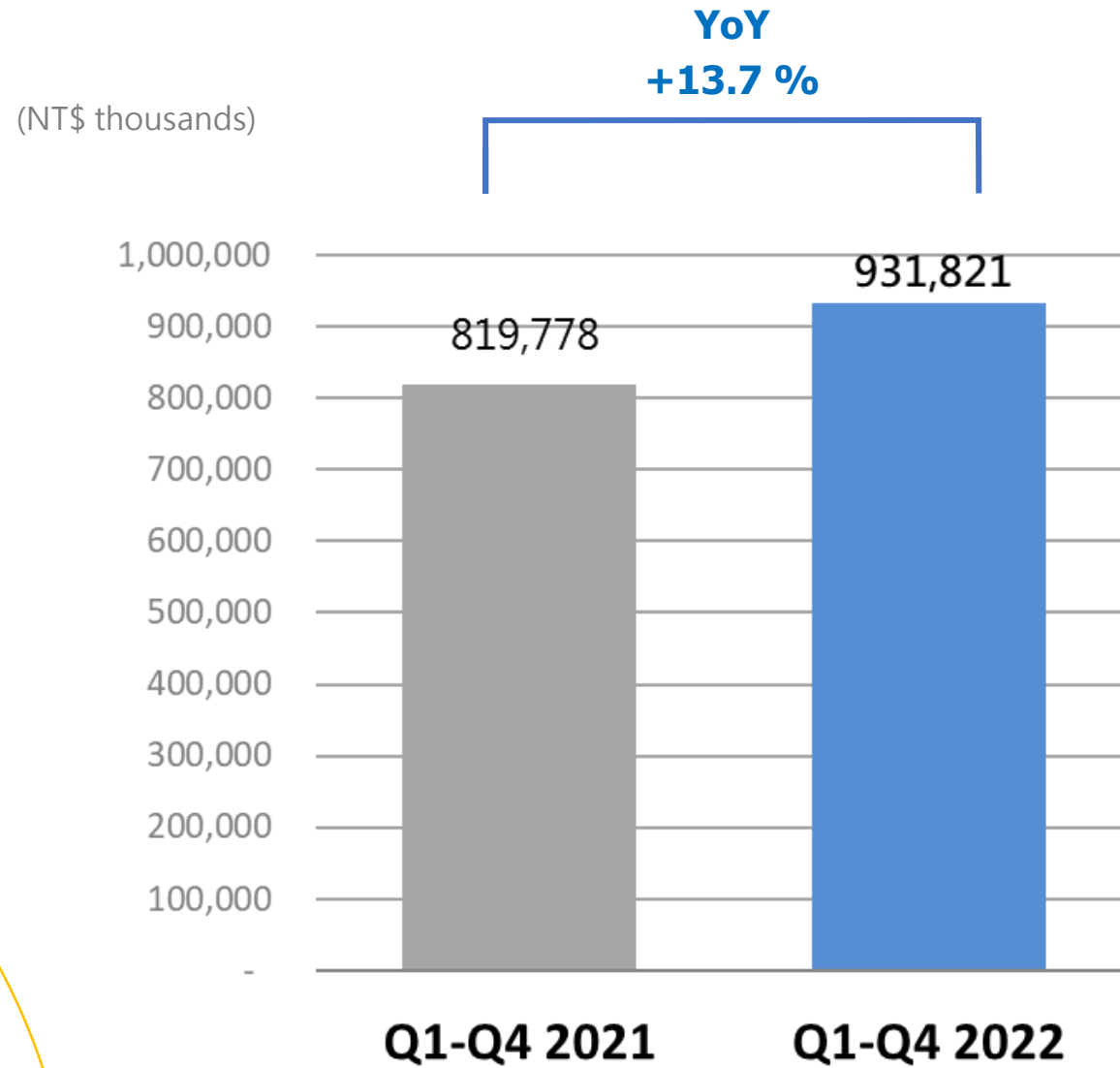


# Operation Results

<http://www.andestech.com>



# 2022 Revenue Analysis

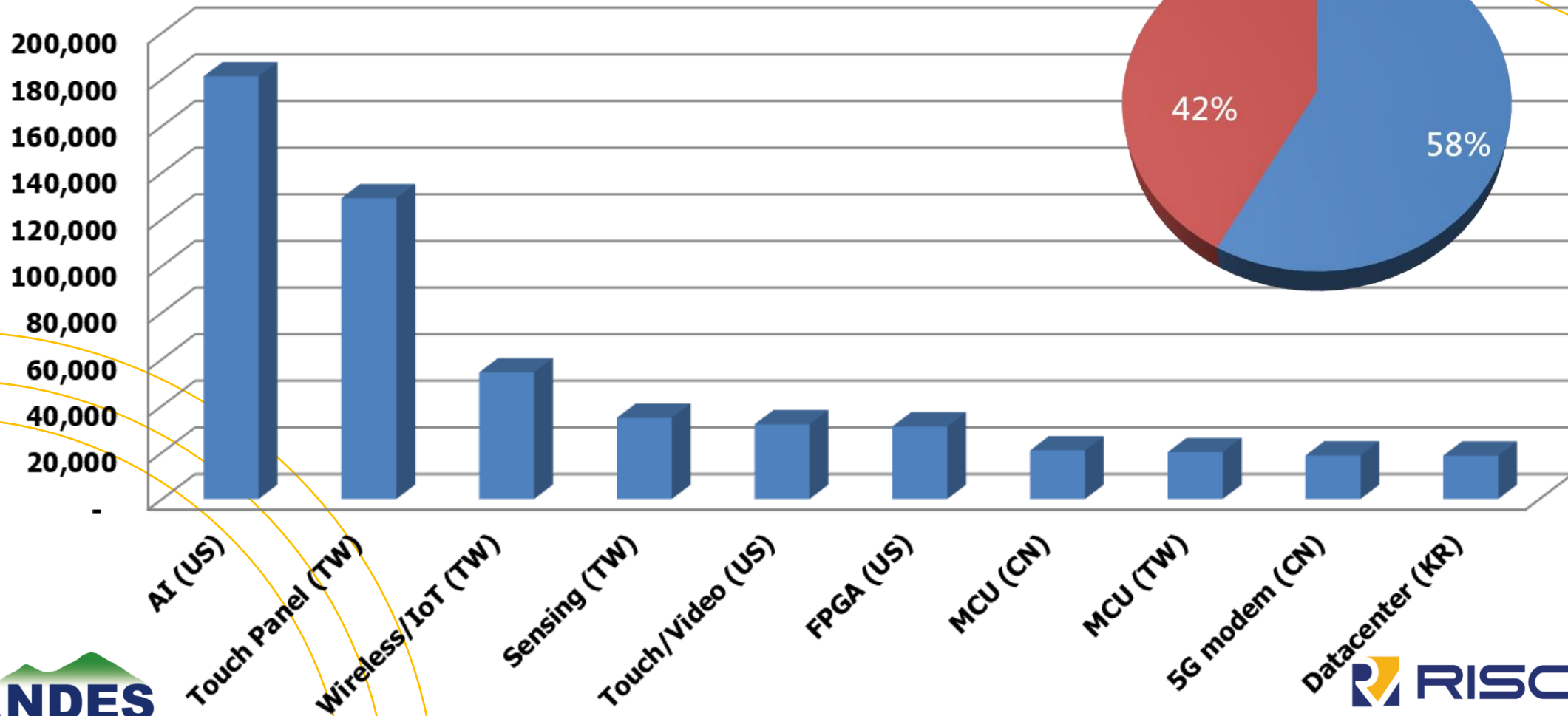




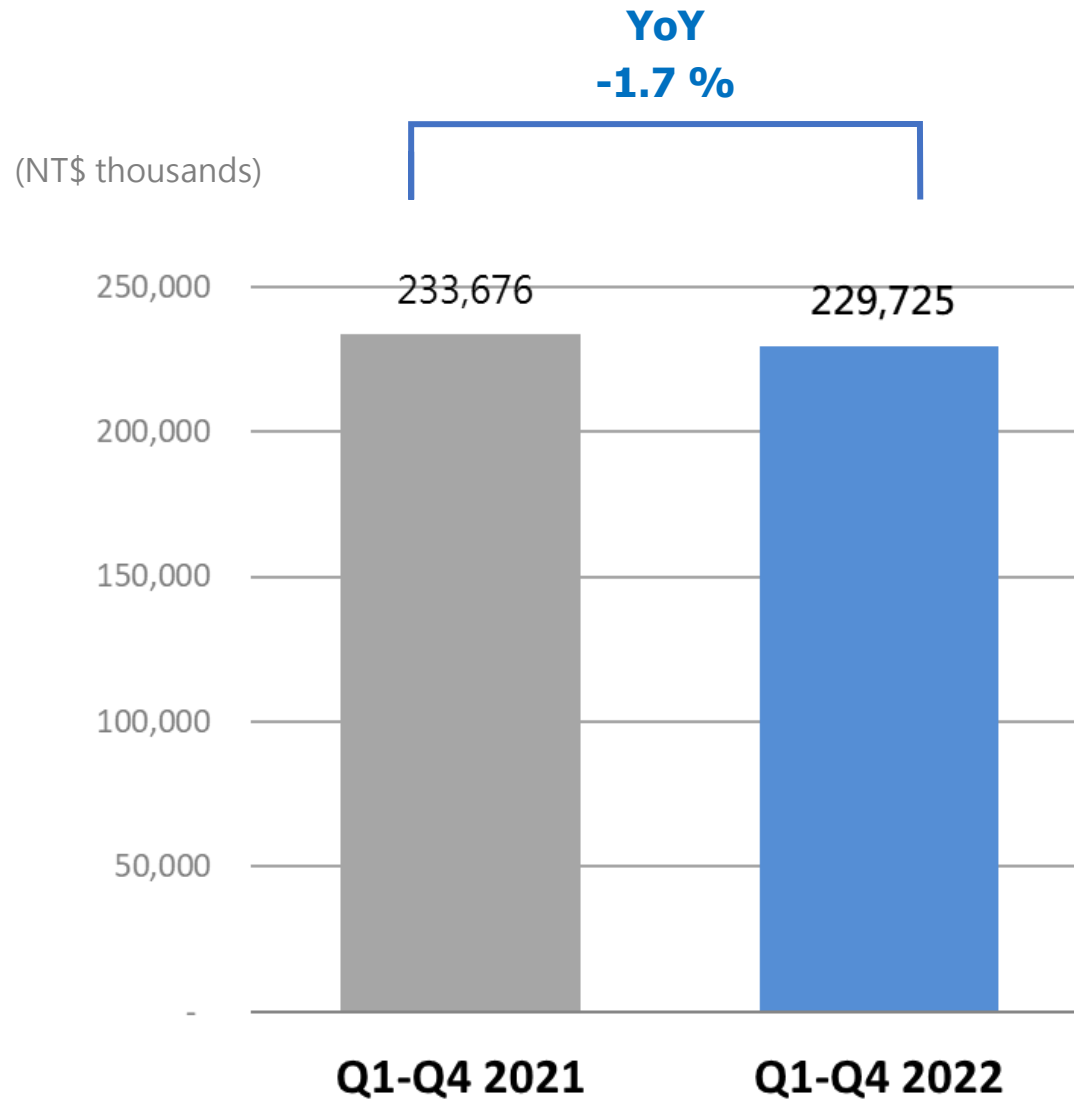
# 2022 Top 10 Customers Analysis by Revenue

Top 10 Customer Contributed 58% Revenue

(NT\$ thousands)

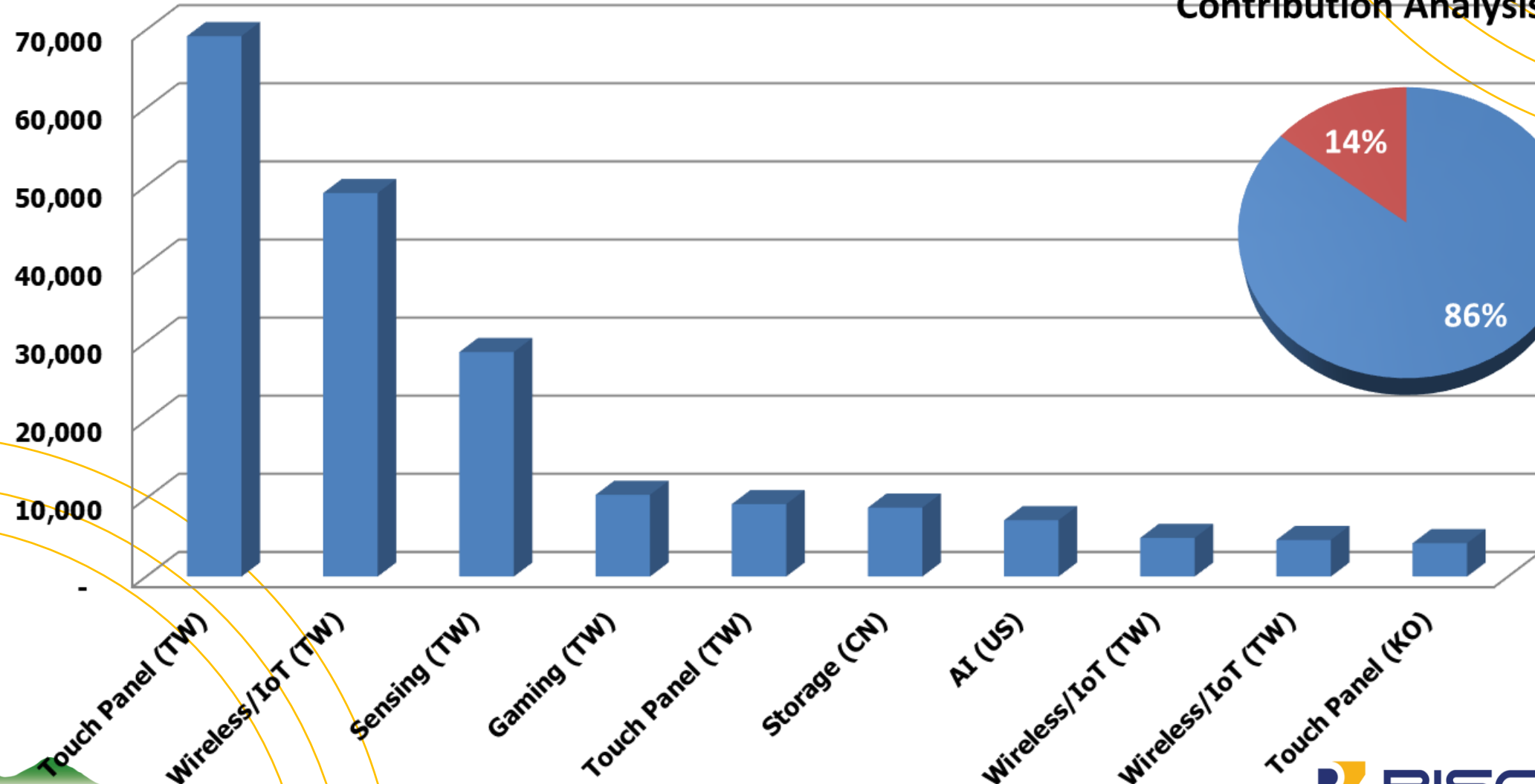


# 2022 Royalty Analysis

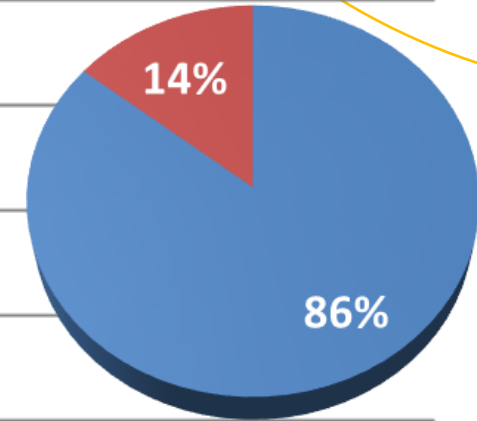


# 2022 Top 10 Royalty Contributors Analysis by Application

(NT\$ thousands)



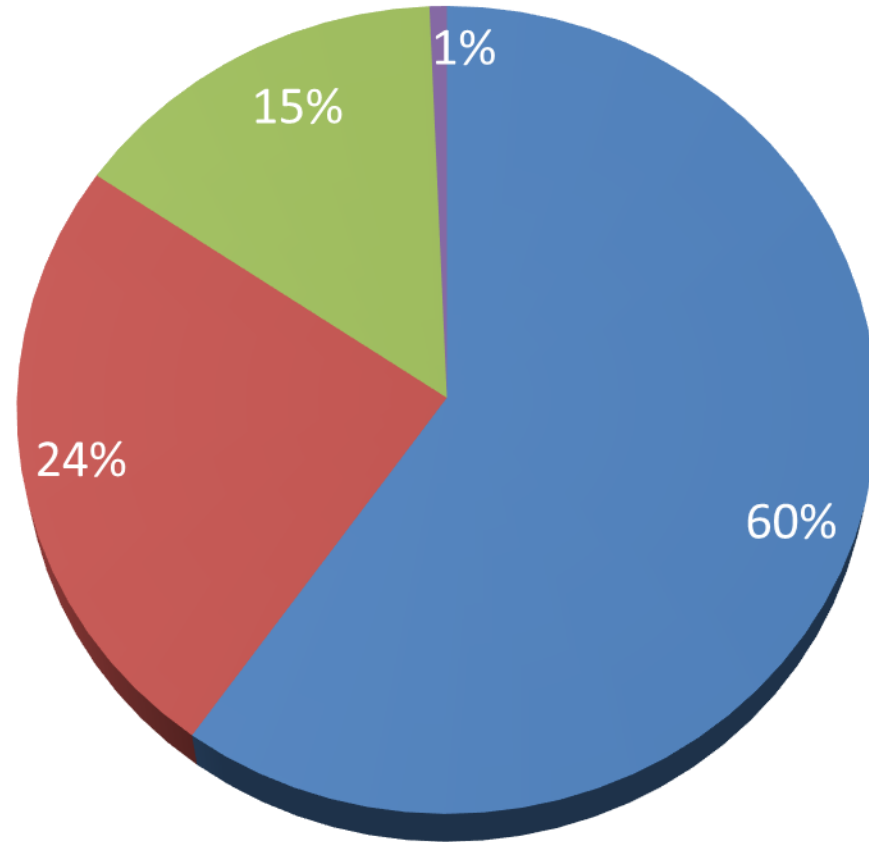
Top 10 Royalty Customers  
Contribution Analysis: 86%





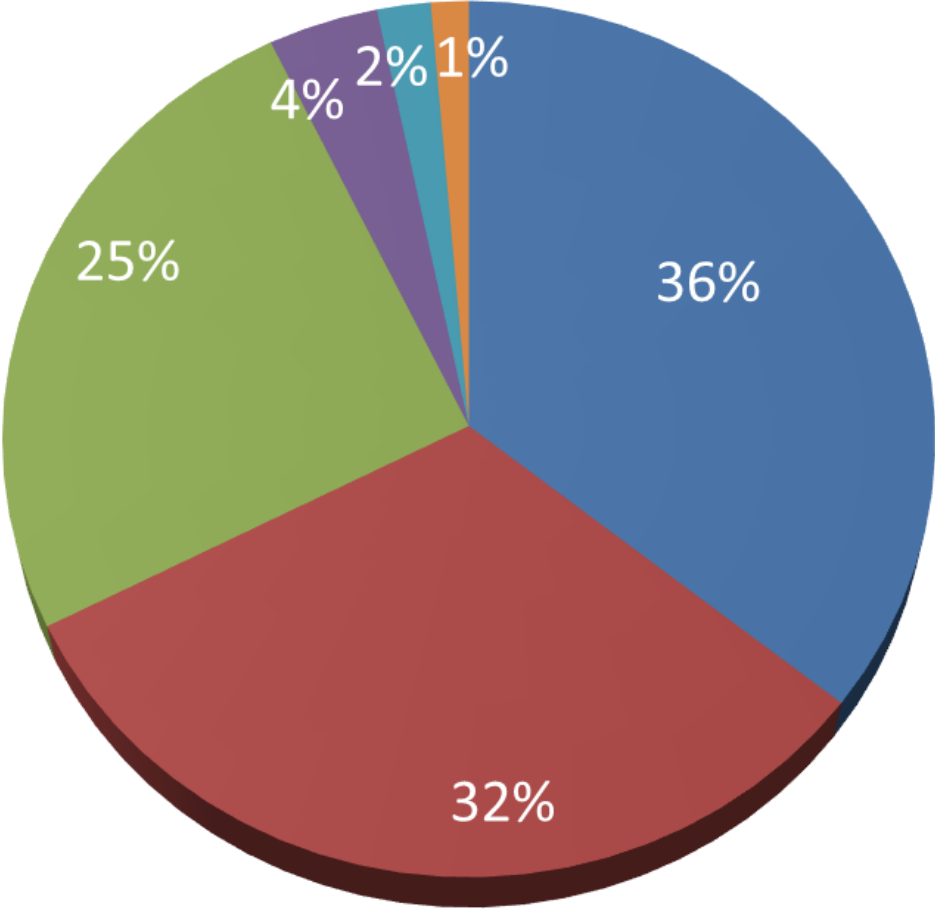
# 2022 Revenue Analysis by Payment Model

■ License Fee ■ Running Royalty ■ Maintenance ■ Others

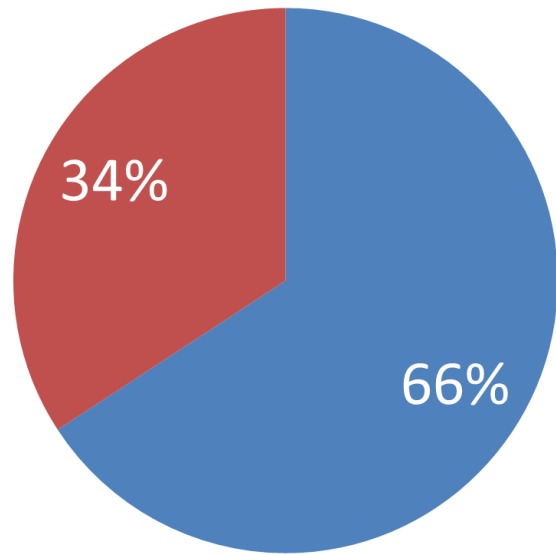


# 2022 Revenue Analysis by Region

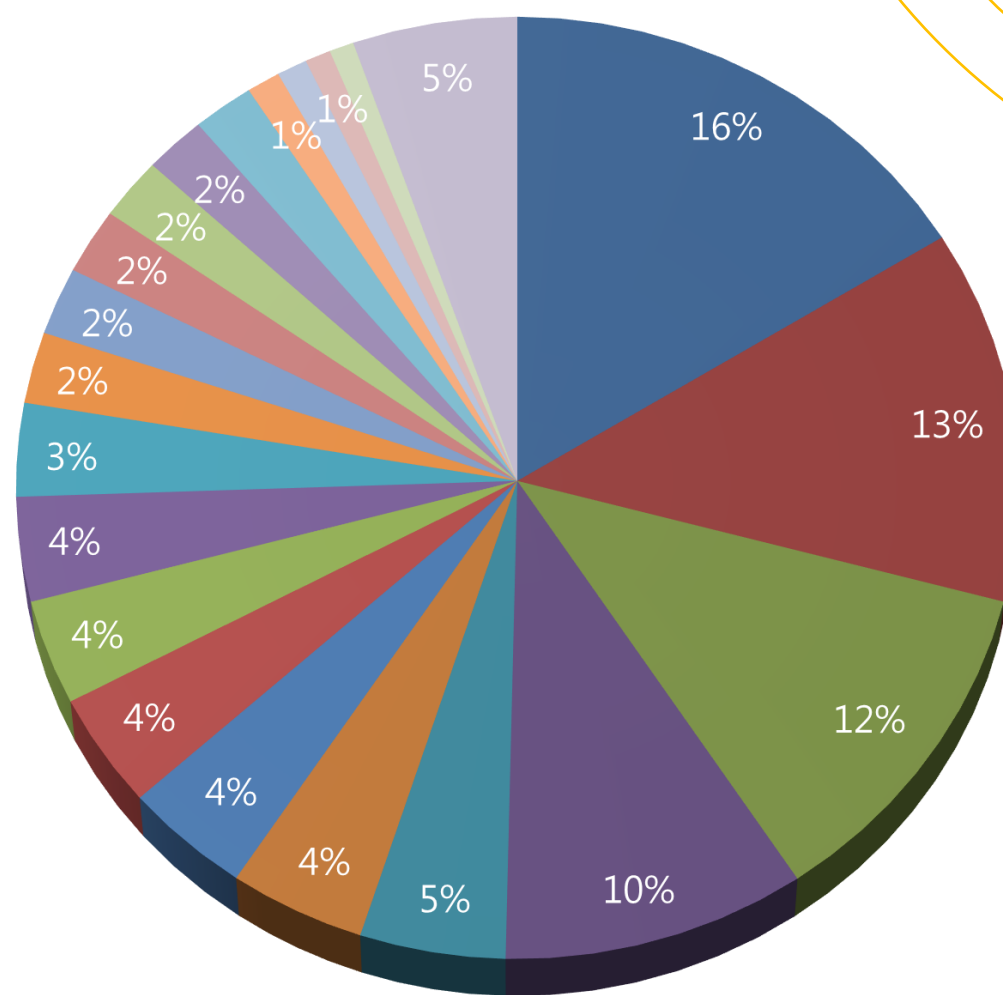
Taiwan USA China Korea Europe Japan



# 2022 Revenue Analysis by Product



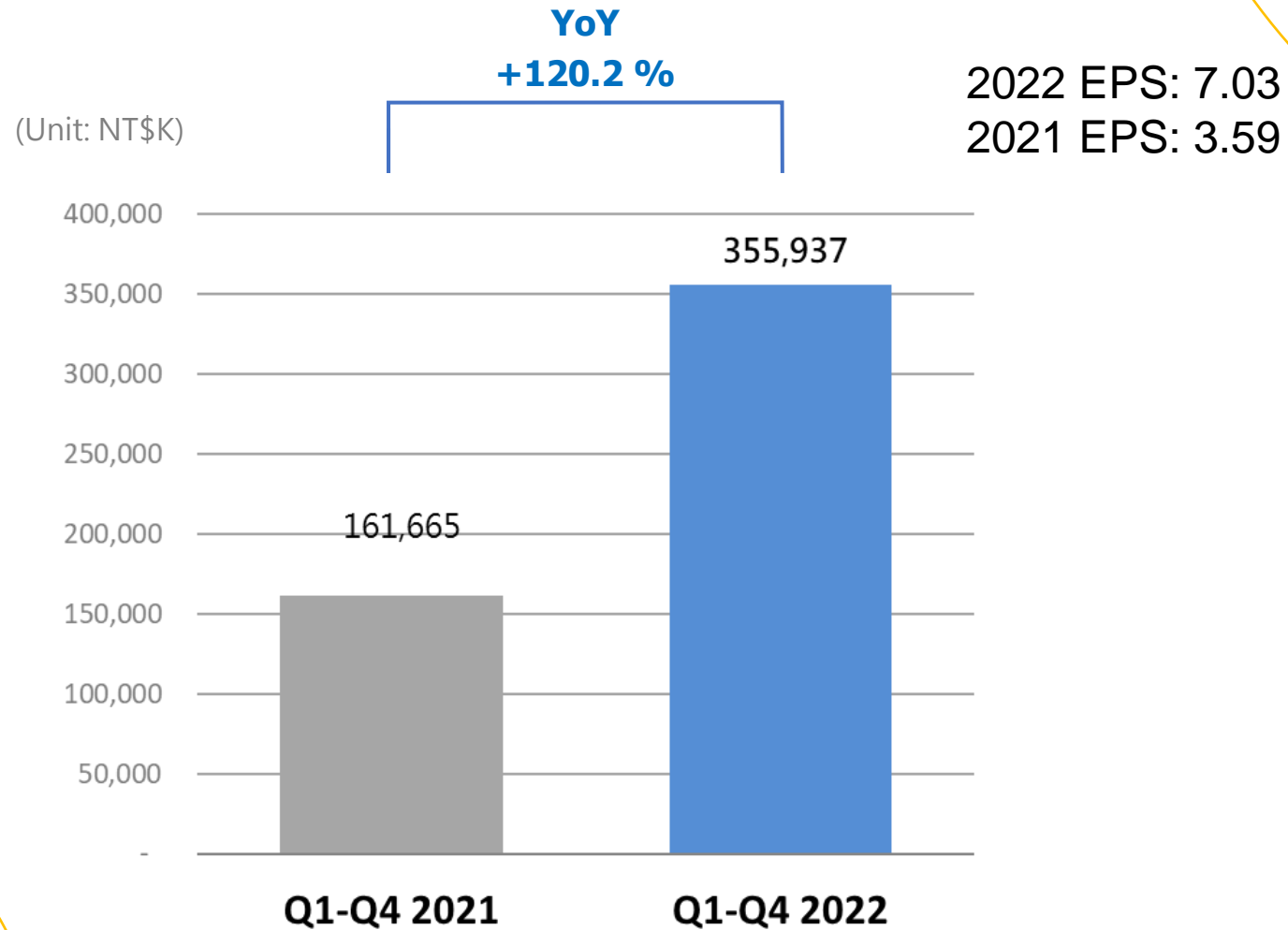
■ RISC-V  
■ V3



- N25
- N8
- N9
- AX45
- NX45
- ACE
- A45
- Customized IP
- NX27
- N13
- D25
- N45
- D45
- N10
- NX25
- D10
- AX25
- E8
- LLVM
- AE250
- A27
- OTHERS

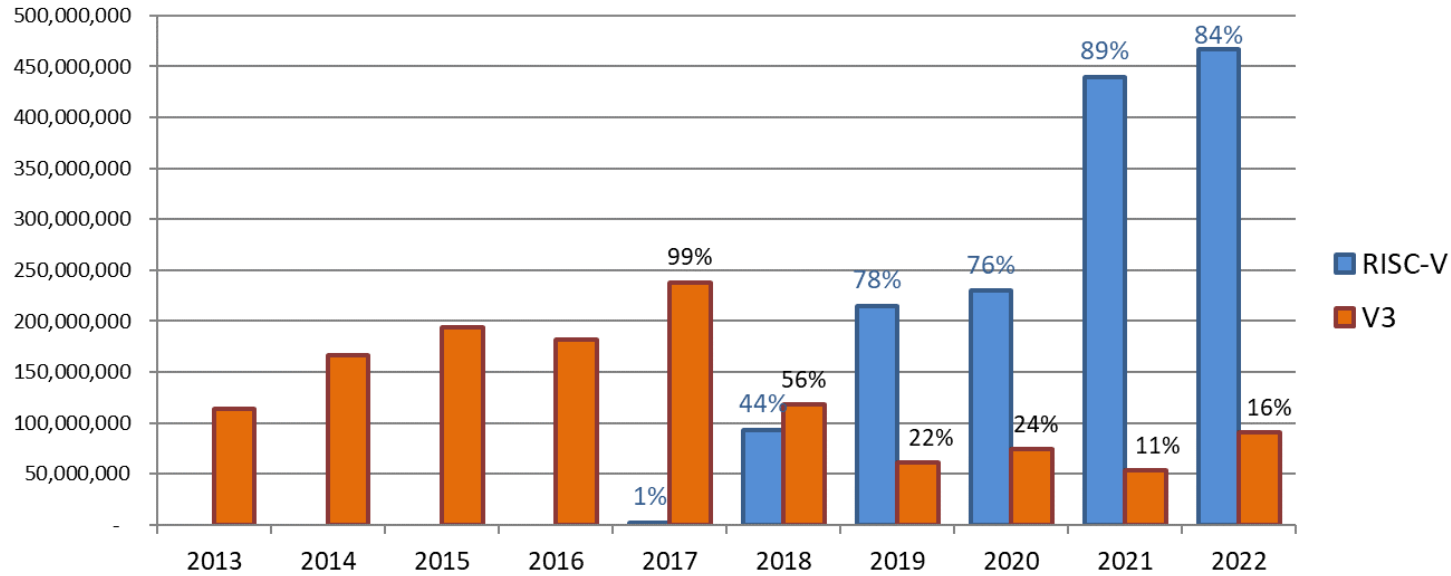


# 2022 Q1-Q4 Net Income Analysis

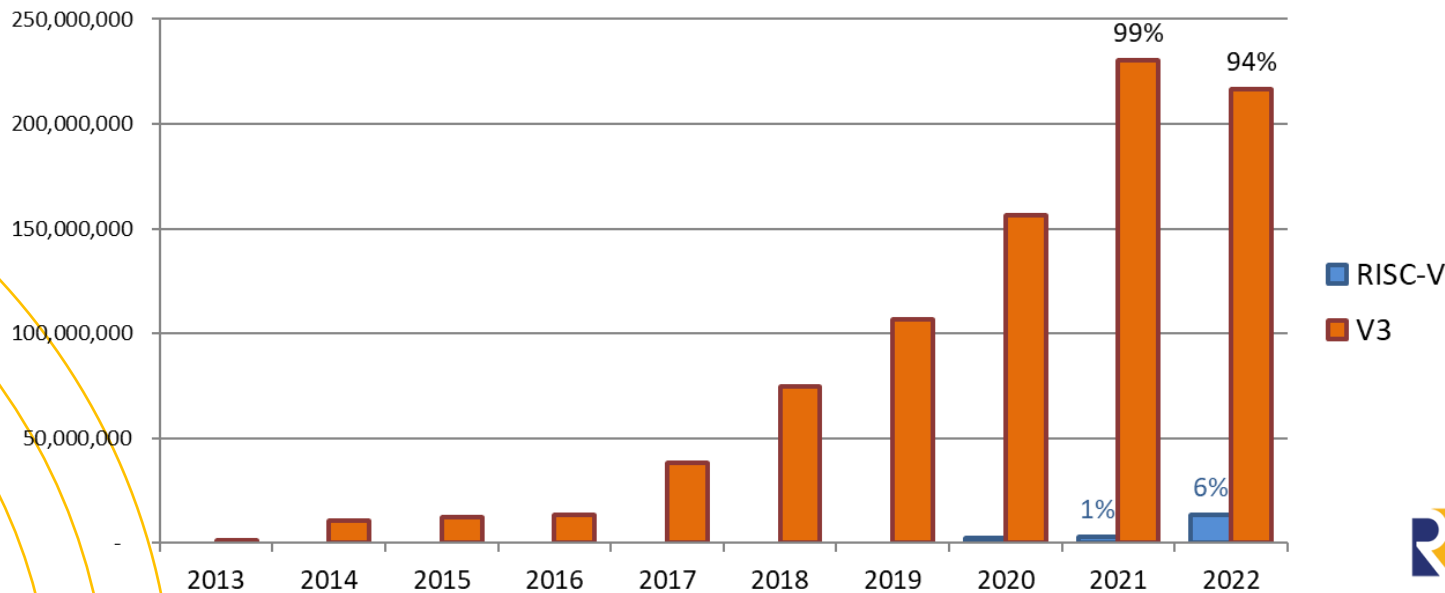


# Historical Revenue Analysis

(NT\$)



**License**



**Royalty**



# Product Applications

---

<http://www.andestech.com>





# V5 Adoptions: From MCU to Datacenters

## ❖ Edge to Cloud

- ADAS
- AIoT
- Blockchain
- FPGA
- MCU
- Multimedia
- Security
- Wireless (BT/WiFi)
- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

## ❖ 40nm to 5nm

## ❖ Many in AI



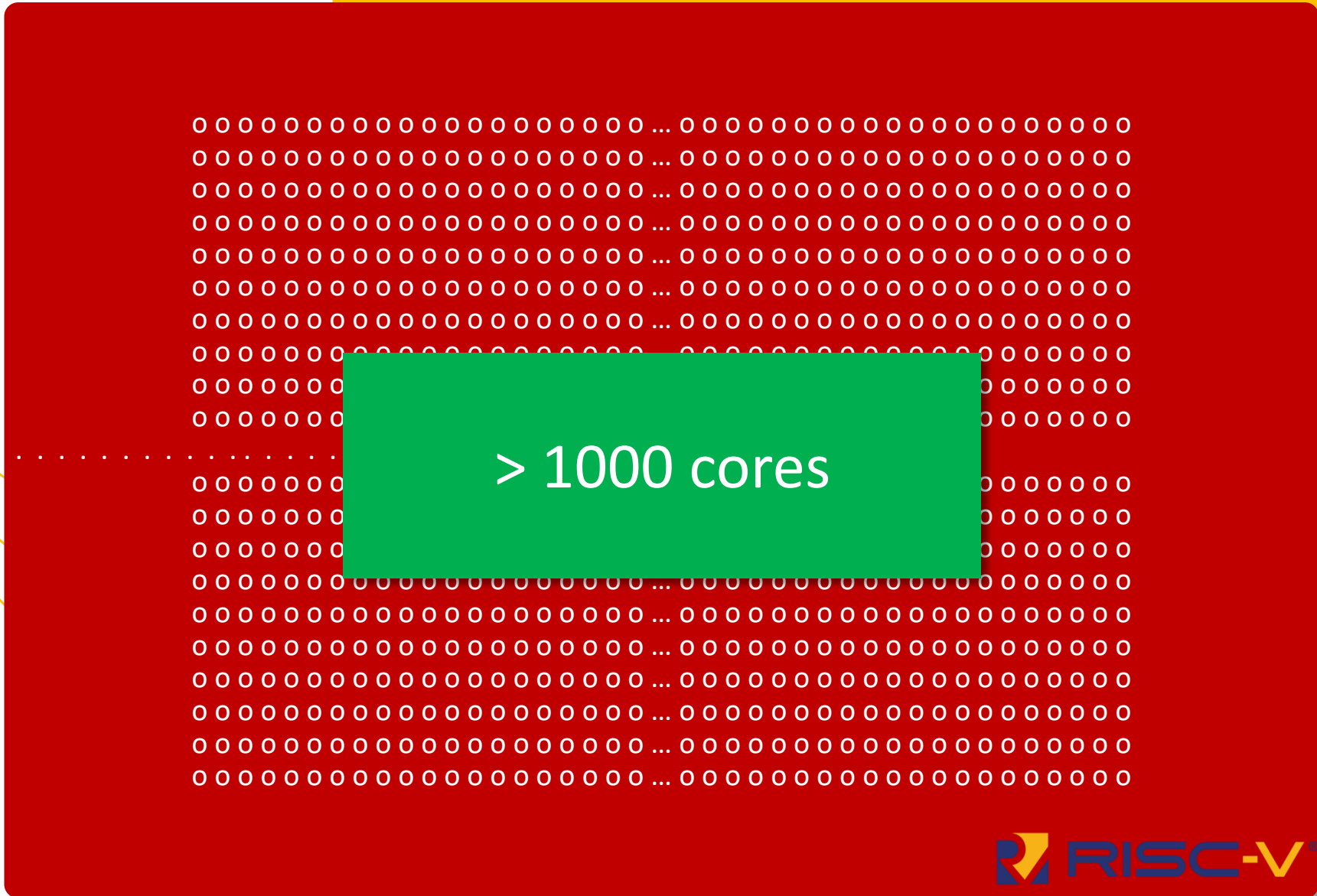
# Andes RISC-V Cores Adopted in SoC

○ single core

○○○○○  
○○○ 2-8 cores

○○○○○○○○○  
> 30 cores  
○○○○○○○○○

○○○○○○○○○○○○○○○○○○○  
> 100 cores  
○○○○○○○○○○○○○○○○○○○  
○○○○○○○○○○○○○○○○○○○  
○○○○○○○○○○○○○○○○○○○



# Andes RISC-V Product Roadmap

RV32/RV64

Vector Ext.

Superscalar

Out of Order

Cache-Coherent  
1-4 Cores

A25MP  
AX25MP

Linux with  
FPU/DSP

A25  
AX25

Fast/Compact  
with FPU/DSP  
**Automotive Grade**

N25F  
D25F  
NX25F  
**N25F-SE**  
**D25F-SE**

**NEW**

5-stage (1.1 GHz)

27-Series:

Vector Ext.  
MemBoost

NX27V  
A27/AX27  
A27L2/AX27L2  
and more.

5-stage (1.1 GHz)

45-Series:

Dual Issue  
Vector Ext.  
MemBoost

N45/NX45/D45  
A45/AX45  
A45MP/AX45MP  
**NX45V, AX45MPV**  
(1024-bit VPU,  
1-8 Cores)

**NEW**

8-stage (1.2 GHz)

60-Series:

> 2.5 GHz  
> 2x per-GHz  
performance of  
45-Series

**AX65** **NEW**  
and more.

13-stage

Leading positions:

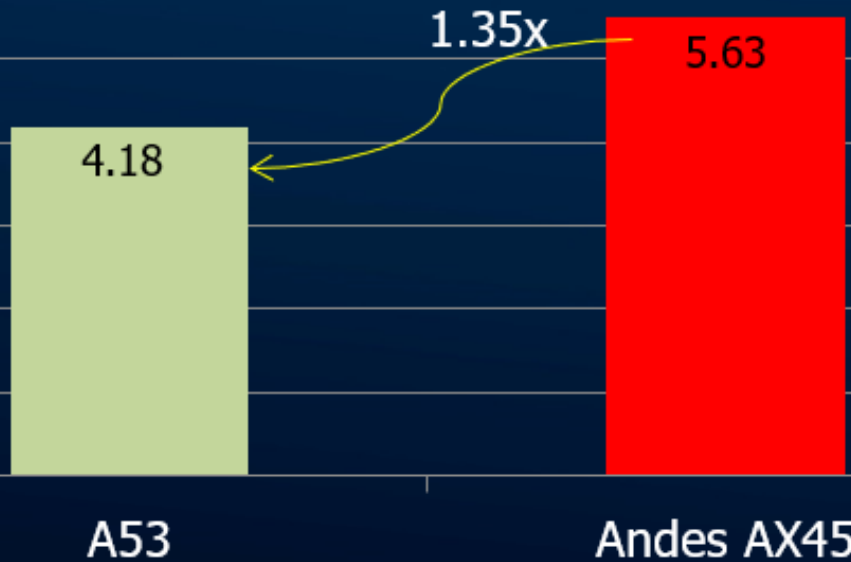
- ❖ The 1st company offering commercial RVP DSP CPU
- ❖ The 1st company offering the most updated spec of commercial RVV vector processor
- ❖ The 1st RISC-V core certified with ISO 26262 full compliance
- ❖ Tools for RISC-V custom extension: ACE

N22  
2-stage  
(700 MHz)

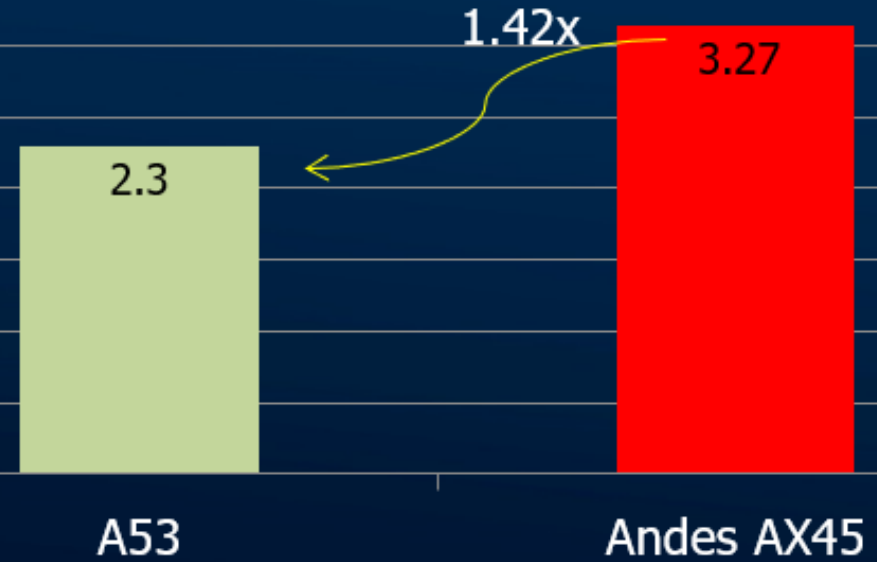
**D23** **NEW**  
3-stage  
(800 MHz)

# AX45 Can Do More (vs. 64bit A-series)

Coremark/MHz



Dhrystone/MHz



## ■ A53

- 8-stage In-Order Dual Issue
- **Widely adopted by industries in many applications**

## ■ AX45

- 8-stage In-Order Dual Issue
- **Performance is better!**
  - Coremark/MHz: 1.35x
  - Dhrystone/MHz: 1.42x

# Target Applications for 27 & 45-Series

■ AI/Deep Learning

■ AR/VR

■ 5G



■ Video Surveillance

■ ADAS



■ Networking



■ V2X (Vehicle to Everything)



■ IVI (In-Vehicle-Infotainment)



■ Storage



*Metaverse and more...*





# Toward 2023: New Products and Ecosystems

---

<http://www.andestech.com> 

# AndesCore™ Lineup with Industry's 1<sup>st</sup> RISC-V Cores



- **D25F**: with **SIMD/DSP capability** (P-extension, 32/64 bits)
- **NX27V**: with **Vector Processing Unit** (V-extension, up to 512 bits)
- **N25F-SE**: with **ISO 26262 Full Compliance**, not just *Ready*

<b>45 Series</b> 8-stage superscalar	N45, NX45	D45	A45(MP) AX45(MP)		A53/55, R52/82, M7
<b>27 Series</b> 5-stage MemBoost		<b>NX27V</b>	A27(L2) AX27(L2)		A5/7/35
<b>25 Series</b> 5-stage fast & compact	N25F, NX25F	<b>D25F</b>	A25(MP) AX25(MP)	<b>N25F-SE</b>	A5/7/35, R4/5, M4/33
<b>Entry Series</b>	N22				M0/0+/3/33/4
<i>Categories</i>	<i>Embedded Control</i>	<i>DSP/Vector</i>	<i>Linux AP</i>	<i>FUSA</i>	<i>References</i>

# AndesCore™ Roadmap Processors



<b>AX60 Series</b> 13-stage OOO MP		<b>AX65</b>	<b>AX67</b>	<b>60-SE</b>	A72~A76; N1/V1
<i>Categories</i>	<i>Power-efficient</i>	<i>Mid-range</i>	<i>Extended</i>	<b>FUSA</b>	
<b>45 Series</b> 8-stage Superscalar	N45, NX45	<b>NX45V*</b> D45	<b>AX45MPV</b> A45(MP), AX45(MP)	<b>45-SE</b>	A53/55, R52/82, M7
<b>27 Series</b> 5-stage MemBoost		<b>NX27V</b>	A27(L2), AX27(L2)		A5/7/35
<b>25 Series</b> 5-stage Fast&Compact	N25F, NX25F	<b>D25F</b>	A25(MP), AX25(MP)	<b>D25F-SE<sup>B</sup></b> N25F-SE <sup>B</sup>	A5/7/35, R4/5, M4/33
<b>Entry Series</b>	N22	<b>D23</b>		<b>23-SE</b>	M0/0+/3/33/4
<i>Categories</i>	<i>Embedded Control</i>	<i>DSP/Vector</i>	<i>Linux AP</i>	<b>FUSA</b>	<i>References</i>

Note \*: AX45MPV configured as one core

- **New Processors: AX65, AX45MPV, D23, D25F-SE**
- **Safety Enhanced (SE) Series: at least one per year**



# AndesCore™ AX65

Multicore Out-of-Order Superscalar Processor

# The Andes AX60 Processor Series



## ■ A new generation of AndesCore™

- Advanced Performance 13-stage Out-of-Order Superscalar Multicore
- Latest RISC-V Architecture
- Supported by Andes Long-term Roadmap
  - AX65 as the first member of the AX60 series
  - More products based on the AX60 micro-architecture planned, including for automotive functional safety

## ■ AndesCore™ AX65

- Offering performance surpassing CA72
- > 2.5 GHz, > 2x per-GHz performance of AX45MP
- Engaging with early customers



# Preliminary Performance Results



AndesCore	AX27L2	AX45MP (over AX27L2)	AX65 (over AX45MP)
Micro-architecture	5 stage scalar in-order	8 stage dual-issue in-order	13 stage quad-issue OOO
Freq. (7nm)	~2 GHz	>2 GHz	>2.5 GHz
Coremark/MHz	3.55	5.64 (+59%)	9.17 (+63%)
Specint2k6/GHz	2.82	3.46 (+23%)	> 7 (>2x, target)
EEMBC FPMark/MHz	27.0	35.2 (+30%)	66.6 (+89%)
Linpack MFLOPS/MHz	0.130	0.220 (+69%)	0.613 (2.8x)
Mem Bandwidth <sup>1</sup> /MHz	1.0x	1.47x	1.90x

1. Based on standard library memcpy



# AndesCore™ AX45MPV

Multicore 1024-bit Vector Processor

# AX45MPV: Linux Multicore Vector Processor



## ■ A new member of popular AndesCore™ 45-series processors

- Inherits all features of AX45MP and leverages 3+ years of field experience from NX27V vector engine
- 64-bit 8-stage dual-issue processor
- Up to 8 cores SMP supporting up to 8MB L2 cache
- Dual-issue 1024-bit Vector Processing Unit (VPU) delivers up to 6 results per cycle

## ■ AndesCore™ AX45MPV

- Targets AI inference/training, ADAS, AR/VR, computer vision, multimedia
- Engaging with early customers



# AndesCore™ D25F-SE / N25F-SE

Automotive Functional Safety(FUSA)




# Andes is *Driving* Innovations in Automotive



with Industry's 1<sup>st</sup> RISC-V ISO 26262 Fully Compliant Core, N25F-SE

## In-Cabin Radar



Radio

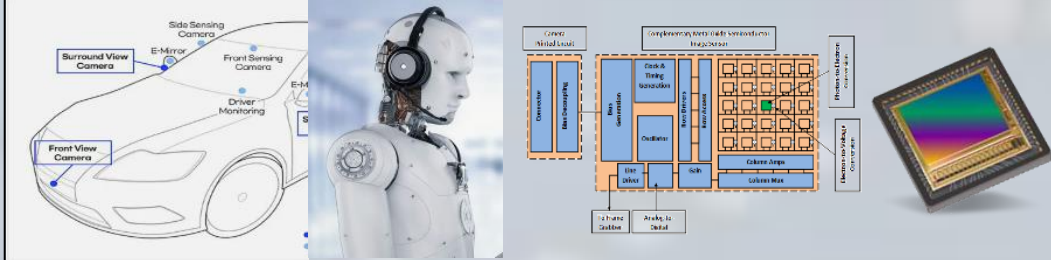
**Radar Subsystem**  
N25F-SE

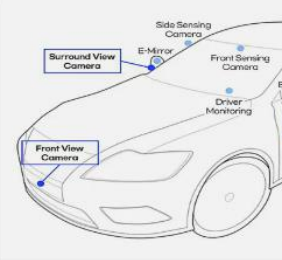
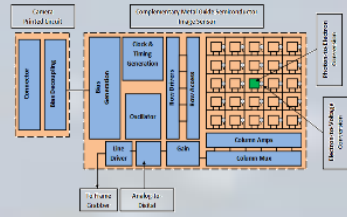
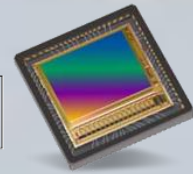
**Host Controller**  
N25F-SE

Memory

Peripheral

## CMOS Sensor



## Auto TDDI

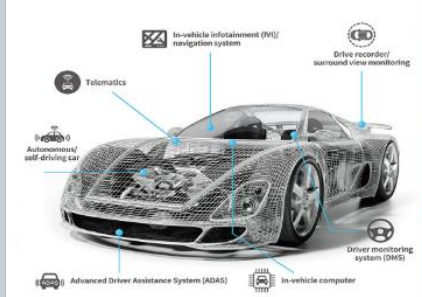
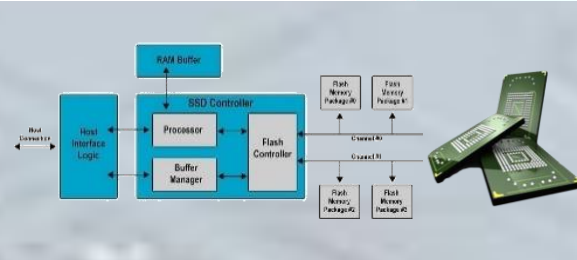



## Auto MCU



器件	数量	物料号
主控	1	AND9000
存储器	2	AND9001
收发器	1	AND9002
接口芯片	1	AND9003
电源管理	1	AND9004
时钟	1	AND9005
其他	1	AND9006

## Auto Storage



# N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor



- ISO 26262 Certification for Development Process: ASIL-D
  - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- ISO-9001 QMS achieved and maintained since 2010
- ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE
  - ISO 26262-2,4,5,8,9
  - Covers all the sections applicable to CPU core

# D25F-SE: FuSa processor with DSP/SIMD capability



## ■ CPU Core

- AndeStar™ V5 Instruction Set Architecture (ISA)
  - RISC-V 32-bit, RV32GC + Andes Extensions
  - RISC-V P(draft) and B extensions.
  - Machine+User (M+U) privilege levels
- Dynamic branch prediction with BTB, BHT, RAS
- CoDense™ code size reduction, StackSafe™ stack protection

## ■ Memory Subsystem

- Support I/D cache up to 32KB each
- Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses

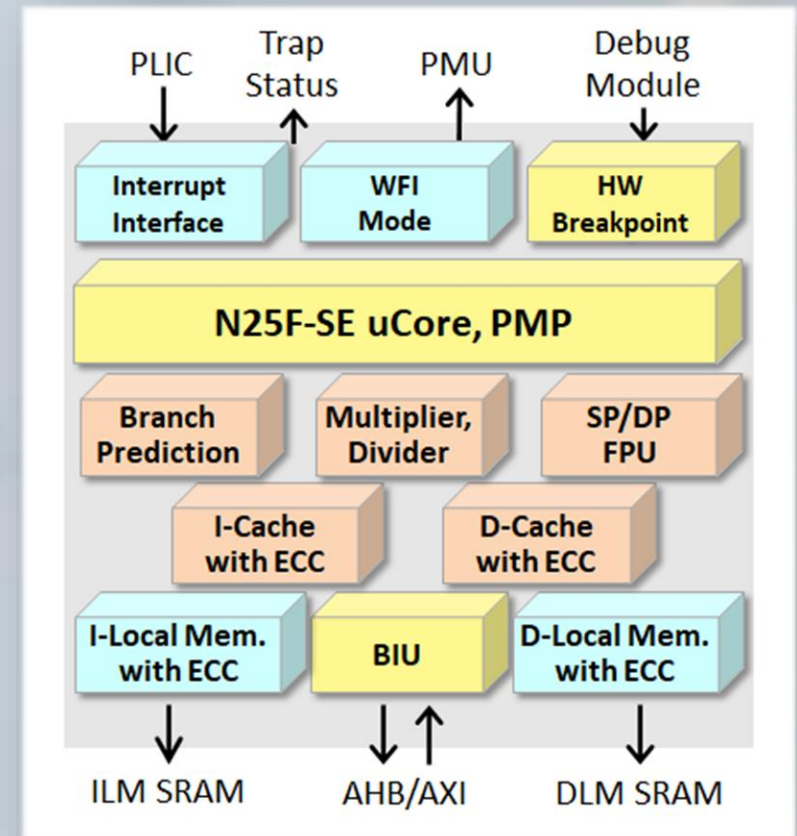
## ■ Bus Interfaces

- AXI or AHB bus master port
- N:1 CPU clock vs. bus clock ratio

## ■ Others

- Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface

## ■ Safety Package including Safety Manual & FMEDA report



# D25F-SE: FuSa processor with DSP/SIMD capability



## ■ CPU Core

- AndeStar™ V5 Instruction Set Architecture (ISA)
  - RISC-V 32-bit, RV32GC + Andes Extensions
  - RISC-V P(draft) and B extensions.
  - Machine+User (M+U) privilege levels
- Dynamic branch prediction with BTB, BHT, RAS
- CoDense™ code size reduction, StackSafe™ stack protection

## ■ Memory Subsystem

- Support I/D cache up to 32KB each
- Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses

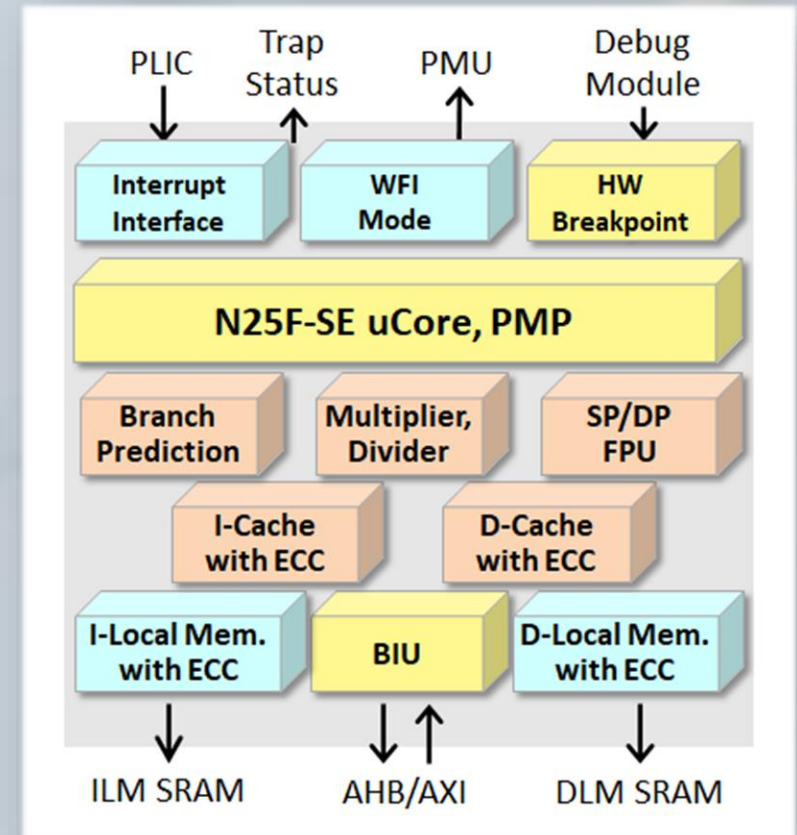
## ■ Bus Interfaces

- AXI or AHB bus master port
- N:1 CPU clock vs. bus clock ratio

## ■ Others

- Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface

## ■ Safety Package including Safety Manual & FMEDA report

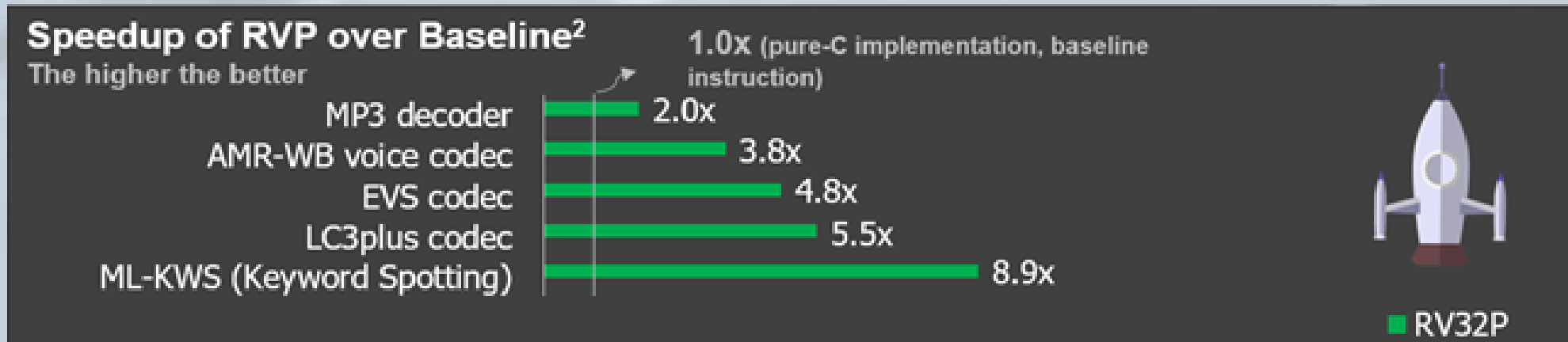




# D25F-SE with DSP and Bit-manipulation



- RVP: Powerful DSP/SIMD instructions for audio/voice codec and endpoint AI/ML
- SIMD instructions such as a quad 8 x 8 accumulated into 32-bit data
- DSP library support of over 200 functions



- RVB: Efficient bit-manipulation operations for codes such as cryptographic & checksums
  - Latest RVB ISA-extension Ver 1.0.0, including:
    - address generation, basic bit-manipulation, carry-less multiplication and single-bit instructions
    - Accelerate Crypto calculations: **27%** improvement on SHA256, **19%** for AES, **16%** for MD5

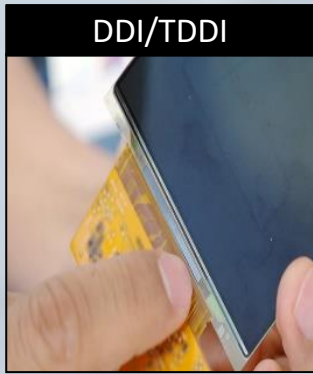


# AndesCore™ D23

Compact, Secure, Low-Power Controller



# D23 Targets Diverse Embedded & IoT Applications



DDI/TDDI



Wearable



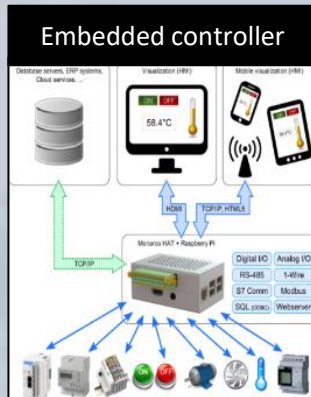
Smart Home



Motor Control



Connectivity



Embedded controller

Applications	D23 Capability fit
DDI, TDDI	Small gate count
Wireless controller core (WiFi, BT or others )	Security, small gate count
Smart Home Appliance	Security, performance, small gate count
Wearable	DSP (Edge AI), Security
E-Toys	DSP (Speech and Sound Processing)
RF Sensor control	DSP (Edge AI, Front-End Signal/Protocol Stack Processing)
MEMS/Sensor Fusion	DSP (Edge AI, Front-End Signal processing)
Battery or charging control	Performance
Advanced Motor Control	DSP



# RISC-V: 2022 Toward 2023 & Beyond

**- New Application Market**

<http://www.andestech.com> 

# RISC-V Technology 2022 to 2023

- Drive Progression and Closure on Specs and Technical Deliverables

Item	2022	2023	% change
TGs	33	40	25%
SIGs	23	28	25%
ISA Spec Ratifications	2	20	1000%
non-ISA Spec Ratifications	4	11	275%
Profiles	-	6	N/A
Platforms	-	1	N/A



# Android Support for RISC-V



**Google Announced**

**Android RISC-V Support**

READ MORE



Date: 2023-01-07

# 2023 & Beyond



- **Google Android will be ported to RISC-V**
- **The ecosystem will get more mature in 3 years**
- **Andes is committed in making its high end RISC-V CPU running Android in quality**
  - For example, 45 series AX45MP, 60 series AX65, and more higher end RISC-V cores
- **ChatGPT is hot yet “mainframe” style deployed, OpenAI put it in one neuro-network type of AI system**
  - Future trend is to make AI “edge” style or “personal” style, which will lead to further Edge AI revolution, SoC is still solution for future deployment
- **Andes will deliver such solution in terms of core hardware, developing platform, and software ported**



# Thank You

<http://www.andestech.com>

+886-3-5726533

