晶心科技股份有限公司

ANDES TECHNOLOGY

投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

01 公司簡介

02 營運成果

03 產品應用

04 新產品及生態系統

05 總結

公司簡介

http://www.andestech.com

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數達400人; 80%為工程師。
- 獲得TSMC 2015年新的 IP OIP Award 。
- 晉升為RISC-V國際聯盟(前身為RISC-V基金會) 首席會員。 (2020)
- 獲得AI Global Media頒發「2020年最傑出嵌入式處理器IP供應商」。
- 向量處理器核心NX27V獲頒「新竹科學園區優良廠商創新產品獎」 (2020)
- EE Awards亞洲金選獎 -「Taiwan 產品獎」,「Asia 企業獎」(2021)

晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

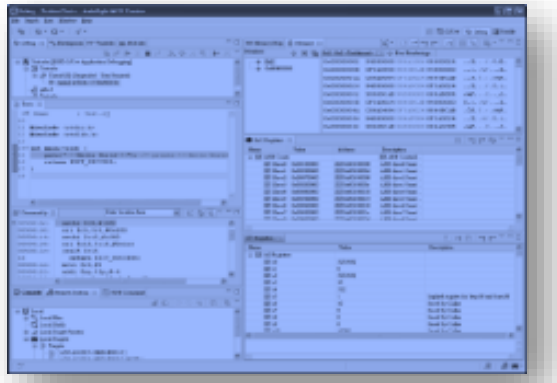
晶心利基

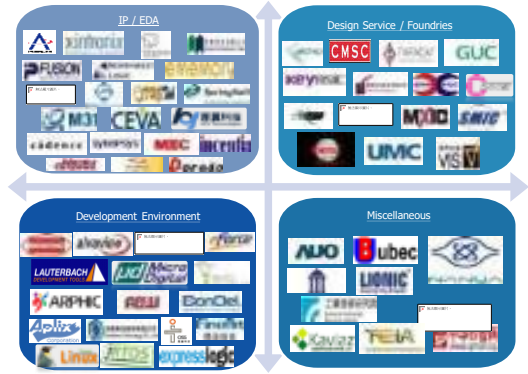
- 智能及環保之電子設備
- 雲端應用,人工智慧及物聯網

ANDES TECHNOLOGY

重要里程碑

- **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed
- AndeSight™ IDE:
  - **24,000+** installations
- Eco-system:
  - **500+** partners
- **12B+** Accumulative SoC Shipped

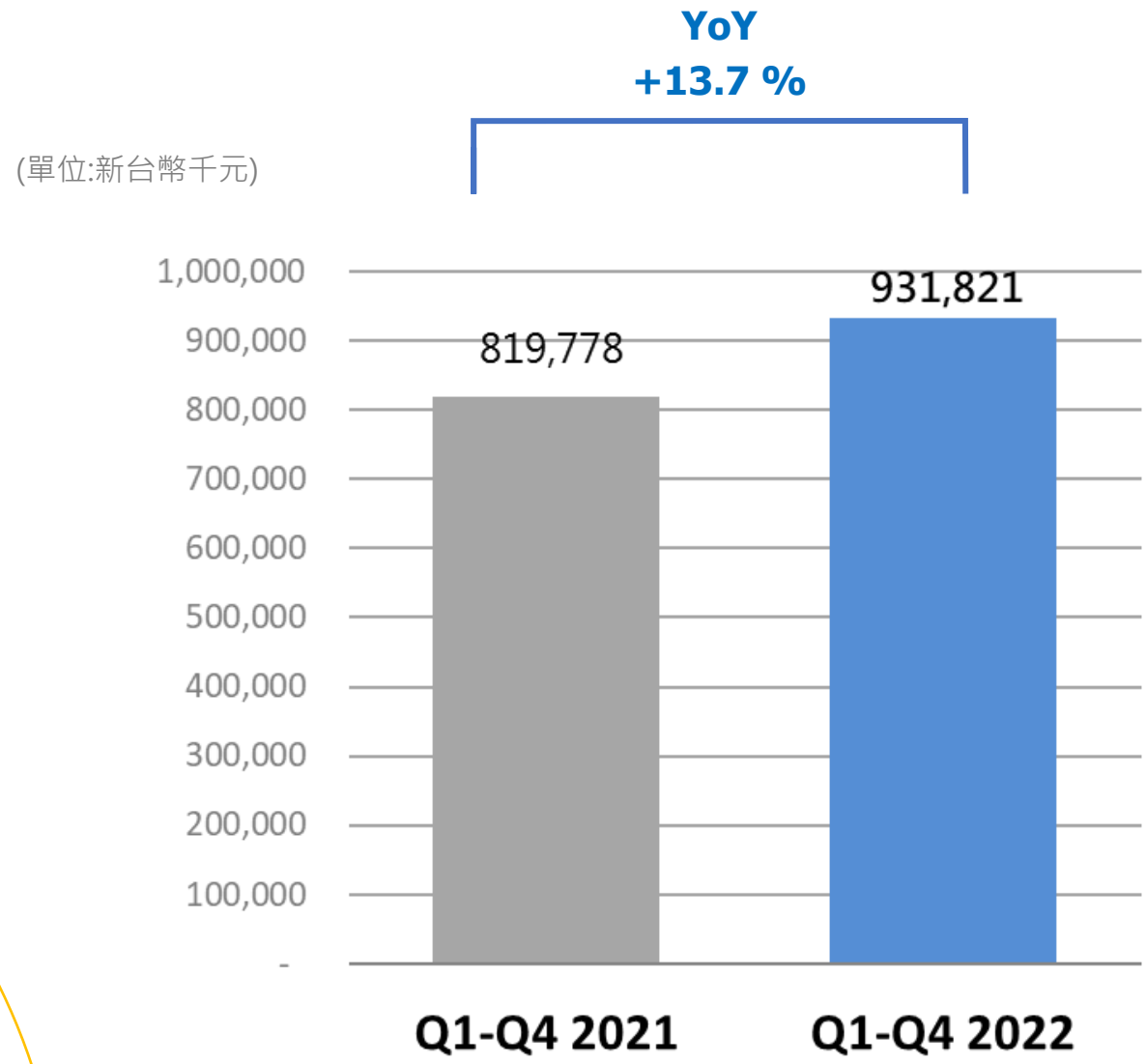




營運成果

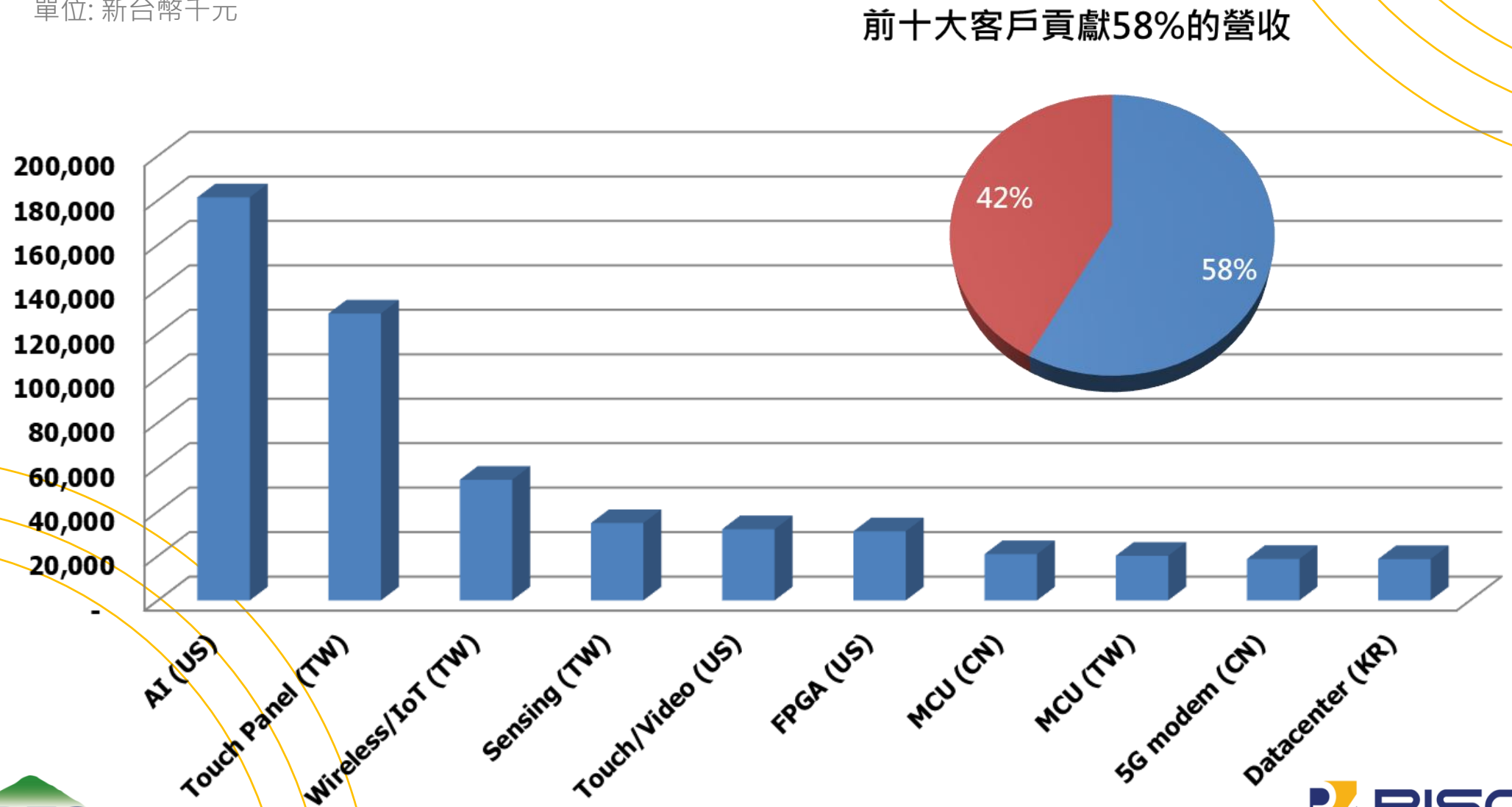
http://www.andestech.com

2022年度 營業收入

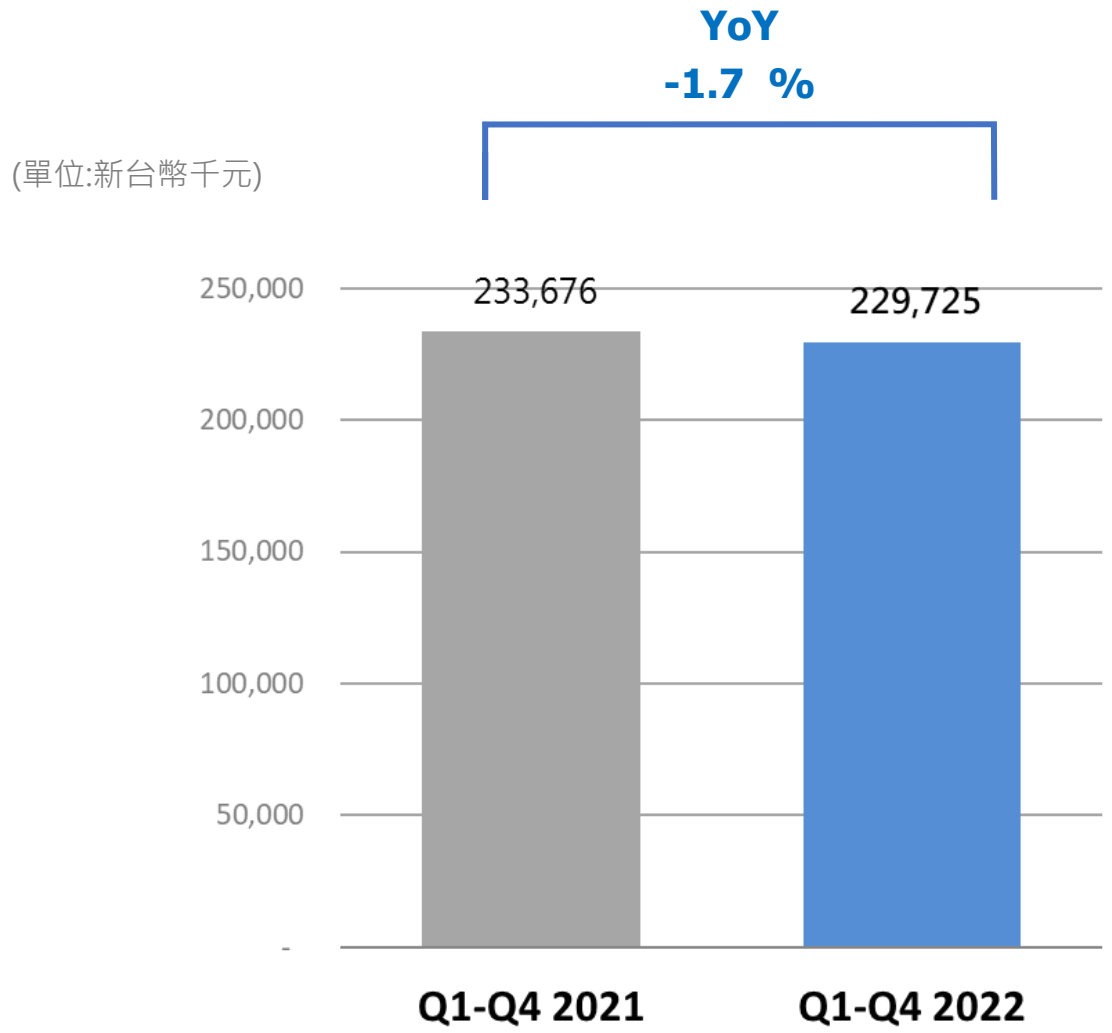

YoY
+13.7 %
(單位:新台幣千元)
1,000,000
900,000
800,000
700,000
600,000
500,000
400,000
300,000
200,000
100,000
-
819,778
931,821
Q1-Q4 2021
Q1-Q4 2022

2022年度前十大客戶之應用分析

單位: 新台幣千元

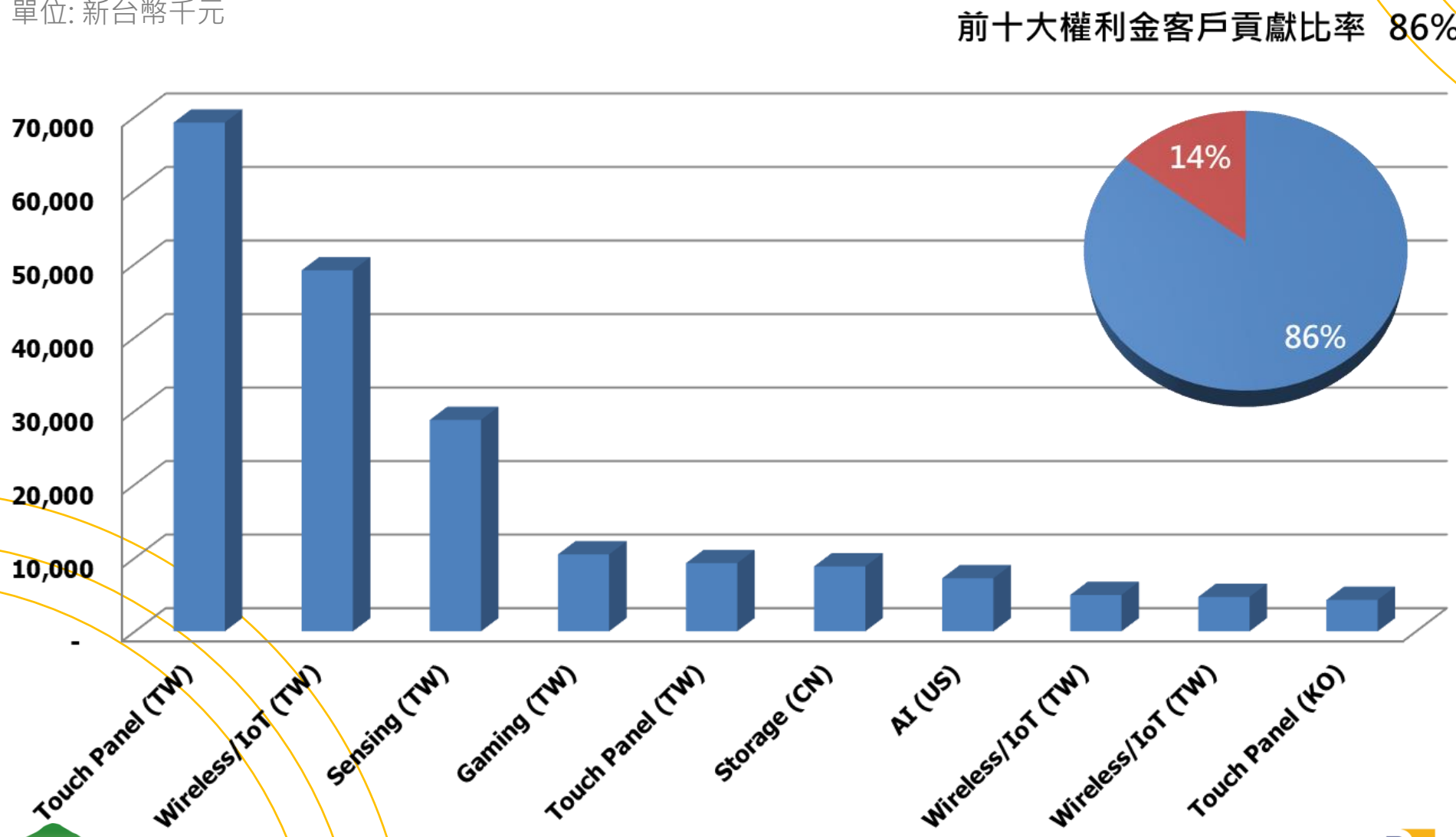


2022年度 權利金收入

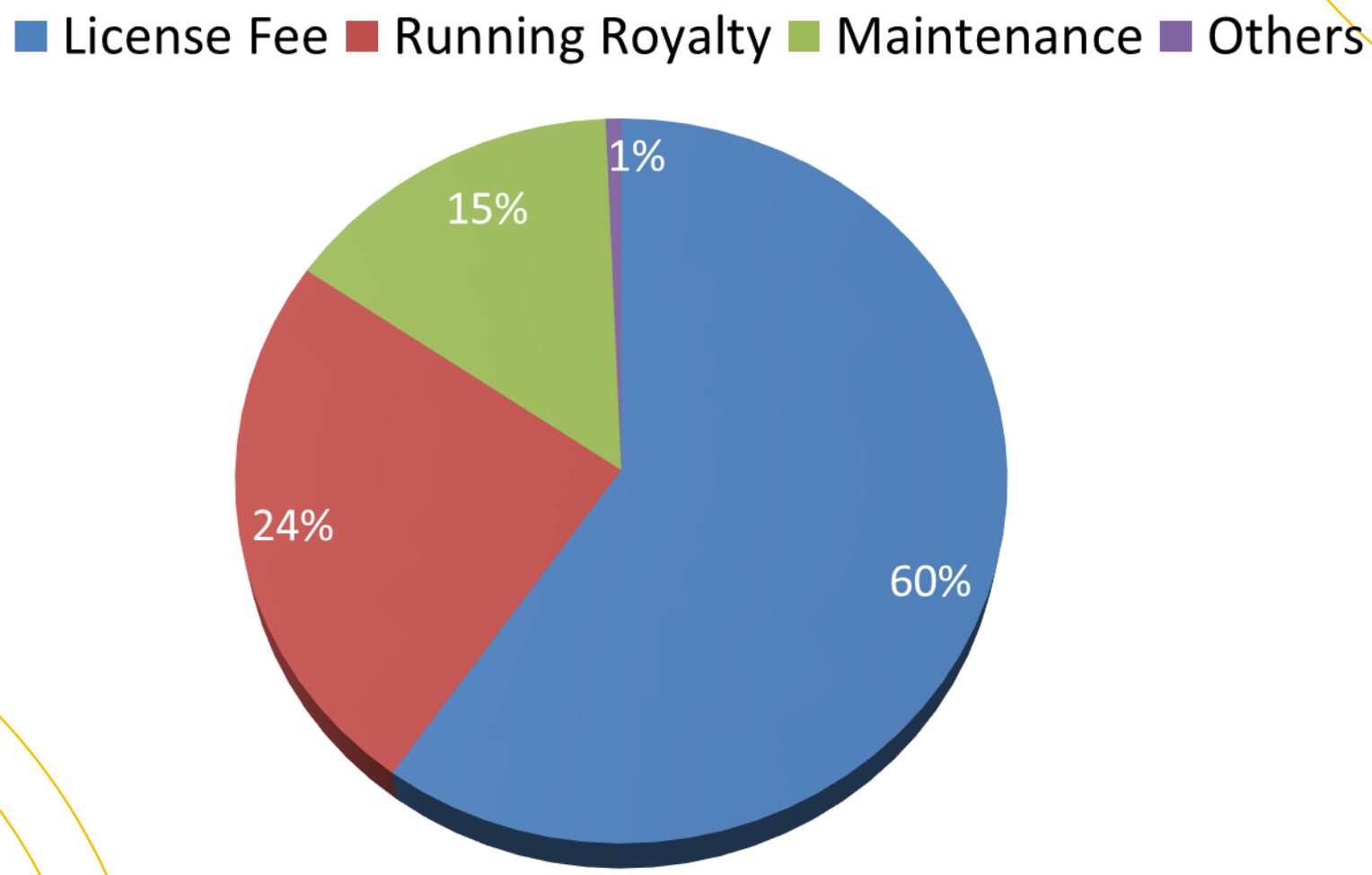


2022年度 權利金前十大客戶應用分析

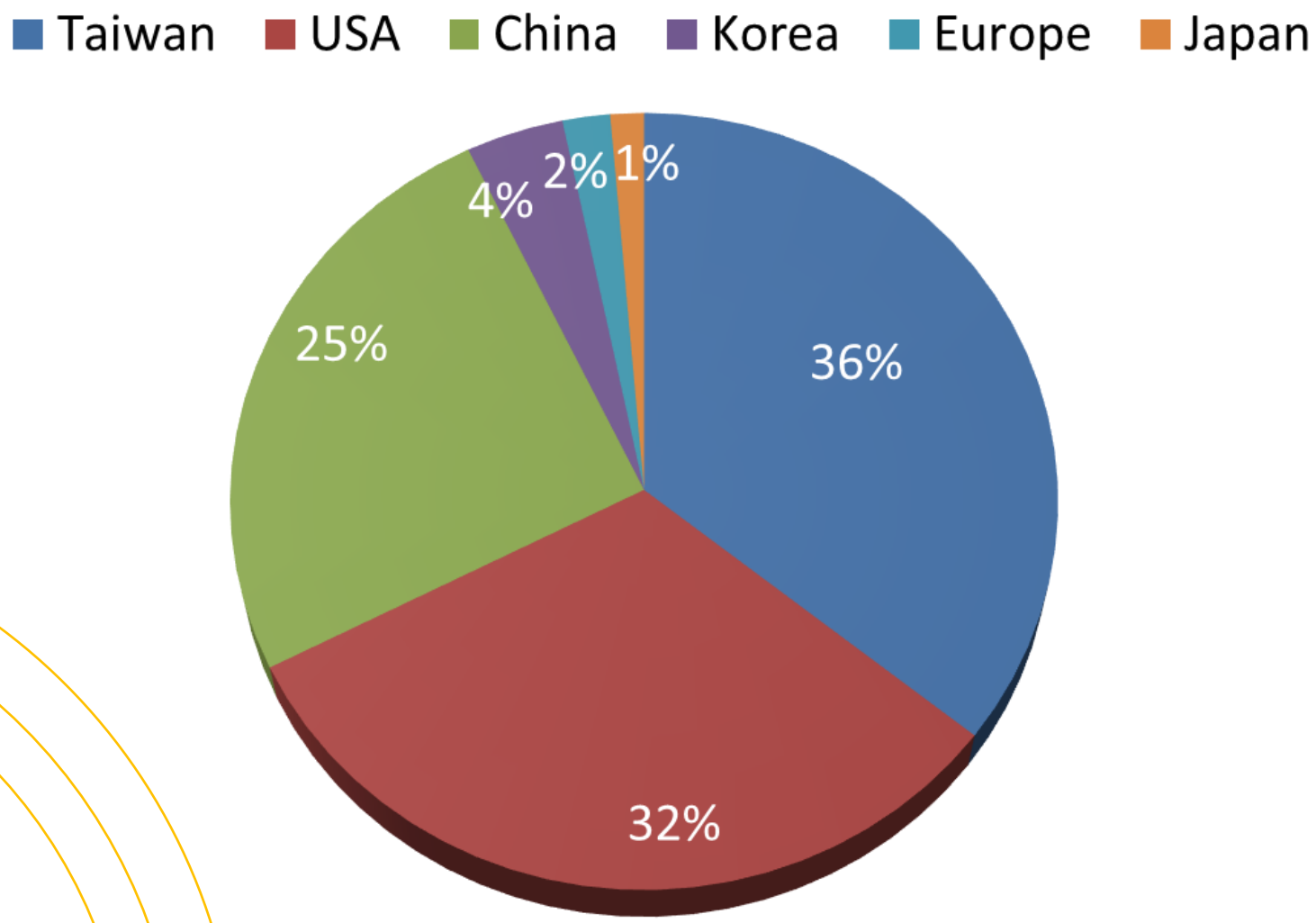
單位: 新台幣千元



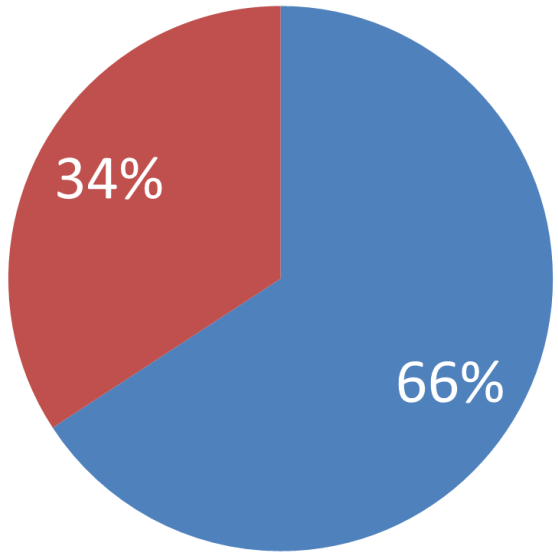
2022年度 銷售分析-收入模式

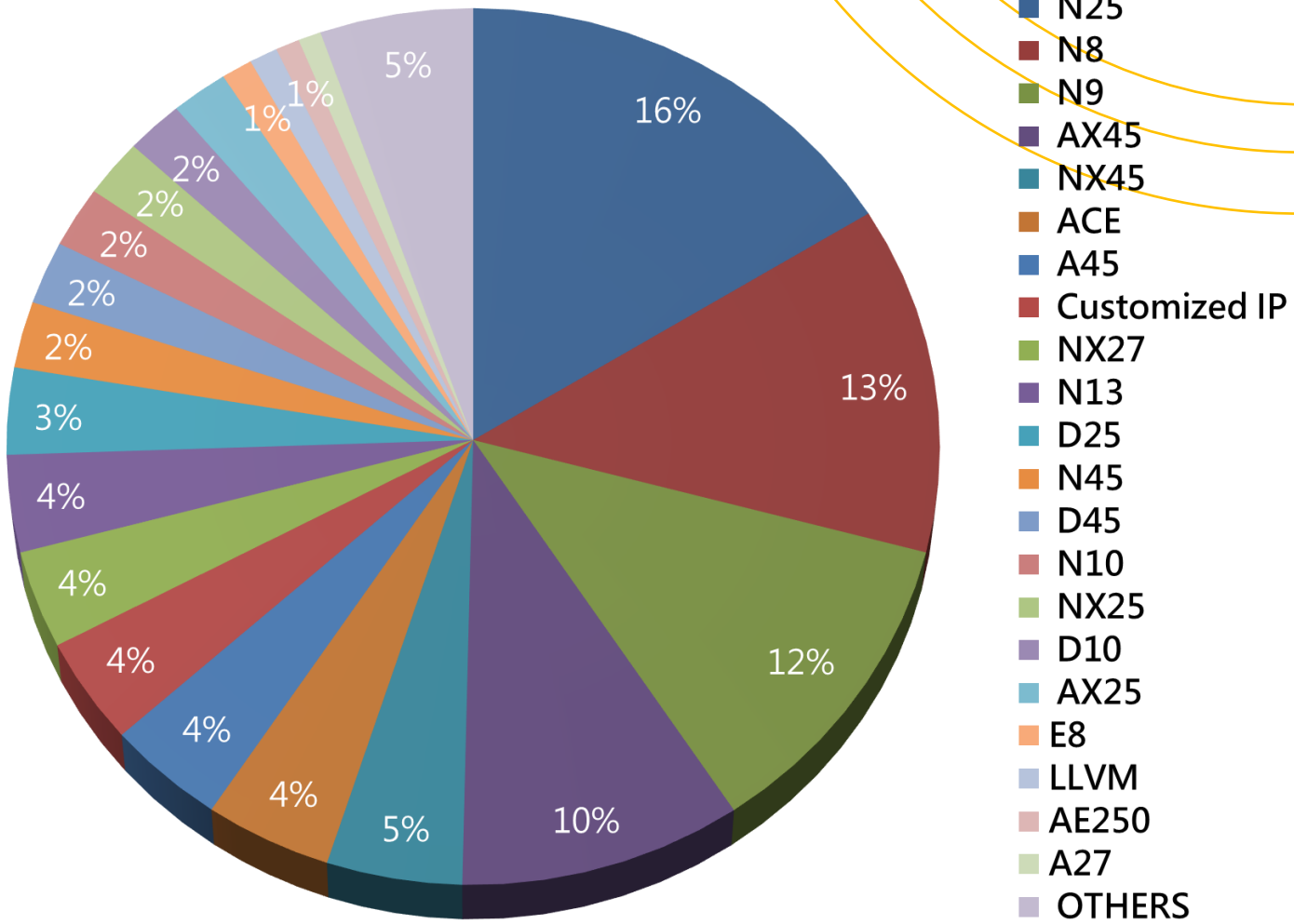


2022年度 銷售分析-地區別

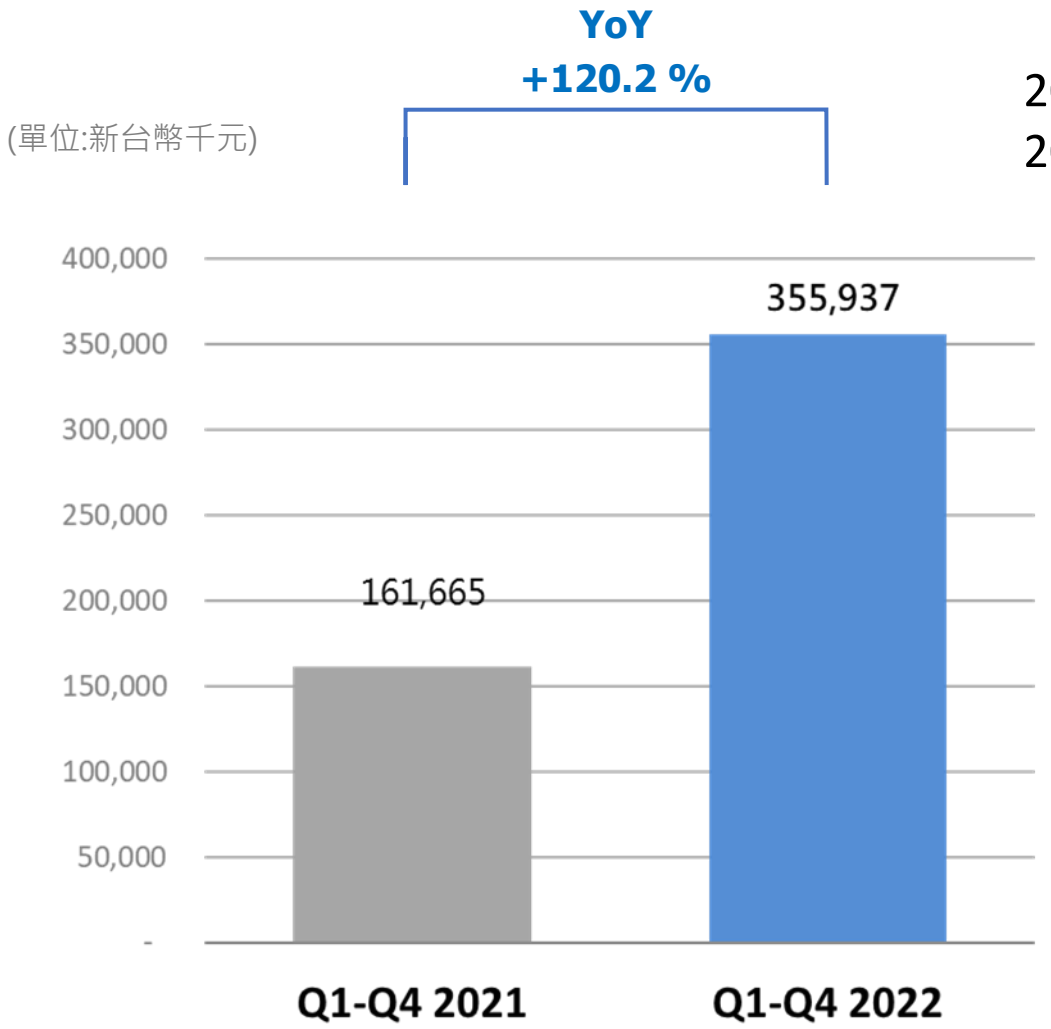


2022年度 銷售分析-產品別





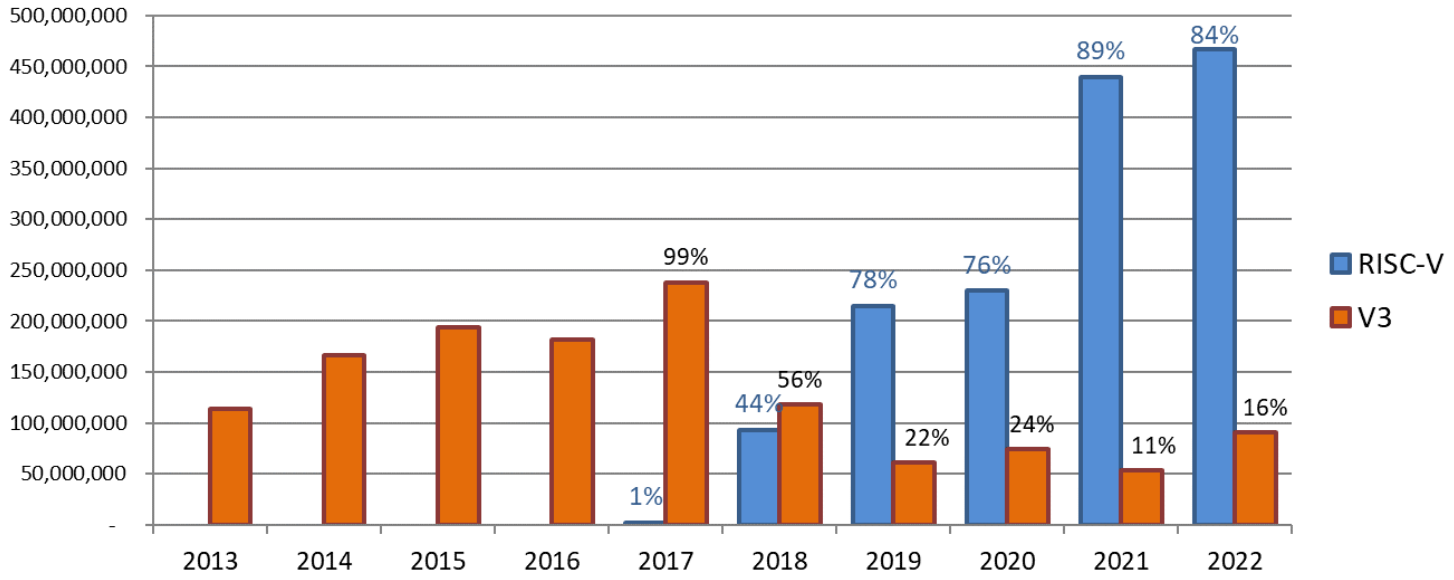
2022年度 稅後淨利



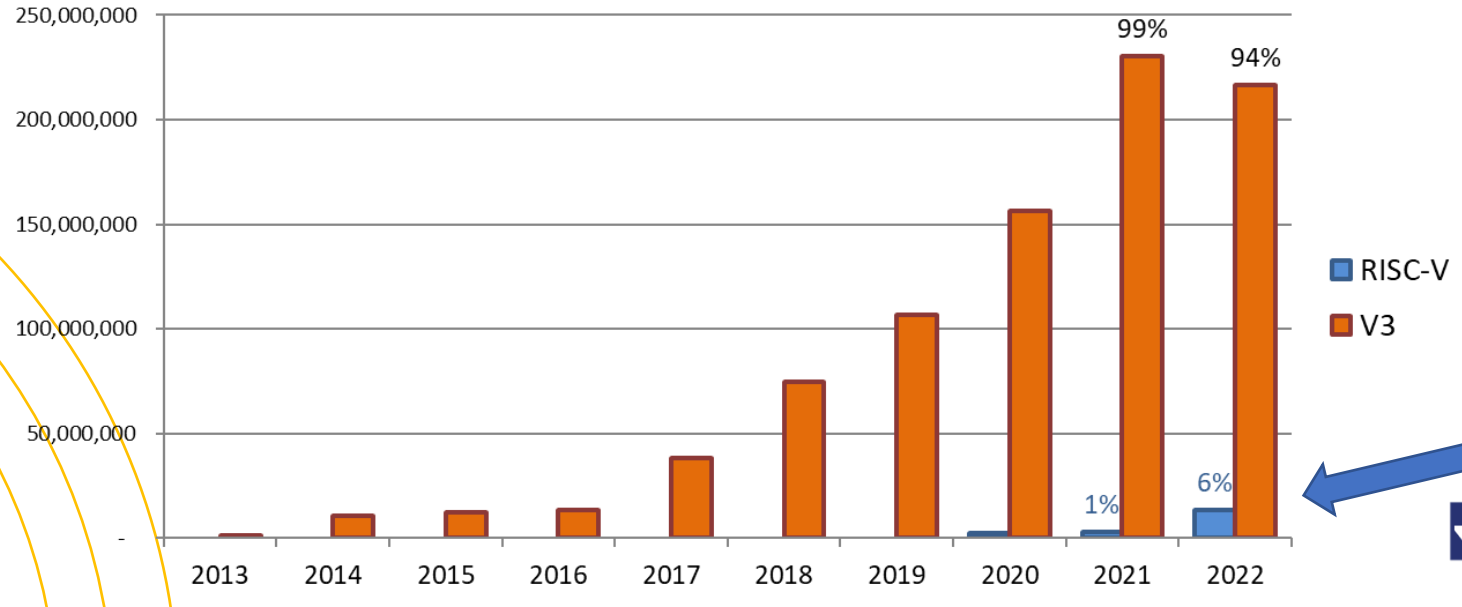
2022 Q1-Q4 EPS: 7.03
2021 Q1-Q4 EPS: 3.59

歷史營收分析

(NT$)



License



Royalty

RISC-V 2022: 6%

產品應用

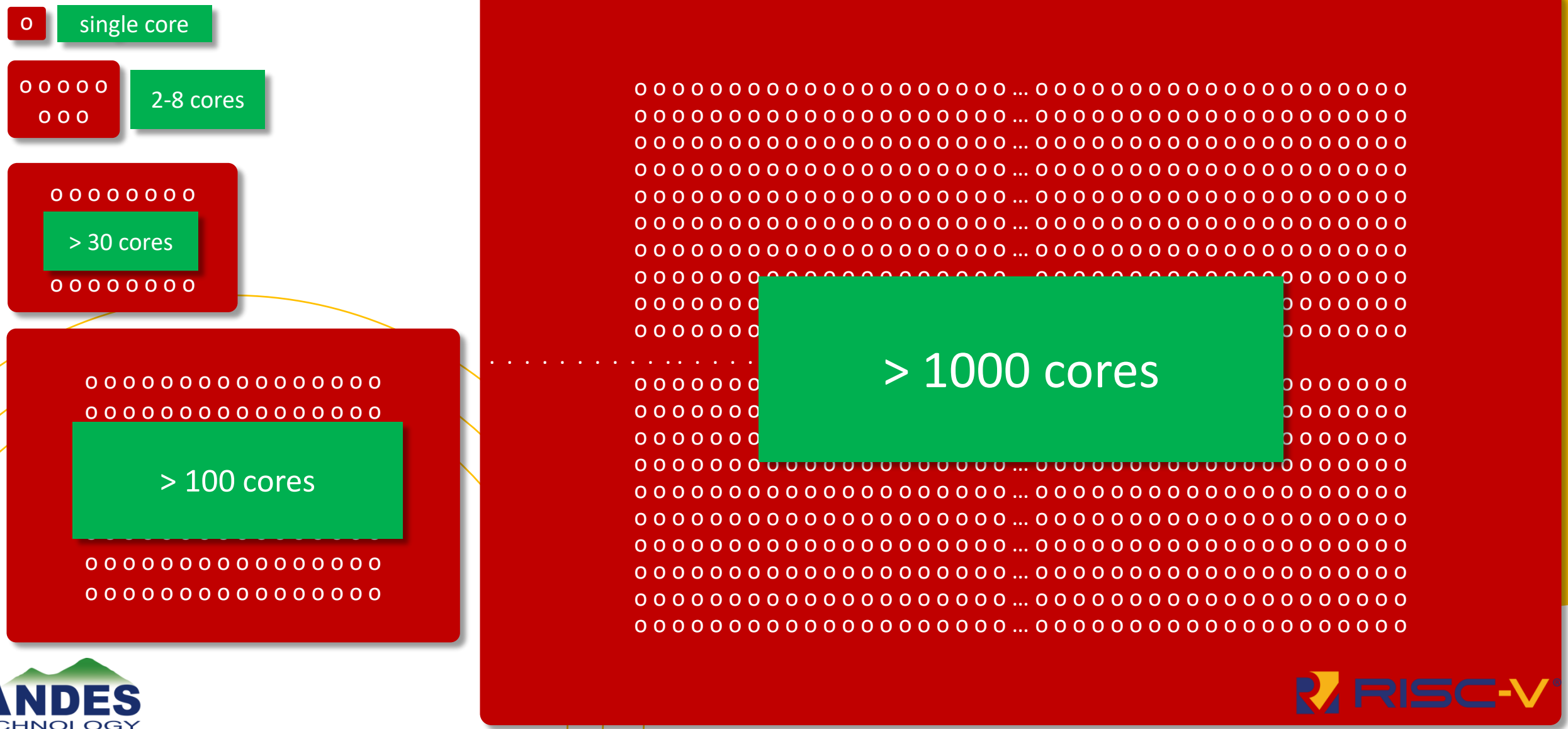
http://www.andestech.com

晶心RISC-V已應用在邊緣到雲端運算的SoC

- **Edge to Cloud**
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)
- **40nm to 3nm**
- **Many in AI**

- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

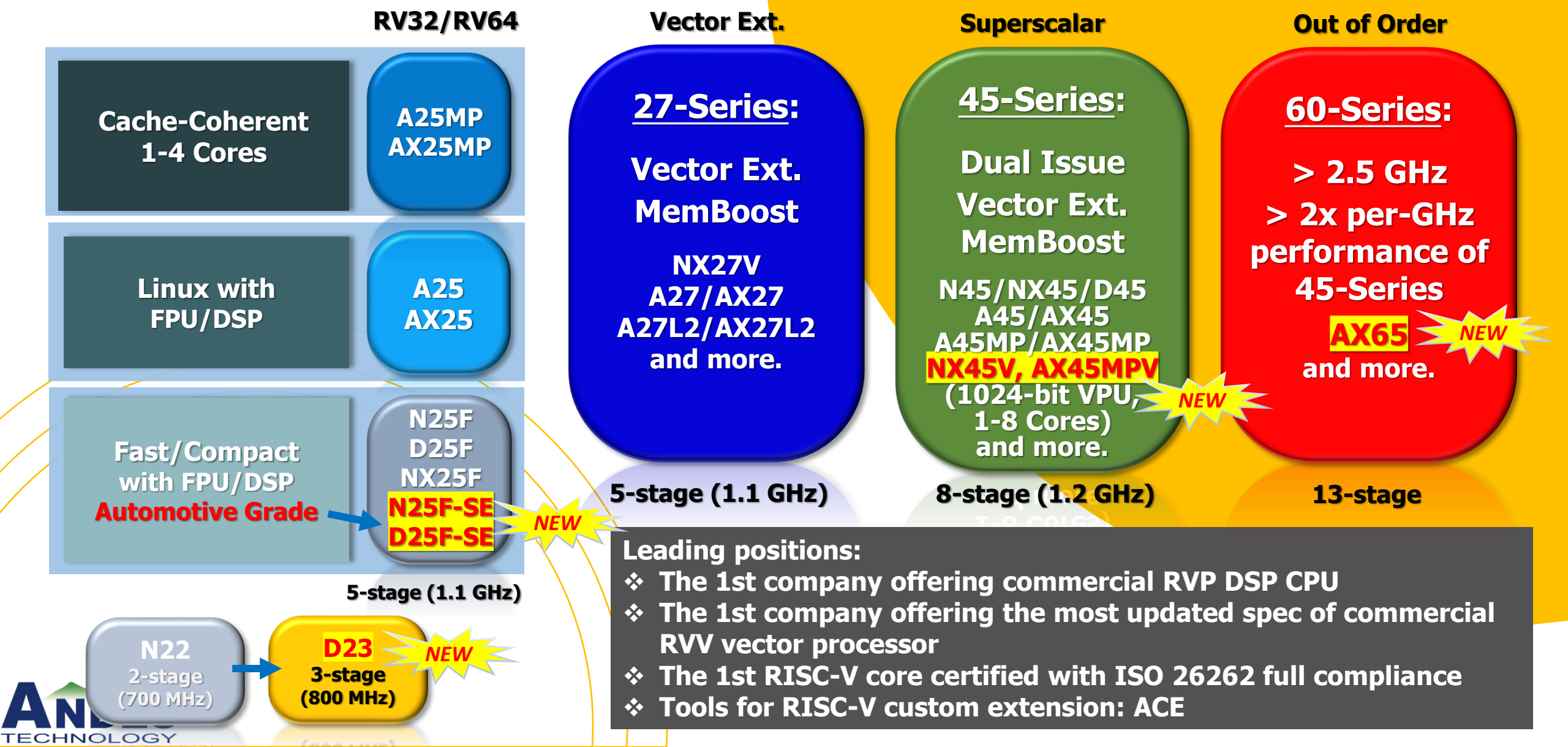
晶心RISC-V核心在SoC中被採用的數目



ANDES TECHNOLOGY

RISC-V

晶心RISC-V產品路線圖

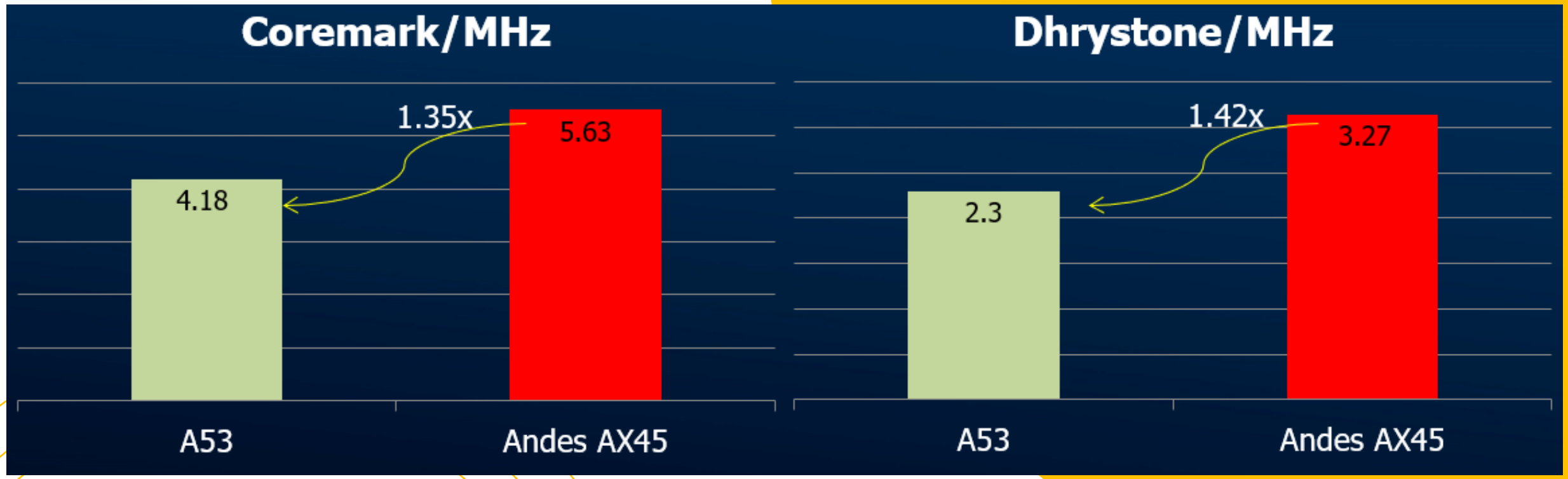


Leading positions:

- The 1st company offering commercial RVP DSP CPU
- The 1st company offering the most updated spec of commercial RVV vector processor
- The 1st RISC-V core certified with ISO 26262 full compliance
- Tools for RISC-V custom extension: ACE

ANDES TECHNOLOGY

AX45 Can Do More (vs. 64bit A-series)



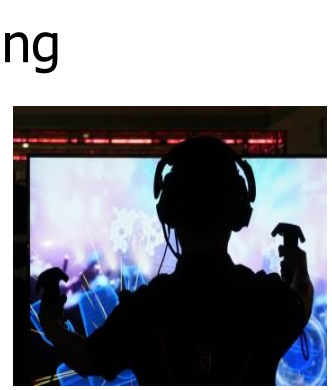
- **A53**
  - 8-stage In-Order Dual Issue
  - **Widely adopted by industries in many applications**

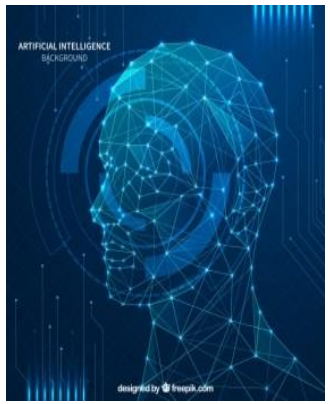
- **AX45**
  - 8-stage In-Order Dual Issue
  - **Performance is better!**
    - **Coremark/MHz: 1.35x**
    - **Dhrystone/MHz: 1.42x**

ANDES TECHNOLOGY

27 & 45系列產品的目標市場

- AI/Deep Learning
- AR/VR
- 5G





- Networking

- Storage

- Video Surveillance

- ADAS

- V2X (Vehicle to Everything)

- IVI (In-Vehicle-Infotainment)

Metaverse, HPC and more…

Toward 2023:
New Products and Ecosystems

http://www.andestech.com

AndesCore™ Lineup with Industry's 1st RISC-V Cores

- **D25F:** with **SIMD/DSP capability** (P-extension, 32/64 bits)
- **NX27V:** with **Vector Processing Unit** (V-extension, up to 512 bits)
- **N25F-SE:** with **ISO 26262 Full Compliance**, not just *Ready*

45 Series 8-stage superscalar	N45, NX45	D45	A45(MP) AX45(MP)		A53/55, R52/82, M7
27 Series 5-stage MemBoost		**NX27V**	A27(L2) AX27(L2)		A5/7/35
25 Series 5-stage fast & compact	N25F, NX25F	**D25F**	A25(MP) AX25(MP)	**N25F-SE**	A5/7/35, R4/5, M4/33
Entry Series	N22				M0/0+/3/33/4
Categories	*Embedded Control*	*DSP/Vector*	*Linux AP*	*FUSA*	*References*

AndesCore™ Roadmap Processors

AX60 Series 13-stage OOO MP		AX65	AX67	60-SE	A72~A76; N1/V1
Categories	*Power-efficient*	*Mid-range*	*Extended*	***FUSA***	
45 Series 8-stage Superscalar	N45, NX45	NX45V* D45	AX45MPV A45(MP), AX45(MP)	45-SE	A53/55, R52/82, M7
27 Series 5-stage MemBoost		**NX27V**	A27(L2), AX27(L2)		A5/7/35
25 Series 5-stage Fast&Compact	N25F, NX25F	**D25F**	A25(MP), AX25(MP)	D25F-SE^{B} N25F-SE^{B}	A5/7/35, R4/5, M4/33
Entry Series	N22	D23		23-SE	M0/0+/3/33/4
Categories	*Embedded Control*	*DSP/Vector*	*Linux AP*	*FUSA*	*References*

*Note *: AX45MPV configured as one core*

- **New Processors:** AX65, AX45MPV, D23, D25F-SE
- **Safety Enhanced (SE) Series:** at least one per year

AndesCore™ AX65

Multicore Out-of-Order Superscalar Processor

The Andes AX60 Processor Series

A new generation of AndesCore™

- Advanced Performance 13-stage Out-of-Order Superscalar Multicore
- Latest RISC-V Architecture
- Supported by Andes Long-term Roadmap
  - AX65 as the first member of the AX60 series
  - More products based on the AX60 micro-architecture planned, including for automotive functional safety

AndesCore™ AX65

- Offering performance surpassing CA72
- > 2.5 GHz, > 2x per-GHz performance of AX45MP
- Engaging with early customers

Preliminary Performance Results

AndesCore	AX27L2	AX45MP (over AX27L2)	AX65 (over AX45MP)
Micro-architecture	5 stage scalar in-order	8 stage dual-issue in-order	13 stage quad-issue OOO
Freq. (7nm)	~2 GHz	>2 GHz	>2.5 GHz
Coremark/MHz	3.55	5.64 (+59%)	9.17 (+63%)
Specint2k6/GHz	2.82	3.46 (+23%)	> 7 (>2x, target)
EEMBC FPMark/MHz	27.0	35.2 (+30%)	66.6 (+89%)
Linpack MFLOPS/MHz	0.130	0.220 (+69%)	0.613 (2.8x)
Mem Bandwidth[1]/MHz	1.0x	1.47x	1.90x

1. Based on standard library memcpy

AndesCore™ AX45MPV

Multicore 1024-bit Vector Processor

AX45MPV: Linux Multicore Vector Processor

A new member of popular AndesCore™ 45-series processors

- Inherits all features of AX45MP and leverages 3+ years of field experience from NX27V vector engine
- 64-bit 8-stage dual-issue processor
- Up to 8 cores SMP supporting up to 8MB L2 cache
- Dual-issue 1024-bit Vector Processing Unit (VPU) delivers up to 6 results per cycle

AndesCore™ AX45MPV

- Targets AI inference/training, ADAS, AR/VR, computer vision, multimedia
- Engaging with early customers

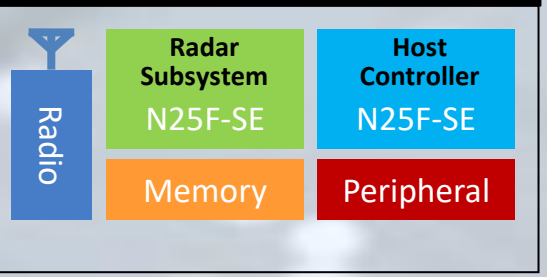
AndesCore™ D25F-SE / N25F-SE

Automotive Functional Safety(FUSA)

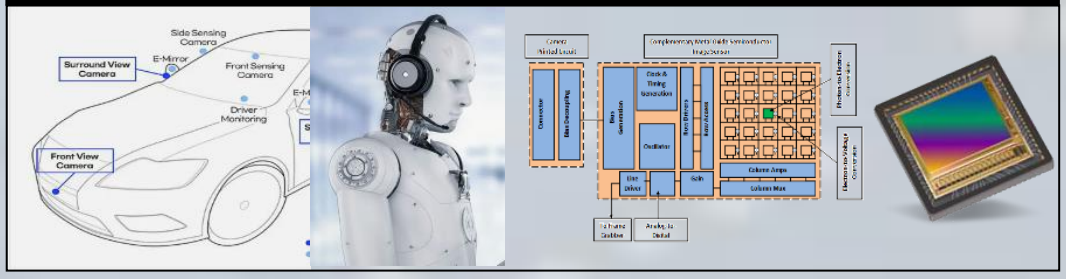
Andes is *Driving* Innovations in Automotive

with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

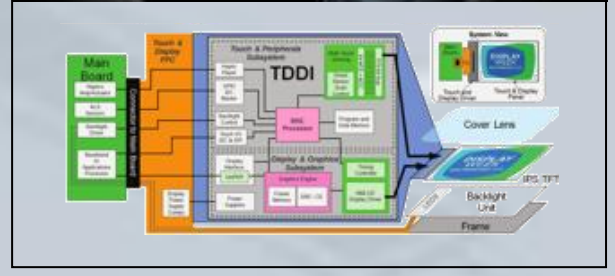
In-Cabin Radar



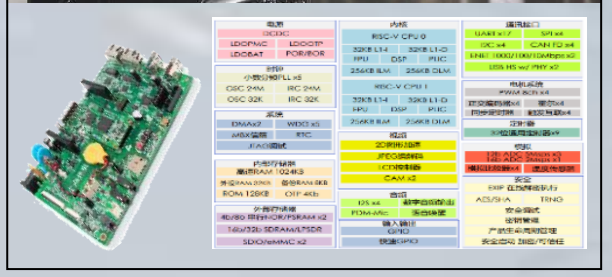
CMOS Sensor



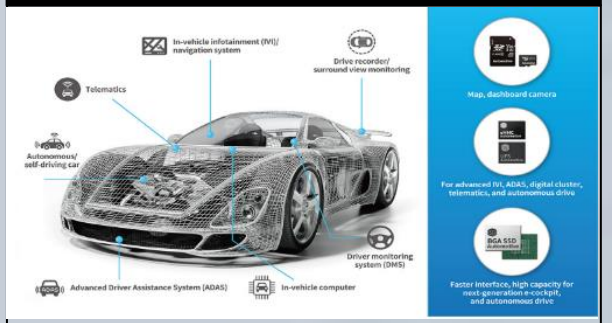
Auto TDDI

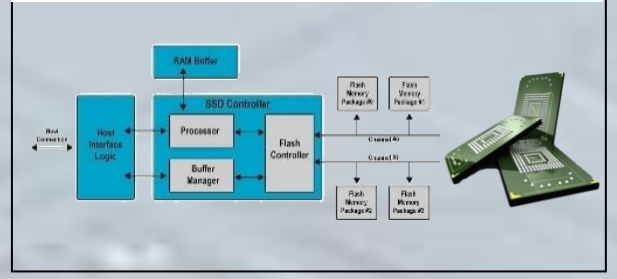


Auto MCU



Auto Storage





N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/20/0639 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY
TAIWAN R.O.C 30069

Project-No/-ID	LICENSED TEST MARK	Report No.
P30L	SGS TÜV SAAR FUNKTIONALE SICHERHEIT GEPRÜFT / FUNCTIONAL SAFETY APPROVED	P30L0001

Tested according to	ISO 26262:2018
Certified Process	Development process for Functional Safety related components up to ASIL D Version V1.0/202011
Technical Data/Parameter	The audited development process complies with the ISO 26262 standard part requirements ISO 26262-2:2018 ISO 26262-6:2018 ISO 26262-4:2018 ISO 26262-8:2018 ISO 26262-5:2018 ISO 26262-9:2018
Specific Requirements	The certificate is created for the purpose of providing conformity of the development and support process in accordance with ISO 26262. Changes which are not covered in the Audit Report have to be reconsidered.

Certification Body
for Functional Safety
SGS-TÜV Saar GmbH

Munich, December 22nd, 2020

Marcus Rau

The test mark regulation is an integral part of this certificate.

CERTIFICATE

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID	LICENSED TEST MARK	Report No.
S280	SGS TÜV SAAR ASIL B COMPLIANT Functional Safety ISO 26262	S2800001

Tested according to	ISO 26262:2018 (Parts 2, 4 partly, 5, 8, 9)
Certified Product(s)	CPU IP "N25F-SE" Version: R320
Technical Data/Parameter	The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance with **ASIL B** requirements.
Specific Requirements	The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval. The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body
for Functional Safety
SGS-TÜV Saar GmbH

The validation status is documented via SGS Certification Database.

The test mark regulation is an integral part of this certificate.

Munich, October 28th, 2022

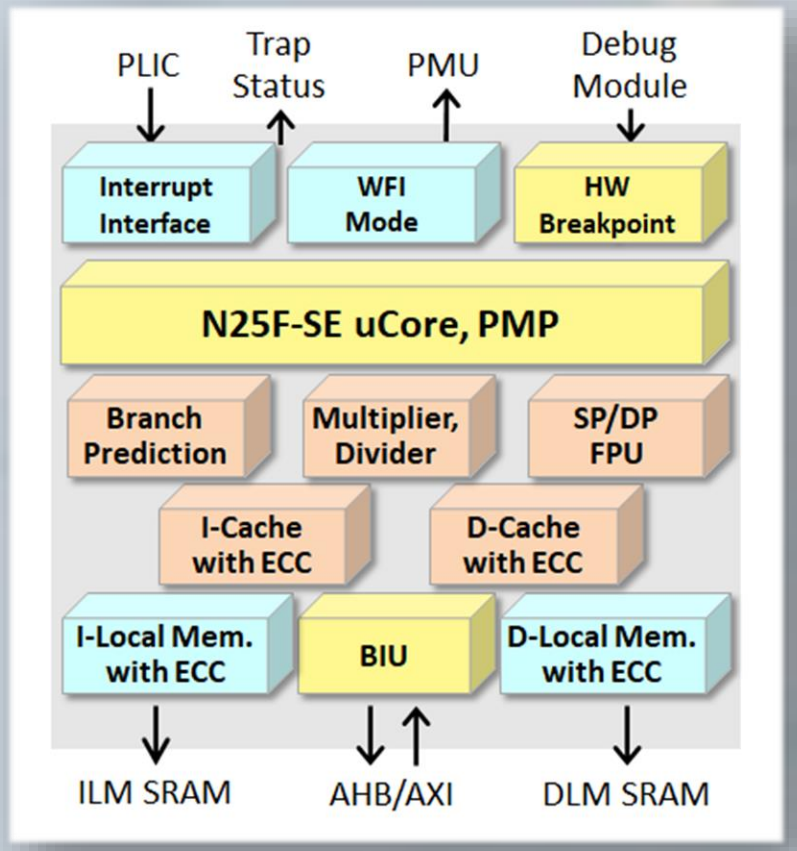
Marcus Rau

CERTIFICATE

- **ISO 26262 Certification for Development Process: ASIL-D**
  - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- **ISO-9001 QMS achieved and maintained since 2010**
- **ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE**
  - ISO 26262-2,4,5,8,9
  - Covers all the sections applicable to CPU core

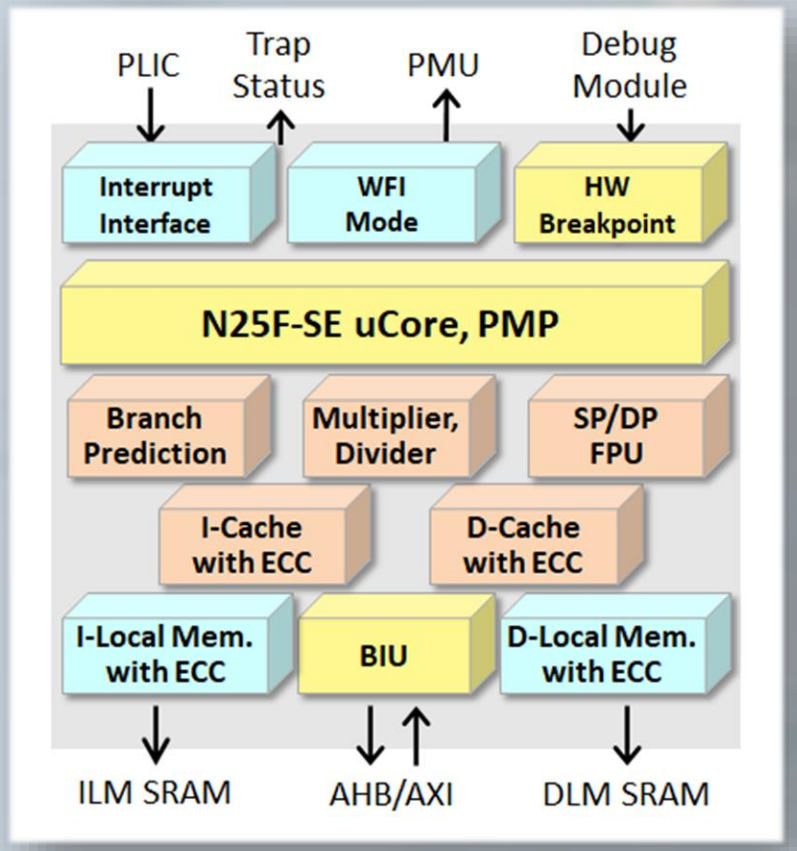
D25F-SE: FuSa processor with DSP/SIMD capability

- **CPU Core**
  - AndeStar™ V5 Instruction Set Architecture (ISA)
    - RISC-V 32-bit, RV32GC + Andes Extensions
    - RISC-V P(draft) and B extensions.
    - Machine+User (M+U) privilege levels
  - Dynamic branch prediction with BTB, BHT, RAS
  - CoDense™ code size reduction, StackSafe™ stack protection
- **Memory Subsystem**
  - Support I/D cache up to 32KB each
  - Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses
- **Bus Interfaces**
  - AXI or AHB bus master port
  - N:1 CPU clock vs. bus clock ratio
- **Others**
  - Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface
- **Safety Package including Safety Manual & FMEDA report**



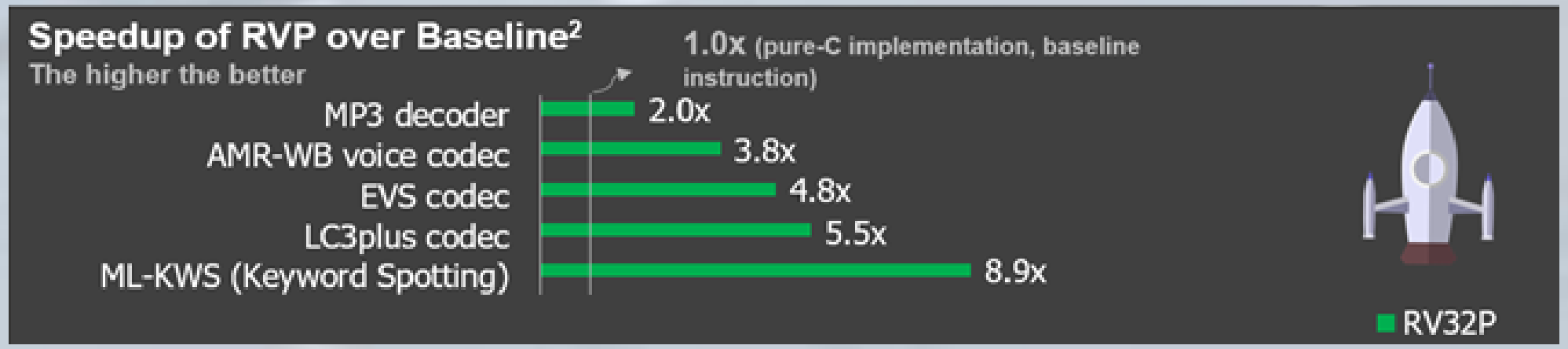
D25F-SE: FuSa processor with DSP/SIMD capability

- **CPU Core**
  - AndeStar™ V5 Instruction Set Architecture (ISA)
    - RISC-V 32-bit, RV32GC + Andes Extensions
    - RISC-V P(draft) and B extensions.
    - Machine+User (M+U) privilege levels
  - Dynamic branch prediction with BTB, BHT, RAS
  - CoDense™ code size reduction, StackSafe™ stack protection
- **Memory Subsystem**
  - Support I/D cache up to 32KB each
  - Support I/D local memory up to 16MB each, with slave port interface for bus master direct accesses
- **Bus Interfaces**
  - AXI or AHB bus master port
  - N:1 CPU clock vs. bus clock ratio
- **Others**
  - Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface
- **Safety Package including Safety Manual & FMEDA report**



D25F-SE with DSP and Bit-manipulation

- **RVP: Powerful DSP/SIMD instructions for audio/voice codec and endpoint AI/ML**
- **SIMD instructions such as a quad 8 x 8 accumulated into 32-bit data**
- **DSP library support of over 200 functions**



- **RVB: Efficient bit-manipulation operations for codes such as cryptographic & checksums**
  - Latest RVB ISA-extension Ver 1.0.0, including:
    - address generation, basic bit-manipulation, carry-less multiplication and single-bit instructions
    - Accelerate Crypto calculations: **27%** improvement on SHA256, **19%** for AES, **16%** for MD5

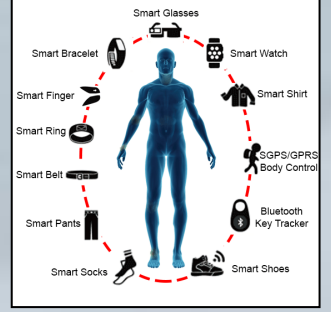
AndesCore™ D23

Compact, Secure, Low-Power Controller

D23 Targets Diverse Embedded & IoT Applications

DDI/TDDI

Wearable

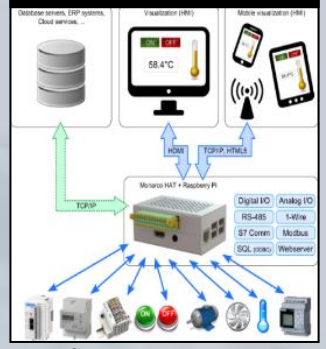


Smart Home

Motor Control

Connectivity

Embedded controller



Applications	D23 Capability fit
DDI, TDDI	Small gate count
Wireless controller core (WiFi, BT or others)	Security, small gate count
Smart Home Appliance	Security, performance, small gate count
Wearable	DSP (Edge AI), Security
E-Toys	DSP (Speech and Sound Processing)
RF Sensor control	DSP (Edge AI, Front-End Signal/Protocol Stack Processing)
MEMS/Sensor Fusion	DSP (Edge AI, Front-End Signal processing)
Battery or charging control	Performance
Advanced Motor Control	DSP

RISC-V: 2022 Toward 2023 & Beyond

- New Application Market

http://www.andestech.com

RISC-V Technology 2022 to 2023

- Drive Progression and Closure on Specs and Technical Deliverables

Item	2022	2023	% change
TGs	33	40	25%
SIGs	23	28	25%
ISA Spec Ratifications	2	20	1000%
non-ISA Spec Ratifications	4	11	275%
Profiles	-	6	N/A
Platforms	-	1	N/A

RISC-V®

Android Support for RISC-V

Courtesy of: Tech News

2023 & Beyond

- **Google Android will be ported to RISC-V**
- **The ecosystem will get more mature in 3 years**
- **Andes is committed in making its high end RISC-V CPU running Android in quality**
  - For example, 45 series AX45MP, 60 series AX65, and more higher end RISC-V cores
- **ChatGPT is hot yet "mainframe" style deployed, OpenAI put it in one neuro-network type of AI system**
  - Future trend is to make AI "edge" style or "personal" style, which will lead to further Edge AI revolution, SoC is still solution for future deployment
- **Andes will deliver such solution in terms of core hardware, developing platform, and software ported**

Thank You

http://www.andestech.com

+886-3-5726533

ANDES TECHNOLOGY

RISC-V®