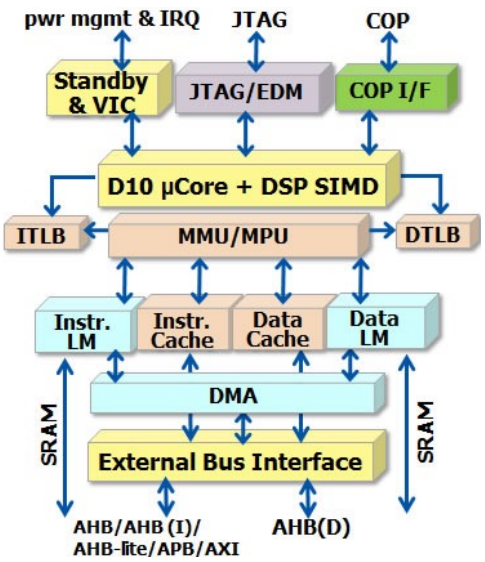
Andes e-Report

Content:

Andes Technology Corporation Launches New DSP+CPU Core Offering 134 Percent Higher Performance than Competing Alternatives for Low-Power SoC Designs

AndesCore™ D1088 CPU+DSP Combination Delivers Better Performance, Using Less Power with Half the Code Size of Competitive Offerings



Andes Technology Corporation, the leading Asia-based supplier of high-volume, low-power 32-bit embedded CPU cores, today announced the D1088, a 5-stage pipeline processor with integrated DSP offering 130 SIMD (single instruction, multiple data) instructions. When implemented in a 90nm low power process, the D1088 delivers 588 DMIPS, 134% higher than competing offerings. Measured using the popular Whetstone floating-point benchmark, the D1088 achieves 92% better

performance. When running popular and comprehensive (over 200) DSP libraries, the D1088 is 116% faster with half the code size. Even with the above advantages, the D1088 still achieves smaller die area and less power per MHz than competing offerings.

"We're proud of the results achieved with the D1088 DSP+CPU core," said Dr. Charlie Su, Chief Technology Officer and Senior VP of R&D at Andes Technology Corporation. "With the increasing numbers of designs performing signal processing for smart sensors, image processing, motion detection, audio and video, the D1088 will provide a wide range of benefits, including better compute performance and power savings, as well as additional functionality. The D1088 easily interfaces with both AHB and AXI bus for simplified use in SOC devices. It comes with an optional memory management unit to support the Linux OS and an optional memory protection unit to support real time operating systems (RTOS)."

About the D1088

Tightly integrated Integer and DSP processor architectures are not new, but most were designed for applications where power was not as much a constraint as it is today. The new D1088 was designed with low power in mind. It contains functionality to enhance efficiency and reduce application code size to lower both power and cost. For example, to significantly boost the computational efficiency in matrix, filtering, Fourier Transform, and statistics functions, it can execute 4-way 8-bit, or 2-way 16-bit SIMD instructions in a single-cycle latency. In addition, for multimedia applications, the D1088 also supports 64-bit add, subtract, and multiply mixed computation.

For voice application, the D1088 offers left shift, right rounding and shift, most significant word, 32x32 multiply and specially designed 32-bit instructions to replace the lengthy 64-bit computation. To reduce code size and increase efficiency, the D1088 provides a Zero Overhead Loop instruction to offload loop branching. To enhance parallel computational capacity, the D1088 provides left and right shift, minimum, maximum, and absolute value, besides traditional SIMD instructions such as add, subtract, and multiply.

Availability

D1088 is available immediately for customer uses and is fully supported by AndesSight™ Integrated Development Environment (IDE) tool chain.

Andes Technology Corporation Receives TSMC 2015 Partner of the Year Honor

TSMC Bestows Andes Technology Corporation Its 2015 Open Innovation Platform® Partner of the Year Award in New IP category

Andes Technology Corporation, Asia's leading supplier of small, low-power, high performance 32-bit embedded CPU cores, announced that it has been awarded TSMC's 2015 Partner of the Year award for New IP. Emerson Hsiao, Senior VP of Andes Technology USA Corporation was presented the award during TSMC's recent Open Integration Platform Ecosystem Forum that brought together TSMC's design ecosystem partners and customers to share solutions to today's design challenges.

"We are extremely proud that TSMC has honored Andes Technology Corporation with its 2015 Open Innovation Platform Partner of the Year," Hsiao said. "The CPU architecture that Andes Technology Corporation developed less than 10 years ago by its world class computer and software architects and engineers is shipping in over 700 million System on Chips, the vast majority of which have been fabricated at TSMC's leading edge foundry. We have worked closely with TSMC to ensure our IP can leverage the foundry's low power and high performance processes to help achieve the best power/performance results for our mutual customers."

"Andes Technology Corporation has developed into a valued TSMC partner," declared Suk Lee, Senior Director of TSMC's Design Infrastructure Marketing Division. "As TSMC has evolved to serve emerging markets such as the Internet of Things, we have expanded our ecosystem to support new products and customers. Having an emerging partner developing CPU IP to meet the low power needs of rapidly growing applications like IoT helps us serve this next generation of chip designs."

Andes and TSMC OIP Forum

The Andes Technology Corporation presentation "Tackling Power and Security Issues for IoT Devices," by Emerson Hsiao, Senior VP of Andes Technology USA Corporation has been selected for publication in the proceedings of the 2015 TSMC Open Integration Platform Ecosystem Forum. The CPU architecture that Andes Technology Corporation developed less than 10 years ago recognizes the new computing paradigm for low-power devices and includes hardware functionality specific for power savings required for machine-to-machine interaction. Andes' next generation 32-bit CPU core offers power savings far exceeding other legacy architectures in the same silicon footprint and with the performance of a high-end 32-bit CPU. "Tackling Power and Security Issues for IoT Devices," describes these power saving features and shows how new IoT devices can benefit from them.

Providing a Better Metric for Measuring Performance and Power in IoT SoCs

By: Emerson Hsiao, Senior VP Andes Technology Corp

The problem confronting chip designers developing IoT SoCs is the need for high computer performance and low power consumption. This is especially true for SoCs being developed for devices required to operate for years on a battery. One example is the new generation of electronic shelf label (ESL) with a requirement of 5 years running on button battery. The ESL receives central server pricing updates along with a few words of text that can occur as frequently as hourly. How does a design team select an embedded processor for such an application? One way is to use a benchmark that specifies some metric per MHz, such as the EEMBC CoreMark® to better evaluate alternative solutions.

Embedded processor for IoT devices, such as the ESL, is expected to provide security, communications, sensing and control, and power management. Robust security is essential to prevent network attacks, physical attacks and, to protect against software/firmware theft. Because IoT devices operate autonomously and provide data to remote clouds, low-power communications requires the processor to compute proprietary or standard protocols such as RFID, 802.15.4, Bluetooth Smart, Bluetooth 4.1, WiFi 802.11ah, and LTE Cat-0. Processing a variety of sensor data coming from the control interface requires versatile DSP capabilities. And power management is essential to enable months to years of operation on small batteries or harvested energy, thus demanding processors with efficient power management for long sleep cycles, fast power-up/power-down, and the ability to operate at varying clock frequencies—to sip energy rather than full-on or full-off. The EEMBC benchmark provides guidance on how well an embedded core will meet these requirements.

Built upon objective, clearly defined, application-based criteria, the EEMBC CoreMark benchmark reflects real-world applications and tests a processor's basic

pipeline structure, as well as the ability to test basic read/write operations, integer operations, and control operations. Over time, CoreMark has replaced Dhrystone MIPS as the industry standard for measuring processor, DSP, and compiler performance.

Andes Technology Corporation has taken the step of having all its processors certified to the EEMBC CoreMark® to provide designers a comparison metric to use in evaluating processors for their design. This month the company announced that the EEMBC Technology Center (ETC) has officially certified CoreMark results for the Andes' entire CPU product line. EEMBC certification ensures that scores are repeatable, accurate, obtained fairly, and derived according to EEMBC's rules. This certification is the most extensive carried out by any EEMBC member and ranges from the 2-stage pipeline Andes N705 CPU core, which achieved a CoreMark/MHz score of 3.32 to the 8-stage pipeline Andes N1337 CPU core that achieved a CoreMark/MHz score of 3.13 (see table below). The measurement of CoreMark/MHz can provide a good initial comparison of performance-efficiency among different cores with similar pipeline.

Processor	Pipeline Stages	CoreMark/MHz
Andes N705	2	3.32
Andes N801	3	3.05
Andes E801	3	3.51
Andes N968A	5	3.43
Andes N1068A	5	3.75
Andes N1337	8	3.13

Andes in the News

2015/10/17 SemiWiki

Extendible Processor Architectures for IoT Applications

Andes Technology President Frankwell Jyh-Ming Lin Will Present An Ultra Low Power IoT SoC Solution at Linley Group Processor Conference 2015

Capability Described in the Presentation "Developing an Ultra Low Power Processor For IoT Applications" Will be Demonstrated During Exhibition

Andes Technology Corporation, Asia's leading supplier of small, performance-efficient 32-bit embedded CPU cores, today announced that Andes President Frankwell Jyh-Ming Lin will Present at the Linley Group Processor Conference 2015 during Session 2 "IoT Client SoCs" from 1:50 to 3:20 pm on Tuesday October 6, 2015. Capability described during Mr. Lin's presentation "Developing an Ultra Low Power Processor for IoT Applications" will be demonstrated during the exhibition Tuesday evening.

"We are pleased to be presenting at the 2015 Linley Processor Conference, which is the premier forum for describing next generation processor architectures." Said Frankwell Jyh-Ming Lin, Andes President. "The rapidly developing Internet-of-Things market is redefining the computing requirements of today's embedded processor cores. Instead of CPU architectures that only produce more and more MIPS, IoT applications demand embedded cores that produce power-efficient performance to operate for years before battery recharge. Furthermore, IoT applications require cores with built in security to resist hacking. These are elements we've incorporated in our offerings and that enable us a advantage against competitive offerings, constrained by their legacy architectures."

About Linley Processor Conference

The Linley Processor Conference is a two-day forum featuring technical presentations addressing embedded processors for communications, IoT, and advanced automotive systems. This in-depth technical symposium has become the industry's premier event and features a number of new product announcements. In addition to over 20 technical presentations by experts from the companies leading the industry, the two-day conference program will include a keynote session covering technology and market trends in embedded processors. The conference is targeted at system designers, equipment vendors, OEM/ODMs, automakers and subsystem suppliers, service providers, press, and the financial community.

Andes Technology Corporation President Frankwell Lin's speech on Linley Processor Conference on Oct 6, 2015.

Andes Technology Corporation First Vendor to Use Official EEMBC Certified CoreMark® Results to Reveal the Performance for Its Entire CPU Product Line

Andes Technology Corporation First Vendor to Use Official EEMBC Certified CoreMark® Results to Reveal the Performance for Its Entire CPU Product Line

Andes Technology Corporation, the leading Asia-based supplier of small, low-power 32-bit embedded CPU cores, today announced that the EEMBC Technology Center (ETC) has officially certified CoreMark results for the company's entire CPU product line. EEMBC certification ensures that scores are repeatable, accurate, obtained fairly, and derived according to EEMBC's rules. This certification is the most extensive carried out by any EEMBC member and ranges from the 2-stage pipeline Andes N705 CPU core, which achieved a CoreMark/MHz score of 3.32 to the 8-stage pipeline Andes N1337 CPU core that achieved a CoreMark/MHz score of 3.13 (see table on the right). The measurement of CoreMark/MHz can provide a good initial comparison of how much power will vary between different cores for the same level of performance.

Processor	Pipeline stages	CoreMark /MHz
Andes N705	2	3.32
Andes N801	3	3.05
Andes E801	3	3.51
Andes N968A	5	3.43
Andes N1068A	5	3.75
Andes N1337	8	3.13

"Andes is extremely pleased to have completed the certification of all our cores on the CoreMark benchmark," said Charlie Hong-Men Su, Ph.D. Andes Technology CTO and Senior Vice President of R&D. "This represents the strength of our offering based on our CPU cores and the latest compiler technologies, which we continue to advance. Embedded applications where Andes cores find the greatest design activity are unique in that they require high performance, low power consumption, and small die size. CoreMark results, together with achievable frequencies, provide our customers a good initial indication of the amount of total performance each of our cores can achieve so they can select the core with the smallest silicon footprint and lowest power consumption to fit their end application. Once a customer selects a core, we often work with them to measure performance for their specific application, with the goal of keeping the power at a minimum. For example, a recent electronic shelf label design win needed to operate for five years on battery power and they chose an N801 core running 60 MHz."

"I'm very impressed with the extensive list of certified CoreMark results that Andes has revealed – clearly providing a great service to its customers. Furthermore, Andes is the first EEMBC member to have all of its processor cores certified for the CoreMark benchmark," said Markus Levy, EEMBC President. "As designers increase the number of cores going into embedded applications, especially the ultra low-power Internet of Things, CoreMark becomes less a measure of brute force performance and more a measure of the right amount of performance for a specific design goal."

About the Coremark Benchmark

Built upon objective, clearly defined, application-based criteria, the EEMBC CoreMark benchmark reflects real-world applications and tests a processor's basic pipeline structure, as well as the ability to test basic read/write operations, integer operations, and control operations. Over time, CoreMark has replaced Dhrystone MIPS as the industry standard for measuring processor, DSP, and compiler performance.

Andes Technology Joins the Thread Group

Andes Joins IoT Consortium Helping to Drive Adoption of Thread Wireless Networking Protocol

Andes Technology Corporation, the leading Asia-based suppliers of small, low-power 32-bit embedded CPU cores, today announced that it has joined The Thread Group, an industry organization dedicated to market education and product certification for Thread, a low-power, wireless mesh networking protocol designed to easily and securely connect hundreds of devices in the home. Andes intends to leverage its expertise in low power device design to incorporate Thread technology into their industry-leading, low-power CPU core portfolio, enabling secure, low-power Thread devices - such as thermostats, light bulbs and security cameras - for the connected home.

"Andes has deep experience in balancing the competing design requirements of IoT devices which will compose Thread mesh networks – intensive signal processing capacity, support for a wide range of sensor inputs, and years of battery life," said Charlie Hong-Men Su, Ph.D. Andes Technology CTO and Senior Vice President of R&D. "We look forward to incorporating Thread technology into CPU cores the size of an 8051, with sophisticated data handling functions found in power-hungry 32-bit and 64-bit processors, which can operate for years on a coin cell battery."

Andes Role in Thread

The additional value that Andes brings to the Thread Group is its intimate knowledge of extreme low-power operating capability. This is demonstrated by recent design wins in electronic shelf label and others that required operation on a coin cell battery for a minimum of 5 years. Andes also has deep roots in wireless communications protocols including WiFi and ZigBee. For example, Andes power-aware ZigBee stack implementation (AndesZ) can fit in a memory as small as only 12.7KB. Andes low power cores can support 802.11n WiFi driver with IP v6 stacks and 6LoWPAN, which in turn are the basis for WiFi Station and AP, DHCP, DNS, and HTTP.

About Thread

Designed for consumers and devices in and around the home, Thread easily and securely connects hundreds of devices to each other and directly to the cloud using real Internet Protocols in a low-power, wireless mesh network. The non-profit Thread Group is focused on making Thread the foundation for the Internet of Things in the home, educating product developers and consumers on the unique features and benefits of Thread and ensuring a great user experience through rigorous, meaningful product certification. Thread is backed by industry-leading companies including ARM, Big Ass Fans, Freescale Semiconductor, Nest Labs, Qualcomm, Samsung Electronics, Silicon Labs, Somfy, Tyco and Yale Security. Since opening its membership in October 2014, Thread has quickly grown to more than 160 members. For more information, please visit http://www.threadgroup.org.

Real Time Logic Joins Andes Technology Corp.'s New Internet of Things Community Knect.me™ to Provide Software Stack Solutions

Knect Partners Real Time Logic Provides Suite of Application/Web Server Development, Connectivity, and Security Software for Embedded Devices

Andes Technology Corporation, the leading supplier of small, low-power, high performance 32-bit embedded CPU cores, today announced that Real Time Logic has joined Knect.me, the new Internet of Things community that provides open-source, commercial solutions for connected devices. Real Time Logic brings to the Knect community its complete web-enablement, and secure connectivity portfolio for embedded devices to deliver dynamic control, fast enterprise-level security, and web functionality for industrial control, building automation, military, medical, and consumer markets. These include Barracuda Application Server™, SharkSSL™ "World's Fastest and Smallest SSL/TLS, Client and Server", SMQ IoT Protocol, Secure MQTT client machine-to-machine IoT Protocol, Barracuda Web Server, and PikeHTTPS Client.

"Real Time Logic is delighted to join the Knect community," said Wilfred Nilsen, CEO of Real Time Logic. "With the advent of the Internet of Things, developers building remote management and control systems have had to apply slow, memory-intensive enterprise-level point tools to the task. Real Time Logic solved the problem with our Barracuda Application Server Tools. It enables developers to deliver fast, secure, GUI-rich web server applications on compact, low-power devices. These extremely compact applications can meet the most stringent security requirements of today's proliferating variety of IoT applications. Being part of Knect, our solution can reach the expanding numbers of developers building IoT solutions."

"We are very pleased that Real Time Logic is providing its solutions to the Software Stack section of the Knect community," said Charlie Hong-Men Su, Ph.D. Andes Technology CTO and Senior Vice President of R&D. "The Knect Software Stack comprises software building blocks for smart devices and Internet of Things applications, including device drivers, real-

time operating systems, middleware, protocol stacks, and IoT APIs running on AndesCore. Because IoT devices operate autonomously, they are vulnerable to all the hacking attacks that plague the rest of the human connected world. Real Time Logic's expertise in securing machine-to-machine interaction provides users of Knect a best-in-class security solution to IoT designs with an Andes core."

About Knect

The Knect SoC IP Platform is intended to provide SoC developers with a complete solution and is comprised of the AndesCore™ and Andes platform IP along with partners' IP. The Knect Software Stack includes choices of open source software, and production-proven, certified and optimized software by Andes partners to fulfill a wide range of smart products and emerging applications development requirements. The Knect Development Boards include both FPGA based prototyping boards and ASIC based development systems. For prototyping from the chip level and up, IP cores such as Bus Matrix, DMA, SPI, and I2C controller serve as building blocks for customized designs. The Knect Development Tools include the AndeSight™ IDE and the open source GNU toolchain for AndesCore™. AndeSight™ Lite is a compact version of the Eclipse-based AndeSight™ IDE for free download. A no-cost evaluation version comes with all major functionality up to a code size of 32KB.

About Real Time Logic, LLC.

Real Time Logic products help developers create embedded web applications with dynamic, user-friendly interfaces on compact, low-power devices. We deliver fast, enterprise-level security and web functionality that meets today's demands for secure, remote application management and control. The company's web application and security tools are highly optimized for embedded devices in industrial control and building automation, military, medical, and consumer markets. Real Time Logic's proven technology has been incorporated into products manufactured by Honeywell, ABB, and large military suppliers and consumer products vendors around the world. Founded in 2006, Real Time Logic is headquartered in Monarch Beach, California, with a worldwide distributor and support network.

Security a Priority in a Smart Connected World

By: Jim Lipman Marketing Director, Sidense Corp

In the increasingly interconnected world that we are experiencing, fueled largely by the evolving IoT ecosystem, data and IP security is rapidly being recognized as a critical consideration for IoT-targeted devices and systems. In an ecosystem where everything is interconnected, each device must be highly secure, since a security breach on even one simple edge device can conceivably propagate to any other device on the network.

Sidense uses the term "Smart Connected Universe" as a compilation of traditional market segments, including mobile computing, IoT, wearables, automotive, industrial and medical, where a collection of devices are connected via a common network. Achieving the necessary level of security in the Smart Connected Universe requires the cooperative efforts of several types of semiconductor and silicon IP companies that contribute sensor, memory, communication core, cryptography and Trusted Execution Environment (TEE) technology, among others.

The memory technology these devices use must be both physically secure and tied in to proven cryptographic and other security technology, either intrinsically implemented or through the addition of third-party software and hardware. The end-game for all of the contributors to a secure Smart Connected device is to provide an environment that is safe from the many types of security attacks that exist both now and in the future.

As a provider of one-time programmable (OTP) memory, Sidense recognizes the important role secure memory plays working with a processor company such as Andes. Secure NVM performs multiple tasks at a processor-based IoT node, which includes sensor hubs and smart edge devices. The NVM technology must be highly secure when storing processor code, custom processor instructions and encryption keys. This requires an NVM technology that not only meets IoT requirements of low power and small footprint, but also provides a datain- place environment that is secure against hacking and malicious content extraction and modification.

Secure storage of custom processor instructions is of particular interest to processor developers. These instructions can not only be used for product differentiation and performance enhancement, but may also be employed to implement security features in a device, such as running encryption/decryption algorithms, which cannot be exposed to hackers.

An antifuse-based OTP memory that does not depend on charge storage has many attributes that makes it a good candidate for one-time and few-time programmable uses in Smart Connected devices. A programmed antifuse bit cell cannot be un-programmed with voltage, temperature or radiation. Beyond the intrinsic security of the antifuse-based bit cell, in which it is almost impossible to detect whether a bit cell is programmed or not, the

bit-cell-based OTP macros must also be designed to defeat hacking attempts.

Such design techniques include fully differential data storage and differential read modes, along with leakage compensation for un-programmed cells or for leakage induced by current and temperature manipulation, to prevent successful side-channel attacks. Another security feature is no power signature on charge-sensing read circuitry to prevent differential power analysis attacks. Furthermore, covering IO and memory array areas with metal layers that render the OTP dysfunctional when removed prevents visual detection of OTP properties by attacks utilizing process layer removal followed by scanning and inspection.

JIM LIPMAN, MARKETING DIRECTOR
SIDENSE CORP.

Sidense's Split-Channel antifuse-based 1T-OTP bit cell has the inherent security required in the Smart Connected Universe. The security of 1T-OTP macros has been confirmed by multiple independent analysis teams. The state of a 1T-Fuse™ bit cell is virtually impossible to detect using chemical etching, SEM and other conventional reverse engineering methods and a bit-cell state is not dependent on any charge storage. When programmed, a bit-cell undergoes a permanent structural change in a few atomic layers that cannot be altered by exposure to high temperature, voltage or

Andes Technology Corporation

Andes Technology Corporation was founded in Hsinchu Science Park, Taiwan in 2005 to develop innovative high-performance/low-power 32-bit processor cores and its associated development environment to serve worldwide rapidly-growing embedded system applications. It delivers the best super low power CPU cores with integrated development environment and associated software and hardware solutions for SoC development.

In order to meet demanding requirements of today's electronic devices, Andes delivers configurable software/hardware IP and scalable platforms to respond to customers' needs for quality products and faster time-to-market. Andes' comprehensive CPU includes entry-level, mid-range, high-end, extensible and security families to address full range of embedded electronics products, especially for connected, smart and green applications.