Andes University Program

- There are three universities signed up in US
- In Taiwan we supported thirty-six universities and colleges

<table>
<thead>
<tr>
<th>US University signed up</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCLA</td>
</tr>
<tr>
<td>Univ of Utah</td>
</tr>
<tr>
<td>University of Florida</td>
</tr>
</tbody>
</table>
University Program Introduction

❖ Upon signing the agreement, Andes donates the following IP cores and development IDE tools.

❖ **AndesCore™:**
  - Three (3) design usages are granted in total and can be chosen from Andes N22, 25-Series, 27-Series or 45-Series CPU IP. Academic use only, not for commercial use.
    - If turn from academic use to commercial use, apart commercial license agreement shall be signed.

❖ **AndeSight™:**
  - Sixty (60) usage licenses are granted. Academic use only, not for commercial use.
## Status of RISC-V Project in Various Universities

<table>
<thead>
<tr>
<th>University</th>
<th>CPU</th>
<th>Application</th>
<th>Delivery</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTU</td>
<td>N25</td>
<td>Seizure Prediction Algorithm</td>
<td>2018/07</td>
</tr>
<tr>
<td>NCTU</td>
<td>N25</td>
<td>Security</td>
<td>2018/10</td>
</tr>
<tr>
<td>NSYSU</td>
<td>N22</td>
<td>Sensing system</td>
<td>2019/11</td>
</tr>
<tr>
<td>NCU</td>
<td>N25F</td>
<td>3D Hand Gesture Recognition</td>
<td>2019/12</td>
</tr>
<tr>
<td>CCU</td>
<td>N22</td>
<td>Dysarthria voice conversion</td>
<td>2019/12</td>
</tr>
<tr>
<td>NTU</td>
<td>N25F</td>
<td>AIoT</td>
<td>2020/02</td>
</tr>
<tr>
<td>CCU</td>
<td>N25F</td>
<td>Dysarthria voice conversion</td>
<td>2021/01</td>
</tr>
</tbody>
</table>
Founded in March 2005, Andes Technology is the provider of innovative embedded processors and SoC platform solutions.

RISC-V IP licensing specialist

The ONLY independent, pure-play CPU IP provider

220+ employees of which 80% are R&D staffs and engineers

99% gross margin with 27% of recurring revenue from royalties in 2020

200+ licensees

500+ agreements signed

AndeSight™ IDE: 20,000+ installations

160+ partners

7bn+ accumulated SoC shipments

TSMC OIP(1) Award “Partner of the Year” for New IP (2015)

Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)

Al Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)

Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)

(1) The TSMC Open Innovation Platform (“OIP”) initiative is a comprehensive design technology infrastructure that encompasses IC implementation areas to reduce design barriers and improve first-time silicon success.
Andes Successful Commercial Stories

- **Andes Custom Extension**
- **Vector Processor**
- **Interface Customization**
- **Advanced Tools**
- **Custom AndeSight**

**Implementation and Verification Service**: Taiwan customer 5G

**AndesCore™ Vector and ACE Extension**: USA customer Cloud training

**AndesCore™ Interface Customization**: China customer TWS

**Compiler and Debugging Support**: USA customer Cloud inference

**High Performance and Cycle Accurate Analysis Tool**: China customer AIoT
Andes RISC-V Processor Lineup

**Cache-Coherent 1-4 Cores**
- RV32: A25MP, A25
- RV64: AX25MP, AX25

**Linux with FPU/DSP**
- RV32: N25F, D25F
- RV64: NX25F

**Fast/Compact with FPU/DSP**
- RV32: 5-stage (1.1 GHz)
- RV64: 5-stage (1.1 GHz)
  - Vector Ext.: MemBoost, Vector Ext.

**Superscalar**
- RV32: 8-stage (1.2 GHz)
- RV64: 8-stage (1.2 GHz)
  - Vector Ext.: MemBoost, Dual Issue.
  - 45-Series: N45/NX45, D45/DX45, A45/AX45, A45MP, AX45MP

**Note:** Common features are RV*IMACN, Caches, LM, ECC, BrPred, CoDense™, PowerBrake, StackSafe™, ACE (Andes Custom Extension™); Frequencies at 28nm.
Andes V5 Product Overview

Best extensions to RISC-V

AndeStar™ Architecture

Highly optimized design with leading PPA

AndesCore™ Processors

Handy peripheral IPs to speed up SoC construction

AndeShape™ Platforms

Professional IDE with high code quality

AndeSight™ Tools

Extensive SW stacks from bare metal, RTOS to Linux

AndeSoft™ Stacks
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Thank You

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