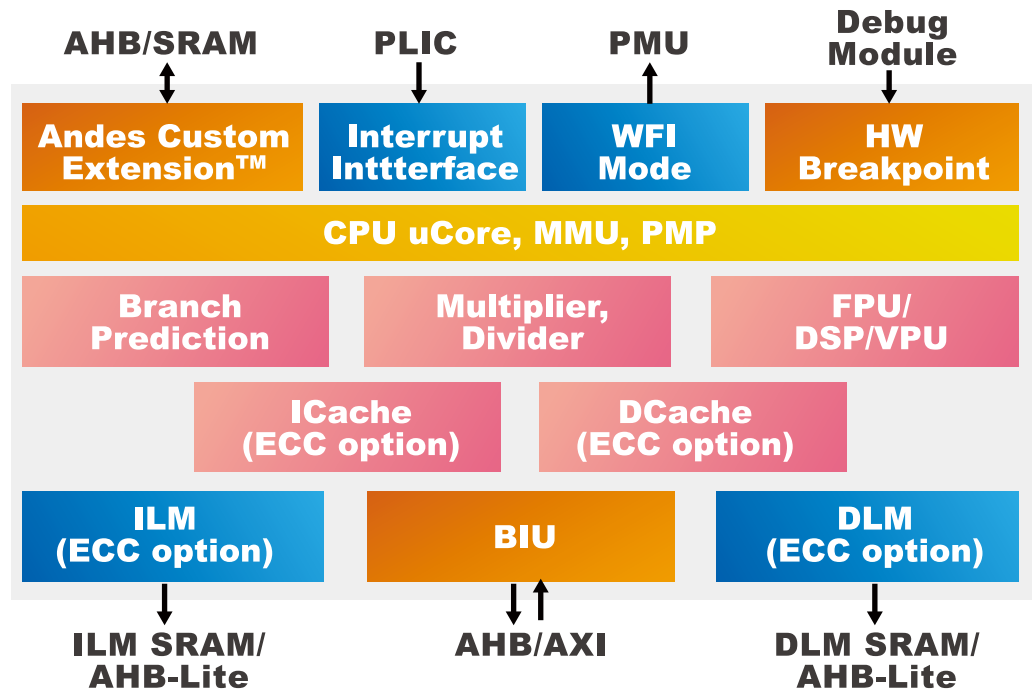


Andes Core



# AndesCore™ RISC-V®

AndesCore™ is a series of high performance CPU core families geared to diverse market segments of today's emerging embedded applications. The versatile and rich features of the AndesCore™ families allow flexible SoC customizations based on the application needs in a design to improve platform performance and reduce system cost. In addition, the processors employ various commonly-used low power design techniques to save energy and further allow smart SoC level power management for better energy/performance outcome.



\*Availability of the above function blocks varies on each core

## AndesCore™ : Performance, Power and Area

| V5 Processors<br>RISC-V  | Pipeline Stage | Best DMIPS (/MHz)% | Best CoreMark (/MHz) | Max Freq. * | Power * | Gate Count * (K) |
|--|----------------|--------------------|----------------------|-------------|---------|------------------|
| <b>N22</b><br>Ultra compact RISC-V core                          | 2              | 1.80               | 3.95                 | 700 MHz     | 2.42    | 15.8             |
| <b>N25F</b><br>32-bit Compact, High Performance                  | 5              | 1.98               | 3.57                 | 1.2 GHz     | 17      | 127              |
| <b>NX25F</b><br>64-bit Compact, High Performance                 | 5              | 2.14               | 3.55                 | 1.2 GHz     | 18      | 172              |
| <b>D25F</b><br>32-bit High Performance with DSP                  | 5              | 1.98               | 3.57                 | 1.1 GHz     | 17      | 186              |
| <b>A25</b><br>32-bit High Performance, Linux                     | 5              | 1.98               | 3.57                 | 1.1 GHz     | 17      | 144              |
| <b>AX25</b><br>64-bit High Performance, Linux                    | 5              | 2.14               | 3.55                 | 1.1 GHz     | 20      | 193              |
| <b>A25MP</b><br>32-bit Multicore, Linux SMP                      | 5              | 1.98               | 3.57                 | 1.1 GHz     | #       | 880              |
| <b>AX25MP</b><br>64-bit Multicore, Linux SMP                     | 5              | 2.14               | 3.55                 | 1.1 GHz     | #       | 1076             |
| <b>A27</b><br>32-bit with MemBoost, Linux                        | 5              | 1.98               | 3.57                 | 1.1 GHz     | 21      | 223              |
| <b>AX27</b><br>64-bit with MemBoost, Linux                       | 5              | 2.14               | 3.55                 | 1.1 GHz     | 23      | 273              |
| <b>A27L2</b><br>32-bit with MemBoost/L2, Linux                   | 5              | 1.98               | 3.57                 | 1.1 GHz     | 27      | 427              |
| <b>AX27L2</b><br>64-bit with MemBoost/L2, Linux                  | 5              | 2.14               | 3.55                 | 1.1 GHz     | 30      | 477              |
| <b>NX27V</b><br>64-bit with Vector Extension                     | 5              | 2.14               | 3.55                 | 1.2 GHz     | #       | #                |
| <b>N45</b><br>32-bit Superscalar                                 | 8              | 2.86               | 5.67                 | 1.4 GHz     | 25.6    | 300              |
| <b>NX45</b><br>64-bit Superscalar                                | 8              | 3.27               | 5.63                 | 1.3 GHz     | 29.1    | 396              |
| <b>D45</b><br>32-bit Superscalar with DSP                        | 8              | 2.86               | 5.67                 | 1.1 GHz     | 25.9    | 354              |
| <b>A45</b><br>32-bit Superscalar Application Processor, Linux    | 8              | 2.86               | 5.67                 | 1.2 GHz     | 27.5    | 450              |
| <b>AX45</b><br>64-bit Superscalar Application Processor, Linux   | 8              | 3.27               | 5.63                 | 1.2 GHz     | 32.0    | 586              |
| <b>A45MP</b><br>32-bit Superscalar Application Processor, Linux  | 8              | 2.86               | 5.67                 | 1.1 GHz     | 27.6    | 510              |
| <b>AX45MP</b><br>64-bit Superscalar Application Processor, Linux | 8              | 3.27               | 5.63                 | 1.1 GHz     | 30.0    | 715              |

% no-inline ground rules.

\* All cores at 28nm except NX27V at 7nm. N22 configured with minimum useful configuration (small multiplier, static branch prediction). N(X)25F and D25F configured with 256-entry BTB, 16-entry PMP and 32KB L1 I/D cache, without FPU; A(X)25MP, A(X)27/L2 in addition with 128-entry TLB, without DSP; A(X)25MP configured with 4 cores, A(X)25MP and A(X)27L2 with 256KB L2 cache. Synthesis with 28nm process slow silicon, 0.9Vdd, 125°C with I/O constraint. Power reported at typical process corner, Vdd, 25°C. Power and gate count are core only at 1GHz. NX27V configured with VLEN=512bit and 512-bit AXI bus. Synthesis with 7nm process, 0.675V/0°C with I/O constraint, Dhrystone program.

N(X)45 and D45 configured with 256-entry BTB, 16-entry PMP and PMA, and 32KB L1 I/D cache, without FPU; A(X)45/A(X)45MP in addition with 128-entry TLB. All 45-series (except A(X)45MP) data does not include DSP; A(X)45MP do not include L2 cache controller. Synthesis with 28nm process slow silicon, 0.9Vdd, 125°C with I/O constraint. Power reported at typical process corner, Vdd, 25°C running Dhrystone benchmark. Power and gate count are core only @ Data are subject to change without notice. A(X)45MP power/area are for single core only.

# Contact Andes for details.

# AndeSight™

## Software Developer's Environment

### General Description

AndeSight™ is an Eclipse-based integrated development environment (IDE) which provides an efficient way to develop embedded applications for AndesCore™ based SoCs.

### Features

#### AndeSight™

- Eclipse-based IDE
- Project management
- Managed build system
- Feature-rich editor
- Source level debugger
- Profiling analysis
- In-System programming
- RTOS awareness debugging
- Break and display on exceptions
- Register Bitfield viewing and update
- Multicore development support
- Custom UI
- AndeStar™ V5 CPU support
- Extensive demo projects
- Flexible license control
- Corvette F1 (Arduino-Compatible board) support

#### Toolchains

- Compiler for ELF and Linux targets
- Andes efficient ROM patch solution
- Highly optimized DSP library functions
- Highly optimized libc functions

#### Simulator

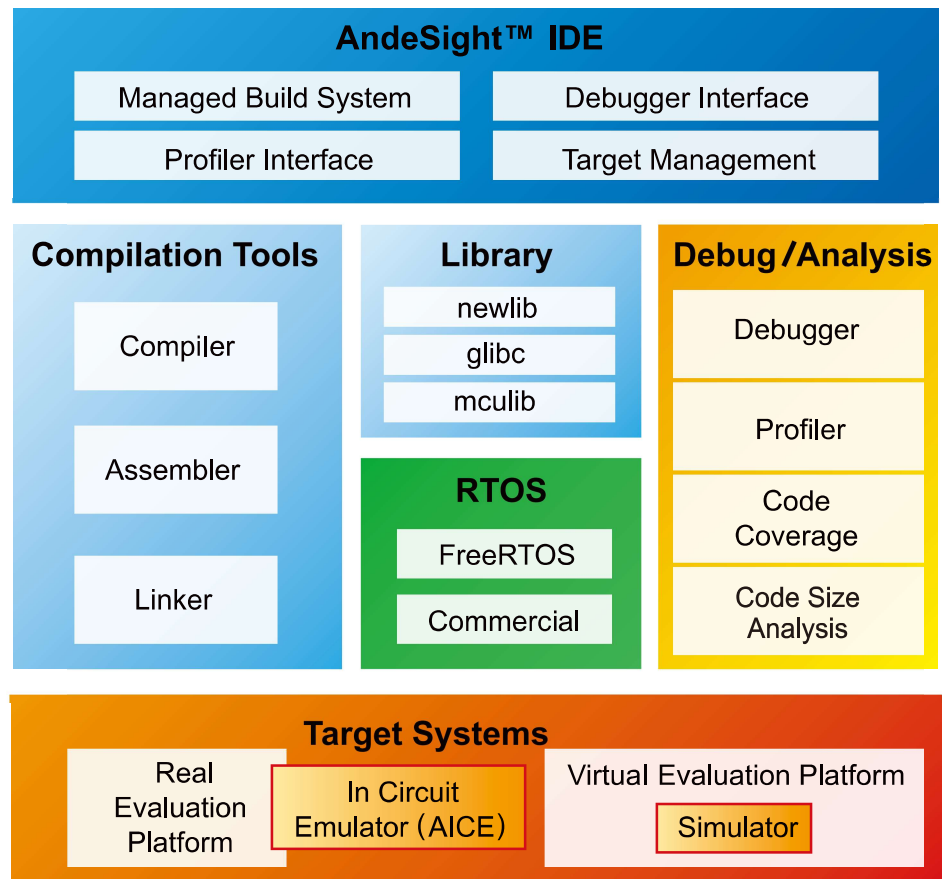
- CPU simulator(near-cycle accurate)
- Models of AndeShape™ SoC platform

#### ICE

- AICE debugger (4-wire/2-wire) with OpenOCD support

### Supported Host Platforms

- Windows 7 / Windows 10
- Ubuntu Linux 18.04 / CentOS 7.0 / Red Hat Linux 7.0



### Two AndeSight™ Versions:

#### STD

A comprehensive IDE with highly-optimized compilers, all GUI features, and Linux support.

#### RDS

Based on AndeSight™ STD with additional customization features for customers' redistribution.



# AndeStar™ Architecture

The AndeStar™ V5, the latest generation of Andes architecture, consists of both 32-bit and 64-bit register architectures with mixed-length 16/32-bit instructions. It adopts the RISC-V technology as its subset and benefits from the fast growing RISC-V ecosystem. Together with the merits of performance enhancement extensions inherited from V3, the third generation RISC-style architecture, the AndeStar™ V5 brings compact, modular and customizable advantages to SoC applications. As a founding Premier member of the RISC-V International Association, Andes is determined to take RISC-V to the mainstream.

## AndeSoft™

### Building Blocks for System - AndeSoft™ Software Components

With AndeSight™ IDE, users can develop software with hardware in a seamlessly integrated environment efficiently. To speed up the development process, Andes further provides a rich set of software components, from Real-Time Operating System, Linux kernel and drivers, libraries, and middleware, to application frameworks, running on AndesCore™ processors under the name AndeSoft™. Users can leverage those well-prepared and verified building blocks based on their needs and focus on tackling products to greatly improve time-to-market.

#### Fundamental

- Compiler and toolchain are contributed to and supported officially by **GNU** and **LLVM** communities
- Optimized C libraries: **MCUlib**, newlib and glibc
- Optimized low-level compute libraries for NN, DSP and vector processing: **libnn**, **libdsp**, **libvec**
- Concise linker script and its tools, **Linker Scattering-and-Gathering (LdSaG)**
- **Bare-metal drivers and demo programs** to demo AndesCore™ features
- Virtual platforms: **AndeSim™** (near cycle-accurate), **AndeSysC™** (SystemC library), **Qemu**

#### Real-Time Operating System

- Open source port on Andes: **Zephyr**, **FreeRTOS**
- Commercial port on Andes: **Azure RTOS ThreadX**, **RT-Thread**, **SylixOS**

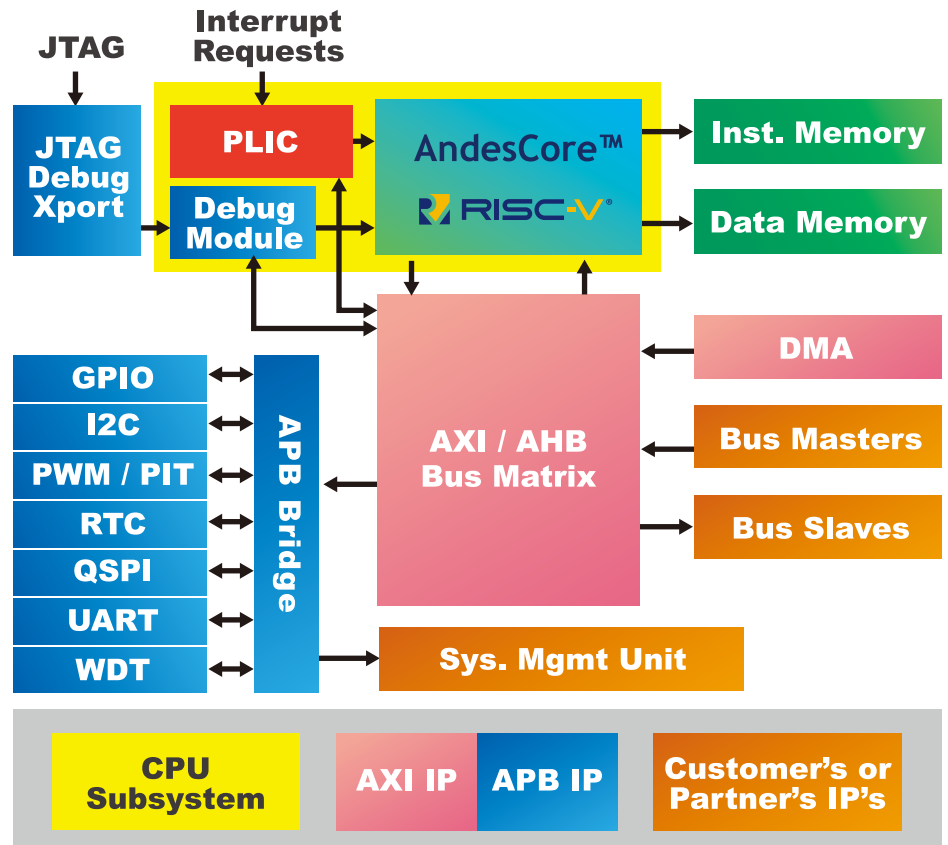


#### Linux, Middleware and SW Framework

- **Linux kernel** since 4.17 and LTS v5.4, device drivers and advanced features: **strace**, **ftrace**, **Perf**, **SMU**, **power throttling**, **suspend-to-RAM** and **kernel module**
- **U-Boot**, **OpenSBI** and **BBL**
- **Andes6**: connect LPWAN to IPv6 seamlessly

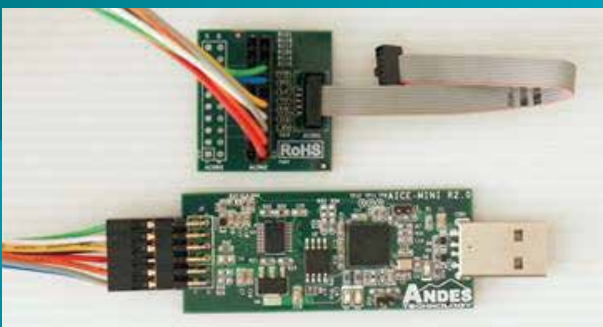
# AndeShape™

The AndeShape™ development platform includes variety of hardware entitles, such as pre-platform IPs, ICE debuggers (AICE), and hardware evaluation boards for AndesCore™ processor based system development. To satisfy the best quality-of-result (QoR) requirements for different system applications, various platform IPs are available with different bus and datapath structures. In addition to a basic set of connectivity and storage devices, the rich set of hardware options in both board and SoC levels enable versatile flexibility in hardware/software co-development and early prototyping.



- \* Platform is pre-integrated with CPU
- \* Availability of platforms varies on each core

The comprehensive debugging support, including in-system programming, self-diagnosis, and embedded ICE, greatly reduces the system development cycle while maintaining the quality of design.



**AndeShape™ AICE-MINI+**



**AndeShape™ ADP-XC7KFF676 EVB**



**AndeShape™ AICE-MICRO**

## About Andes Technology

Andes Technology, the first CPU IP supplier in Asia, has been devoting to the development of innovative high-performance/low-power 32/64-bit processors and associated SoC platforms since its foundation in 2005. Its powerful CPU lineup covering entry-level, mid-range, high-end, extensible and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 9 billion SoC shipment containing Andes IP up to 2021. While delivering advanced features based on proprietary ISAs, as the Founding Premier member of RISC-V International Association, Andes is also the first mainstream CPU vendor adopting the open RISC-V. For more information about Andes' products, technologies and services, please contact us through the following:

### Headquarters

10F., No. 1, Sec. 3, Gongdao 5th Rd.,  
East Dist., Hsinchu City,  
Taiwan R.O.C 30069  
Tel : +886-3-5726533  
Fax : +886-3-5726535  
E-mail : sales@andestech.com  
www.andestech.com

### Shanghai

Tel: +86-21-50310722  
Mobile: +86-136-8186-2493  
Room 303A, No. 500, Bibo Rd, Pudong District,  
Shanghai, China  
Business : sales.sh@andestech.com  
technical : support.sh@andestech.com

### USA

2860 Zanker RD, Suite 104,  
San Jose CA 95134  
Tel : 1-408-809-2929  
Business : america@andestech.com  
Technical : support.usa@andestech.com

### Shenzhen

Mobile: +86-184-1103-1047  
Business : sales.sz@andestech.com  
Technical : support.sz@andestech.com

### Korea

Business : sales.korea@andestech.com  
Technical : support.korea@andestech.com

### Beijing

Mobile : +86-139-1037-7174  
Business : sales.bj@andestech.com  
Technical : support.bj@andestech.com

### Japan

Business : sales.japan@andestech.com  
Technical : support.japan@andestech.com

### Europe

Business : europe@andestech.com  
Technical : support.europe@andestech.com

