Andes Corporate Overview

<table>
<thead>
<tr>
<th>Silicon Valley Ties</th>
<th>• Core R&amp;D from AMD, DEC, Intel, MIPS, nVidia, and Sun</th>
</tr>
</thead>
</table>
| 15-Year CPU IP Company | • IPO in 2017; HQ in Taiwan  
• AndeStar™ V1-V3, V5 (RISC-V) |
| >1 Bn Annual Run Rate of Andes-Embedded SoC | • ~300 customers in TW, CN, US, EU, JP, KR |
| Founding Platinum Member and Major Contributor | • Chairing Task Groups  
• Contributing to GNU, LLVM, uBoot, glibc, Linux, etc. |
Andes Product Overview

Best extensions to RISC-V

AndeStar™ V5 Architecture

AndesCore™ Processors

Highly optimized design with leading PPA

AndeSight™ Tools

Professional IDE with high code quality

AndeShape™ Platforms

Handy peripheral IPs to speed up SoC construction

AndeSoft™ Stacks

Extensive SW stacks from bare metal, RTOS to Linux

2020 RISC-V CON Webinar
Agenda

- Overview of Tools and Runtime Support
- AndeSight™ IDE: Simulator, Compilation and debugging
- AndeSoft™ BSP: Bare Metal, RTOS, Linux and DSP ISA
- Summary
SoC SW Development Environment

AndeSight™ IDE
- Eclipse-Based IDE
- Streamlined GUI
- Feature-rich Editor
- Managed Build System
- Optimized Toolchains
- Source Level Debugger
- Profiling Analysis
- Extensive Demo Projects
- Flash ISP

AndeSoft™ SW Stack
- Application Layers
- Middleware
- Drivers
- App Drivers
- OS/Kernel
- Libraries

AndeShape™

Virtual SoC
- AndesCore™
- Bus Controller
- NVIC 10/100
- SMI Controller
- USB2.0
- LCD Controller
- SDRAM Controller
- DMA Controller
- SRAM Controller
- PWM
- I2C
- GPIO
- INT
- WDT
- Timer
- RTC
- ST
- UART
- BT
- UART
- SSP
- CF
- I²C
- MHC

Andes/Partners’ Solutions
- Customers’ Designs

Profiling/Tracing/Debugging data

Virtual SoC Configuration
Overview of Tools and Runtime Support

**AndeSight™ IDE**
- **Simulator:** AndeSim (near-cycle accuracy), Qemu
- **Compilation:** GNU toolchain, LLVM compiler/linker, optimized MCU library, DSP library
- **Debugging:** GDB, speed-optimized OpenOCD, USB-to-JTAG ICE cable

**AndeSoft™ BSP**
- Several Bare metal sample projects for Andes-specific features
- **RTOS:** FreeRTOS, Zephyr, LiteOS, RT-Thread
- **Linux:** MMU/TLB support, LTP tested
- Arduino support for Andes Corvette-F1 FPGA board
AndeSight™ IDE
Comprehensive Development Environment
AndeSight™: Professional IDE

**Project Setup:**
- Meta linker script editor
- Flash ISP configured through GUI

**Debug Support:**
- Virtual hosting
- Register Bitfield display/update
- Break-n-Display on exceptions
- Script-Based RTOS awareness
- Stack protection handling

**Custom Plugin Interface**
AndeSight™: Profiling

- Program Analysis
  - Function Profiling
  - Code Coverage
  - Performance Meter
  - Function Code Size
  - (Static) Stack Size
Global Variables Live View

- Runtime updating global variables in a fixed interval
- Highlight the changes in yellow

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>audio</td>
<td>struct audio</td>
<td>{...}</td>
<td>0x534c88 &lt;audio&gt;</td>
</tr>
<tr>
<td>start</td>
<td>unsigned char *</td>
<td>0x01000000</td>
<td>0x534c88 &lt;audio&gt;</td>
</tr>
<tr>
<td>data_sz</td>
<td>unsigned long</td>
<td>661248</td>
<td>0x534c8c &lt;audio+4&gt;</td>
</tr>
<tr>
<td>samplerate_init</td>
<td>unsigned char</td>
<td>1</td>
<td>0x534c90 &lt;audio+8&gt;</td>
</tr>
<tr>
<td>samplerate</td>
<td>unsigned short</td>
<td>48000</td>
<td>0x534c92 &lt;audio+10&gt;</td>
</tr>
<tr>
<td>samplesize_init</td>
<td>unsigned char</td>
<td>1</td>
<td>0x534c94 &lt;audio+12&gt;</td>
</tr>
<tr>
<td>samplesize</td>
<td>unsigned short</td>
<td>16</td>
<td>0x534c96 &lt;audio+14&gt;</td>
</tr>
<tr>
<td>channels_init</td>
<td>unsigned char</td>
<td>1</td>
<td>0x534c98 &lt;audio+16&gt;</td>
</tr>
<tr>
<td>channels</td>
<td>unsigned short</td>
<td>1</td>
<td>0x534c9a &lt;audio+18&gt;</td>
</tr>
<tr>
<td>ssp</td>
<td>ssp_regs_t *</td>
<td>0x99400000</td>
<td>0x534c60 &lt;ssp&gt;</td>
</tr>
<tr>
<td>D</td>
<td>const mad_fixed_t</td>
<td>[...</td>
<td>0x51596c &lt;D&gt;</td>
</tr>
<tr>
<td>mad_timer_zero</td>
<td>const mad_timer_t</td>
<td>[...]</td>
<td>0x5161ec &lt;mad_timer_zero&gt;</td>
</tr>
<tr>
<td>mad_author</td>
<td>const char [48]</td>
<td>[...]</td>
<td>0x516294 &lt;mad_author&gt;</td>
</tr>
</tbody>
</table>
Register Bitfield Viewing and Update

- Bit Fields Display and Update
  - CPU registers
  - SoC registers

- CPU registers

- Benefits
  - Bit fields can be modified at runtime
  - Description of Bit fields can be shown
  - Good for debugging and programming
### General Exception Handling

- It helps user to catch the root cause with ease
  - No need to modify the source code

#### IDE debug configurations setting:

<table>
<thead>
<tr>
<th>Arguments</th>
<th>Debugger</th>
<th>Tracer</th>
<th>Advanced</th>
<th>Source</th>
<th>Common</th>
<th>Exception Handling</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Hardware Stack Recording</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Break on General Exceptions</td>
</tr>
</tbody>
</table>

- Hardware stack protection
- S-mode Environment Call
- ACE disabled exception
- Illegal instruction
- Load Access Fault

- Software Breakpoint
- H-mode Environment Call
- Instruction Access Misaligned
- Non-Maskable Interrupt
- Store Access Misaligned

- U-mode Environment Call
- M-mode Environment Call
- Instruction Access Fault
- Load Access Misaligned
- Store Access Fault

- When general exception is raised, it will pop up an error

![General Exception](image_url)
Script-Based RTOS Awareness

- Provide RTOS information to help debugging
- Display contents controlled by a Python script

### Task List

<table>
<thead>
<tr>
<th>task name</th>
<th>number</th>
<th>priority</th>
<th>start of stack</th>
<th>top of stack</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;IDLE&quot;</td>
<td>3</td>
<td>0</td>
<td>0x208438 &lt;uxIdleTaskStack.2447&gt;</td>
<td>0x208af0 ...</td>
<td>Running</td>
</tr>
<tr>
<td>&quot;Task 2&quot;</td>
<td>2</td>
<td>2</td>
<td>0x200cf8 &lt;ucHeap+2272&gt;</td>
<td>0x2013d0 ...</td>
<td>Delayed</td>
</tr>
<tr>
<td>&quot;Task 1&quot;</td>
<td>1</td>
<td>1</td>
<td>0x200b08 ...</td>
<td>0x200b08 ...</td>
<td>Delayed</td>
</tr>
</tbody>
</table>

Click to show register list

### Event List

<table>
<thead>
<tr>
<th>queue name</th>
<th>handler address</th>
<th>max length</th>
<th>item size</th>
<th>messages waiting</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;TmrQ&quot;</td>
<td>0x200378</td>
<td>5</td>
<td>32</td>
<td>0</td>
</tr>
</tbody>
</table>

Click to show register list
Static Stack Analysis View

- Sizes estimated statically after project is built
- Report the maximum stack size of the whole program
- Display information of stack usage for each function

The maximum amount of stack used by the function’s callees
The amount of stack used for the current function
The amount of stack used before the current function is called
StackSafe™ Protection Handling

- **Record mode**
  - Track the maximum usage of stack pointer

- **Protection mode**
  - Raise an exception if over the allowed limit
Custom UI

- Customize the layout of the Menu and Toolbar items to meet your needs
  - Customize perspective
  - Manage custom UI
- Change menu & toolbar visibility
Multicore Development Support

- Develop the multicore software by simply creating multicore projects with separate build and debug configurations

- Create multicore project
  - Create multicore project
  - Build & debug project

- Separate build & debug configurations
  - Available build configurations for the multi-core project

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Multicore Debug
Cache Dump View

- Easily monitor CPU caches when program suspends
AndeSight Updater

- Friendly and easy-to-use update interface
  - Check update
  - Installing update packages
  - Notification wizard
  - Select the desired packages
AndeSoft™ BSP
Bare Metal, RTOS, Linux and DSP ISA
## AndeSoft™: Application Building Blocks

### Fundamental
- Compiler and toolchain are contributed to and supported officially by GNU and LLVM communities
- Optimized **MCUlib**, newlib, glibc and **DSPlib**
- Concise linker script and its tools, **Linker Scattering-and-Gathering (LdSaG)**
- **Sample programs** to demo AndesCore™ features

### Real-Time Operating Systems
- **Open source**: Zephyr, FreeRTOS
- **Commercial**: ThreadX, LiteOS, RT-Thread, SylixOS
- **RISC-V ready**: VxWorks, μC/OS-[II/III], MyNewt, embOS, RTEMS, NuttX, seL4, uC3/Compact, AliOS Things

### Linux, Middleware and SW Framework
- **Linux kernel** since 4.17, device drivers and advanced features: **strace**, ftrace, Perf, SMU, power throttling, **suspend to RAM** and **kernel module**
- **U-Boot** and BBL
- **Andes6**: connect LPWAN to IPv6 seamlessly
AndeSoft™: Bare Metal

- **Rich startup demo** projects for Andes-specific features

<table>
<thead>
<tr>
<th>Categories</th>
<th>Startup demo</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt</td>
<td>PLIC, CLIC</td>
</tr>
<tr>
<td>Memory</td>
<td>MMU, PMP, cache, cache lock, ECC, bus matrix slave port</td>
</tr>
<tr>
<td>Power Management</td>
<td>PowerBrake, hibernate, WFI CPU standby/resume</td>
</tr>
<tr>
<td>Programming</td>
<td>DSP, printf UART redirect, C++ programming</td>
</tr>
<tr>
<td>Misc</td>
<td>StackSafe™, performance monitor, SMP</td>
</tr>
</tbody>
</table>

- **AMSI (Andes MCU Software Interface) driver APIs**
  - UART, GPIO, RTC, PWM, SPI, I2C, WDT and DMA
Arduino Development

- Support Arduino language reference APIs
- Support Arduino standard libraries
- AndeSight™ IDE Arduino software development plugin

AndeShape™ Corvette-F1

<table>
<thead>
<tr>
<th>Chip Profile Name</th>
<th>Chip ID</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corvette-F1-AE100-N650</td>
<td>Corvette-F1-AE100-N650</td>
<td>[N650]</td>
</tr>
<tr>
<td>Corvette-F1-AE210P-D1088-FPU</td>
<td>Corvette-F1-AE210P-D1088-FPU</td>
<td>[D1088-FPU]</td>
</tr>
<tr>
<td>Corvette-M1</td>
<td>Corvette-M1</td>
<td>[N801-S]</td>
</tr>
</tbody>
</table>
AndeSoft™: RTOS

- A market-leading real-time operating system (RTOS) for MCU
- Scalable size, with memory footprint as low as 9KB
- Tick-less idle
  - Power-saving by stopping periodic tick interrupt in the idle mode, supported by standard RISC-V architecture
- AWS FreeRTOS Qualified
- FreeRTOS test suite verified
- RTOS-awareness debugging
AndeSoft™: RTOS

- An OS that runs best on MCUs for wearable and IoT devices
- Very small memory footprint (will run in 8k)
- Highly configurable, highly modular
- Apache 2.0 license, hosted by Linux Foundation

- Pre-certified by TUV and UL to many safety standards
  - IEC-61508 SIL 4, IEC-62304 SW Safety Class C, ISO 26262 ASIL D and EN 50128
- EAL4+ Common Criteria security certification
- Small footprint, as 2KB instruction area and 1KB of RAM

- Support 32-bit/64-bit version, multicore (AMP & SMP) and MMU
- Large-scale middleware such as Qt, CODESYS, Python, Java Script and POSIX API
- Functional safety certified for rail transport, medical, industrial automation, automotive, electric power and aerospace
AndeSoft™: RTOS

- A Lightweight IoT Operating System that Makes Everything Around Us Smart
- Ultra-small kernel, basic kernel size of less than 10 KB
- Low power consumption
- One-stop software platform, lowering development requirements and improving development efficiency
- Open Source under a BSD 3-Clause license

RT-Thread

- An open source IoT operating system under the Apache 2.0 license
- Abundant software components such as GUI, TCP/IP stack, file system and standard API support like POSIX, CMSIS, C++ runtime, Javascript
- Device and cloud integration design, easy to connect various IoT devices with cloud
AndesSoft™: Linux

- **Linux Kernel**
  - LTS RV32/RV64 port, since 4.17
  - SMP support
  - Cache coherence and cache non-coherence support
  - Linux Test Projects (LTP) verified
  - Device drivers for AE350 platform

- **U-Boot**
  - RV32/RV64 port, maintainer and contributor
  - SMP support
  - Supervisor mode support
  - Device drivers for AE350 platform

- **BBL**
AndeSoft™: Linux

- **Linux Distribution and Build System**
  - fedora
  - yocto
  - OpenWrt
  - BuildRoot

- **Linux Kernel Tools**
  - `strace`/ `ftrace` for developers to debug
  - `Perf` to evaluate the bottleneck of the whole system
  - **System Management Unit (SMU)**
    - Suspend-to-RAM: suspended by sysfs and wakeup by RTC and UART interrupt
    - PowerBrake: power throttling mechanism controlled by sysfs
  - **Kernel module** support all relocation types for RV32 and RV64

- **Andes GitLab Service for Linux Development Packages**

*: available upon request

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Qemu

- Support AndeStar™ RISC-V V5 32/64 bits CPU
- Support AE350 SoC platform
- Integrated with AndeSight™ IDE
- Early software development and verification
  - Run U-Boot and Linux with LTP
  - Run FreeRTOS with software applications
  - Used by HPE and openSUSE project for UEFI EDKII
  - Used by Red Hat for Fedora RISC-V port regression farm
DSP Support

- **DSP ISA assembly programming**
  - Derived and evolved from real use cases over decades
    - Support 32 bits and 64 bits
    - Support saturation and rounding
    - Cover SIMD, partial SIMD, bit manipulation and etc.

- **DSP intrinsic functions**
  - As C-like functions without bothering to program in assembly

- **DSP library**
  - >200 functions in 8 categories (basic, complex, controller, filtering, matrix, statistics, transform and utils)

- **Some source patterns are recognized by compiler, then DSP instructions are auto-generated to facilitate development**

- **Compatible with CMSIS-DSP library API**
  - By including an API wrapper header file

1.84

MP3 decode (compiler auto-gen)
IAR Embedded Workbench for RISC-V

- Complete build and debug toolchain for RISC-V
- Support all series of Andes RISC-V CPU

IAR Embedded Workbench

IDE
- Embedded Workbench

Debugger
- I-Jet ICE
- C-SPY tool

Toolchain
- Compiler
- C-STAT
- Functional Safety

Options for node "123"

Library Options 2
- Stack/Heap
- MISRA-C:2004
- MISRA-C:1998

Target
- Library Configuration
- Library Options 1

Device
- Andes A25 AE350 Orca
- Andes D25 AE150 Orca
- Andes N22 AE250 Corvette-F1
- Andes N22 RV32E AE250 Corvette-F1
- Andes N25 AE250 Corvette-F1
- Andes N25 AE250 Corvette-F1
- Andes N25 AE350 Orca
- Andes N25F AE250 Orca
- Andes N25F AE250 Corvette-F1
- Andes N25F AE350 Orca

IAR Information Center for RISC-V

Product explorer
- Discover how to use basic and advanced product features
- Complete product documentation in PDF format
- All the user and reference information

User guides
- Quick reference
- Release notes
- My pages

Example projects
- Embedded applications
- Software libraries

Integrated solutions
- Andes VIS Toolset
- Andes VIS and middleware solutions

Support
- Andes EAO
- Andes VIS

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Summary

- **AndeSight™ IDE**: Rich features to speed up SW development
  - Ease of use to reduce development time

- **AndeSoft™ BSP**: Well-integrated building blocks to help users to build SoC software quickly and easily
  - Highly-optimized toolchains for better performance and smaller memory footprint

- **Andes Comprehensive RISC-V SW solutions** to achieve fast time-to-market and high quality
  - Supporting 5 Bn+ SoC
Thank you!
See you next Webinar