Andes RISC-V Processor IP Solutions

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Who We Are

- **CPU**: Pure-play CPU IP Vendor
- **15-year-old Public Company**
- **Major Open-Source Contributor/Maintainer**
- **RISC-V Founding Premier Member**
- **RISC-V Ambassador**
  - Running Task Groups
  - TSC Vice Chair
  - Director of the Board

Quick Facts

- **100+ years**: CPU Experience in Silicon Valley
- **80%**: R&D
- **200+**: Licensees
- **17K+**: AndeSight IDE installations
- **6B+**: Total shipment of Andes-Embedded™ SoC

Taking RISC-V® Mainstream
**Examples of AndesCore™ in SoC**

**Renesas: ASSP MCU with configurable V5 cores**
- Scalable/configurable performance
- Selectable safety features
- Customization options
- Feature-rich AndeSight IDE

**Picocom: 5G Open RAN small cells**

![Bus Matrix (16xN)]

**Telink: IoT and Wireless Audio with D25F embedded**
- Strong integer/DSP performance
- Efficient small data processing
- Good development tools

**AI Accelerators for Servers with >10 NX27V Cores**
- RVV with 512-bit VLEN/SIMD
- Custom instructions
- LLVM compiler

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Taking RISC-V® Mainstream
## Andes V5 Processor Lineup

<table>
<thead>
<tr>
<th>Application Processing with Multicore &amp; SMP Linux</th>
<th>AX25MP</th>
<th>AX45MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>A25MP</td>
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<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Application Processing with Single-core &amp; Linux</th>
<th>AX25</th>
<th>AX27/AX27L2</th>
<th>AX45</th>
</tr>
</thead>
<tbody>
<tr>
<td>A25</td>
<td>A27/A27L2</td>
<td>A45</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Data Processing with DSP or Vector</th>
<th>D25F</th>
<th>NX27V</th>
<th>D45</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Embedded Control with Integrated FPU</th>
<th>NX25F</th>
<th>NX45</th>
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<tr>
<td>N25F</td>
<td>N45</td>
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</table>

**25-Series:** 8-stage: 1.1 GHz  
**27-Series:** 8-stage: 1.2 GHz  
**45-Series:** 8-stage: 1.2 GHz

**N22 2-stage (700 MHz)**

### Notes:
1. Core naming: with “X” is 64-bit (e.g. NX25F) and no “X” is 32-bit (e.g. N25F)
2. V5’s common features include RV-IMACN, Caches, LM, ECC/parity, Branch Prediction, CoDense™, PowerBrake, StackSafe™, ACE (Andes Custom Extension™); Frequencies is the worst case at 28nm.
A27L2/AX27L2 Overview

- A27/AX27 + L2$ controller
- AndeStar™ V5 base for “A” cores
  - RV*GCN + P
  - MMU support
  - Andes V5 extensions
- 5-stage single-issue cores
- Programmable PMP/PMA
- MemBoost for L1 caches
  - Skip unnecessary writes to dcache
  - Multiple outstanding data accesses
  - I/D cache prefetch
A27L2/AX27L2: L2$ Controller

**Features:**
- Size up to 2MB with 64B lines
- 16-way, pseudo-random replacement
- 2 tag&data banks with bank interleaving
  - Programmable SRAM latencies (setup & delay)
- Prefetching based on access types (I or D)
- 128-bit AXI master/slave ports through BIU
- Optional ECC error protection

**Performance with 512KB L2 cache:**
- Comparing AX27L2 and AX27
  - Memory bandwidth: 2.1x
  - Memory latency: 30%
  - Specint2k: 1.9x
45-Series: Features

- AndeStar™ V5 architecture:
  - Base: RV*GCN + Andes V5 extensions
  - N45/NX45: base
  - D45: base + P
  - A45/AX45: base + P + MMU
  - A45MP/AX45MP: base + P + MMU

- 8-stage in-order dual-issue
  - Independent pairs with 1 or 2 ALU insns
  - Most dependent pairs with 2 ALU insns
  - Late ALU for 0-cycle load-use penalty

- Unaligned data accesses
- Low power dynamic branch prediction
- MemBoost memory subsystem

*: depending on cores
45-Series: Features

- **Virtual memory support:**
  - MMU and S-mode
  - All page sizes and virtual memory mappings (SV32/39/48)
  - Shared TLB: 32-512 entries

- **Physical memory support:**
  - Up to 16-entry PMP and PMA

- **L1 I/D Caches:**
  - Size up to 64KB, 64B lines, up to 4-way
  - Cache lock support
  - Optional Parity or ECC error protection

- **I/D Local Memory (ILM/DLM)**
  - 4KB up to 16MB
  - Optional ECC error protection

*: depending on cores
A(X)45MP: Cache-Coherent Multicore

- **Cache coherence scheme**
  - Directory-based for scalability
  - MESI coherence protocol

- **45MP Coherence Manager**
  - Support 1~4 A45/AX45
  - IO coherence for cacheless masters

- **L2$ Controller** (optional)
  - Similar to that of A*27L2

- **Bus Interfaces**
  - Memory and MMIO ports
  - LM slave ports (one per core)
  - Coherence slave port

- **PLIC** for global interrupt handling

- **Debug/trace** support

- **Linux SMP** ready
45-Series: Performance

- Total compute performance (at 28nm):

<table>
<thead>
<tr>
<th>Coremark®</th>
<th>45-series (1.2 GHz)</th>
<th>27-series (1.1 GHz)</th>
<th>Speedup (Per-MHz)</th>
<th>Speedup (Total Perf.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RV32</td>
<td>5.66</td>
<td>3.58</td>
<td>1.58</td>
<td>1.72</td>
</tr>
<tr>
<td>RV64</td>
<td>5.50</td>
<td>3.53</td>
<td>1.56</td>
<td>1.70</td>
</tr>
</tbody>
</table>

- 70% higher than the 27-series
- With less than 50% increase in logic area and power

- Memory bandwidth (C copy): 45-series is 35% higher than 27-series
- Running up to 2.4 GHz at 12nm
Andes Solutions for Data Path Acceleration

- RVV extension (Vector)
  - Scalable vector registers
  - For high data rate computations
- RVP extension (DSP/SIMD)
  - Integer/fixed-point on already existing GPR
  - For audio/voice, small image, slow video
- Andes Custom Extension™ (ACE)

**Inputs:** Attributes C code Verilog

**COPILLOT Tools**
(Custom-OPtimized Instruction deveLOpment Tools)

**ACE Framework**

**ISS:**
- AndeSim near-cycle accurate simulator
- Imperas fast simulator

**Extensible Base Components**
**NX27V: Overview**

- **AndeStar V5 architecture:**
  - RV64GCN+ Andes V5 extensions
  - **Vector ext. (RVV) 1.0:** latest spec

- **An efficient 5-stage scalar unit**
  - Optional branch prediction
  - **FP16 instructions**

- **I/D caches**
  - Caches: 8KB to 64KB
  - HW unaligned load/store accesses
  - Optional parity or ECC protection
  - I$/D$ prefetch
  - Multiple outstanding data accesses
    - Cached and uncached
NX27V: Overview

- RVV data formats:
  - Standard: int8~int64, fp16~fp64
  - Andes-extended: bfloat16 and int4

- A powerful Vector Unit (VPU):
  - RVV starts execution after retired
  - Multiple Functional Units
    - Operating in parallel and out of order
    - Chainable, and most fully pipelined
  - VLEN & SIMD width: 128, 256, 512

- Independent memory access paths:
  - RVV load/store thru dcache and system bus
  - ACE load/store thru Streaming Port
Taking RISC-V® Mainstream

**NX27V: ACE Streaming Port**

- **A usage example**
  - HW engine: application-specific DMA and structured computations (e.g. CNN)
  - ACE instructions: control HW engine, and load/store data to/from VRF

- **Advantages:**
  - HW engine is tightly-coupled
  - Data accesses are more efficient (such as address auto-increment and wrap-around)

```c
insn svload {
  operand= {out vr data, io addrCtl addr, imm2 mode, ...}
};

csr_op= {vl};
streaming_port= load;
csim= ... ...
};
```
ACE for Custom Vector Instructions

- RVV is very powerful, but it cannot satisfy everyone.
- ACE makes custom vector instruction possible:
  ```
  rvv insn dotp {
    operands= {out vrf rslt, in vrf vec1, in xrf vec2};
    input_format= ...; // (quad) widening/narrowing
    csim= ... //Instruction semantics in C
    ... //RTL implementation in concise Verilog
  }
  ```
- Designers only need to focus on ELEN-level instruction semantics
- COPILLOT auto-generates supports for:
  - SW: compiler, debugger, simulator
  - RTL: decoding, formatting, dependence checking, chaining, and more
  - RVV control-aware (LMUL, SEW, vl)
Scalable Acceleration Architecture

- Domain-specific acceleration

- Separate control from acceleration to optimize them independently

- Programming support: OpenCL
  - Popular for heterogeneous multicore architecture with host and devices
  - Support RVV intrinsic programming in addition to auto-vectorization
AndeSentry™ Security Framework

- An open framework for a wide spectrum of threat mitigations
  - From cyber attacks to physical attacks
  - Flexible, scalable, and trustable
  - Solutions from Andes and partners

- Scope:
  - TEE, crypto acceleration, protection against cyber attacks, countermeasures for physical attacks
  - Hardware and software
Thank You!!