Andes RISC-V CPU IP Provides Synergism for TSMC Process Portfolio

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Why RISC-V?

- **Open source ISA**
  - Simple, Clean-Slate
  - Modular design
- **Extensibility/Specialization**
  - Engineer could add own instruction sets
  - Engineer could propose design features to Foundation Task Force

Why RISC-V? - 2


Berkeley Architecture Research
NXP
antmicro
EMBEDDED SYSTEMS
SANECHIPS
中兴微电子
Western Digital.
NVIDIA.
Micron
bluespec
ORION
猎户星空
SAMSUNG
Google
QUALCOMM
Microsemi
a MICROCHIP company
cortus
C-SKY
中天微
SiFive
Rambus
RISC-V
Foundation: > 235 members
ESPRESSIF
MEDIATEK
QuickLogic
ANDES TECHNOLOGY
galois
imperas
runtime.io
GLOBALFOUNDRIES
BAE SYSTEMS
Esperanto Technologies
REM
inside secure
Hortonworks
सी डैक CDAC
ETH zürich
oculus
Symbiotic EDA
NUS
VeriSilicon
OpenSingularity
INTRINSIC ID
TRINAMIC
SECURE RF
Barcelona Supercomputing Center
UBILITE
SIEMENS
LAUTERBACH
HITACHI Inspire the Next
Minima
MIT CSAIL
DELPHIN INTEGRATION
IBM
GOWIN
Mentor
ASHLING
EMBECOSM
FORTH
INTRINSIX
TESLA
NORTHROP GRUMMAN
CEVA
优矽科技 UC TECH IP
MINRES
SoundAI
SK hynix
DATA 61
DOVER MICROSYSTEMS
GRAY RESEARCH
tsmc
HEX-Five Security
CMC
cadence
GREENWAVES
IAR SYSTEMS
XtremeEDA
ultraSoC
Syntacore
DRAPER
ICT
VectorBlox
TESLA
SEAGATE
aselsan
IDT
Technolution
Rumble Development
RISC-V Foundation
Roa Logic
SHC
SH CONSULTING
Mellanox TECHNOLOGIES
lowRISC
IBM
SEGGER
codasip
PRINCETON

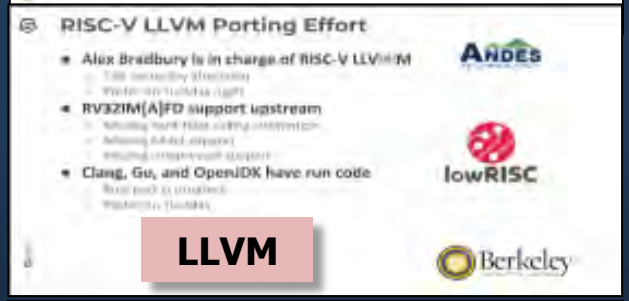
Why Andes - 1: Best RISC-V Extensions

- **Bring Andes strength to RISC-V Core family**
  - Architecture beyond the kernel for diversified requirements
  - Efficient processor pipeline for leading PPA
  - Platform IP support to help speed up SoC construction
  - AndeSight IDE, and compiler/library optimizations
  - RTOS and Linux support, and middleware (such as IoT stacks)
  - Commercial-grade verification for all products
  - Mass production experience with high quality deliverables
  - Professional supporting infrastructure
- **Best Extension AndeStar V5: RISC-V + Andes Extensions**

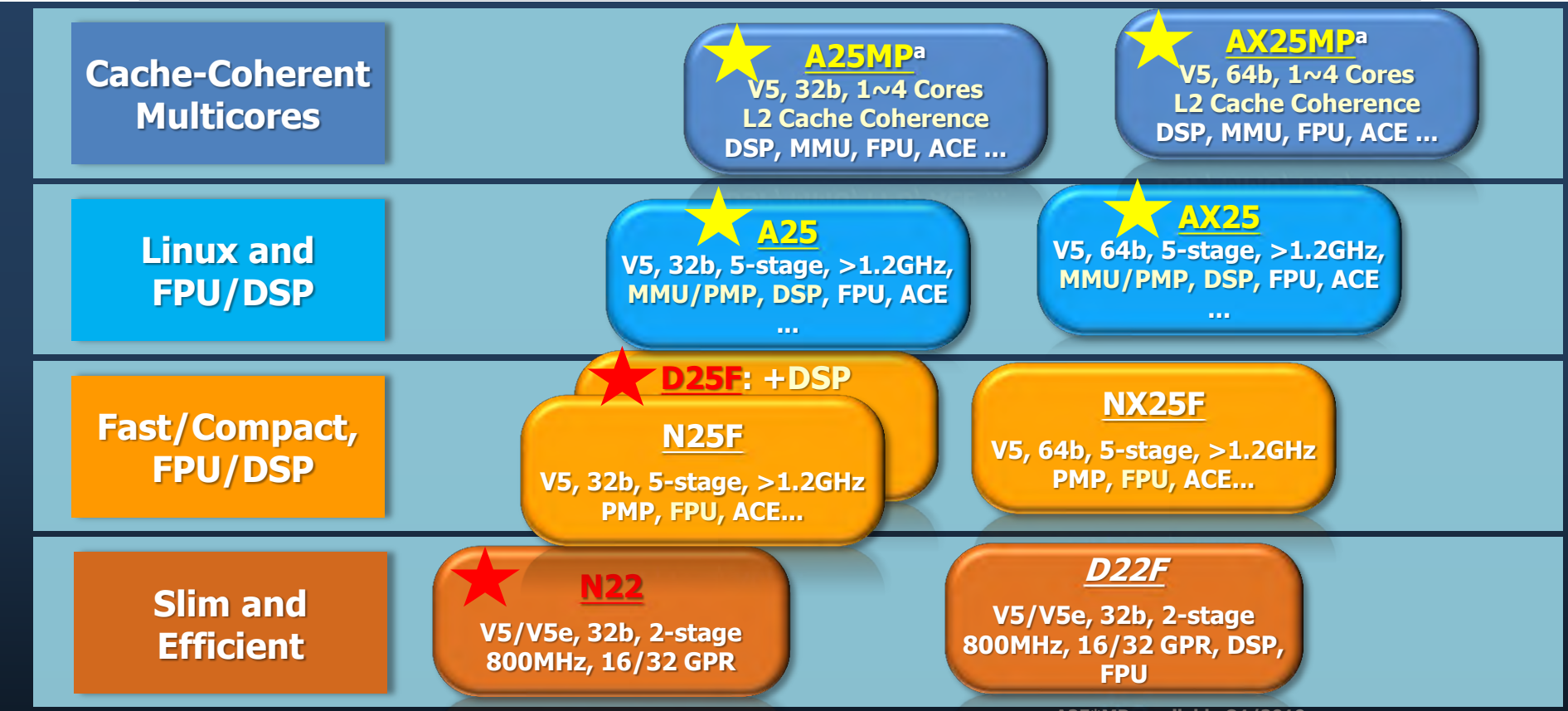
Why Andes - 2

- **14-year-old public CPU IP excellent track record**
- **>1B Andes-Embedded SoC shipped in 2018. >3.5B cumulatively.**

- **A founding member of the RISC-V Foundation**
- **A leading open source maintainer/contributor**
- **Technology leader in RISC-V extensions**
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group



Launch or Upgrade of RISC-V Core IP Series



a. A25*MP: available Q1/2019
b. 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

D25F

- **Designed >150 DSP ISA in the popular Andes V3 cores D10/D15**
- **Donated them as the basis of the P-extension draft for RISC-V**
- **Details:**
  - Use RV32 and RV64 XLEN-bit **GPRs**. (i.e. no additional registers)
  - Support saturation and rounding.
  - Support fixed-point and integer data types.
  - **SIMD**-instructions with 8b, 16b, 32b element size.
  - Complex DSP instructions operating on 16-bit, 32-bit and 64-bit data.
  - Min, Max, Shift, Byte swap, Bit reverse, Pack, Unpack… operations.
  - 64-bit signed/unsigned addition & subtraction
  - 64-bit signed/unsigned multiplication & addition
    - E.g., 64 = 64 + 16x16 + 16x16 or
    - E.g., 64 = 64 + 32x32

Speedup with P-Ext on 25-Series

- **RV32-P for DSP libraries** (>200 functions in 8 categories)

Speedup	Basic	Cmplx	Ctlr	Filter	Matrix	Ststcs	Xform	Utils	ALL
AVG	2.40	1.62	1.84	2.26	1.62	2.44	1.29	1.08	**1.82**
MAX	5.16	4.09	2.13	4.11	2.75	4.39	1.78	1.43	**5.16**

- **RV64-P for DSP libraries** (>200 functions in 8 categories)

Speedup	Basic	Cmplx	Ctlr	Filter	Matrix	Ststcs	Xform	Utils	ALL
AVG	4.73	1.92	1.31	2.41	3.04	4.14	1.28	1.19	**2.50**
MAX	10.81	4.14	1.59	5.04	6.83	8.51	1.67	2.72	**10.81**

- **Speedups for various applications**

Cores	RV64-P		RV32-P	
APP	CIFAR10 (image classification)	PNET (90% of face detection)	AMR voice codec	MP3 decode
Speedup	**10.99**	**7.57**	**3.67**	**1.84**

More Cores featuring SIMD DSP: A25, AX25

Features	A25	AX25
P-Extension	Yes	Yes
32KB I$/D$ + 256 BTB	Yes	Yes
SP/DP FPU	Yes	Yes
MMU and S-Mode	Yes	Yes
Worst-Case Max. Freq. (GHz)[1]	1.2	1.2
Coremark/MHz[2]	3.58 (rv32), 3.52 (rv64)	
DMIPS/MHz (ground rule)[2]	1.96 (rv32), 2.09 (rv64)	

1: TSMC 28HPC+ RVT 9T library and high-speed memory. Frequency condition: 0.81v/-40°c.
2: BSP V5.0.0 toolchain; DMIPS/ground rule uses no-inline option.

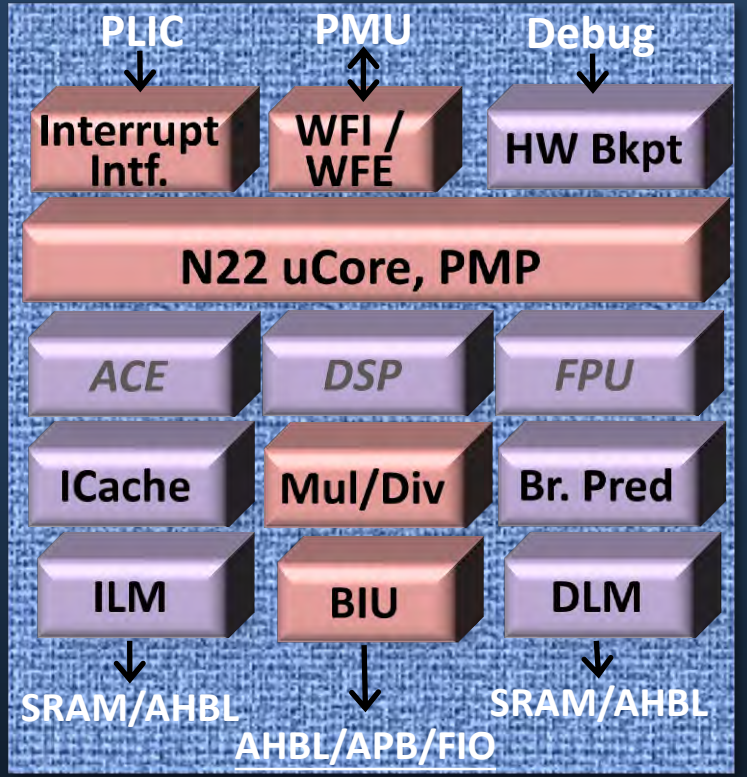
And A25MP, AX25MP too…

7nm Example:
N25F/NX25F PPA with TSMC 7nm Library

- Processor configuration: 8 PMP entries, Performance monitors, 64b wide AXI bus, Dynamic branch prediction with 256 entry BTB, 32KB I and D caches, Debug support with 4 HW breakpoints and instruction trace
- Process & library: 7nm FinFET (TSMC 7nm, CMOS LOGIC Fin FET ELK Cu, 1P18M, HKMG, 0.75/1.8V)
- Power/Performance/Area Analysis -
- For NX25F:
  Frequency(worst case): 1472MHz
  Gatecount: 340Kgates
  Digital Area with Scan: 0.0267mm^2
  Dynamic Power: 10.64uW/MHz
  Static Power: 1.53uW
  DMIPS/MHz: 2.87
  Coremark/MHz: 3.44
- For N25F:
  Frequency(worst case): 1483MHz
  Gatecount: 250Kgates
  Digital Area with Scan: 0.0198mm^2
  Dynamic Power: 8.87uW/MHz
  Static Power: 1.10uW
  DMIPS/MHz: 2.56
  Coremark/MHz: 3.48

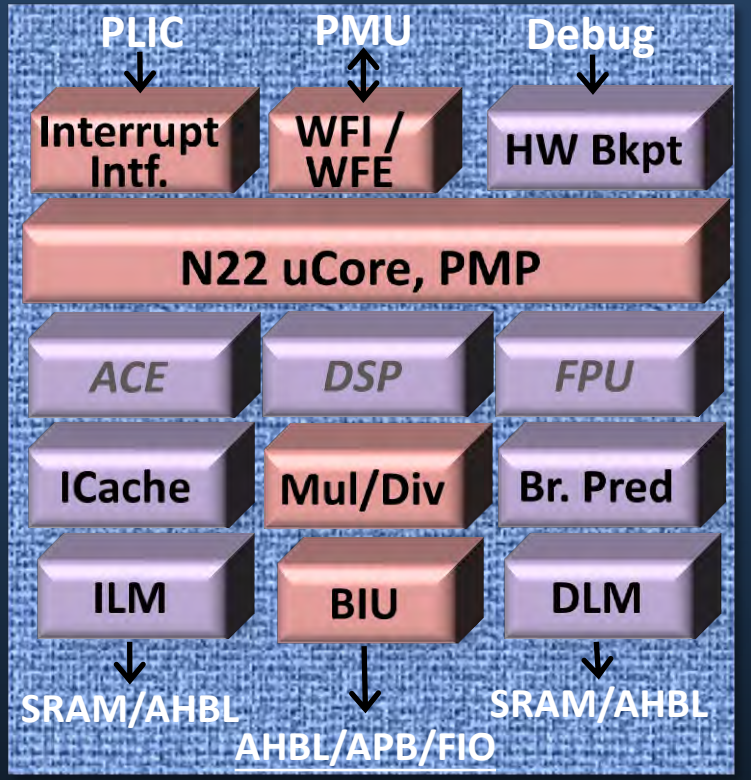
N22

- **AndeStar V5 or V5e ISA**
  - Based on RV32-IMC or RV32-EMC
- **2-stage pipeline, single-issue**
- **AHB-lite system bus**
- **WFI/WFE**
- **Rich baseline options:**
  - PMP: up to 16 entries
  - M-mode, or M+U-mode
  - Multiplier: fast or small (1 or 17 cycles)
  - Branch prediction: static or dynamic
  - I/D Local Memory: 1KB to 512MB
  - I Cache: 1KB to 32KB; direct-map or 2-way
  - HW-handled misaligned load/store



N22

- **Rich baseline options: (cont.)**
  - Core-Local Interrupt Controller (CLIC)
    - >1000 sources, 255 priority levels
    - Selective vectoring with priority preemption
    - Efficient SW-based tail chaining
  - Platform-Level Interrupt Controller (PLIC)
    - For multiple cores
    - >1000 sources, 255 priorities levels
  - **Additional buses**:
    - Fast IO port with 1-cycle latency
    - APB private peripheral port
  - **JTAG debug module**
    - up to 8 triggers (breakpoints/watchpoints)
    - 2-wire or 4-wire support



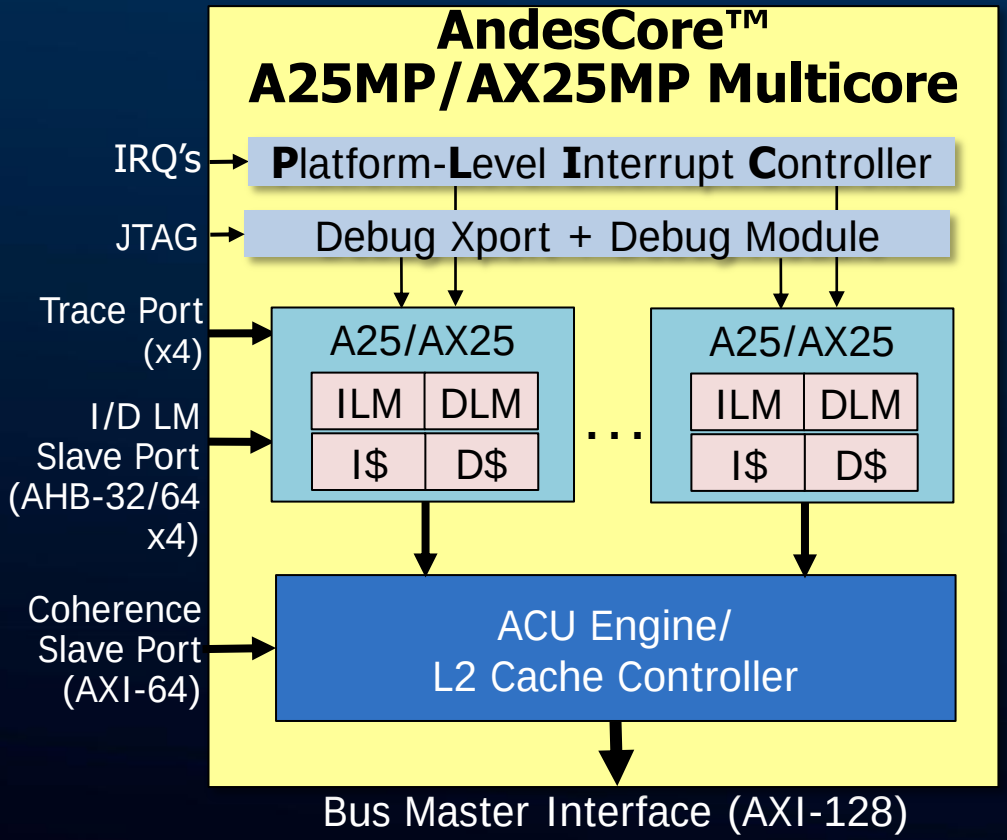
N22 Performance

At TSMC 28nm

- Highest frequency: 700MHz (worst case condition)
- Minimal gate count: <15K gates
- Best scores: 3.97 Coremark/MHz, 1.80 DMIPS/MHz (no-inline)

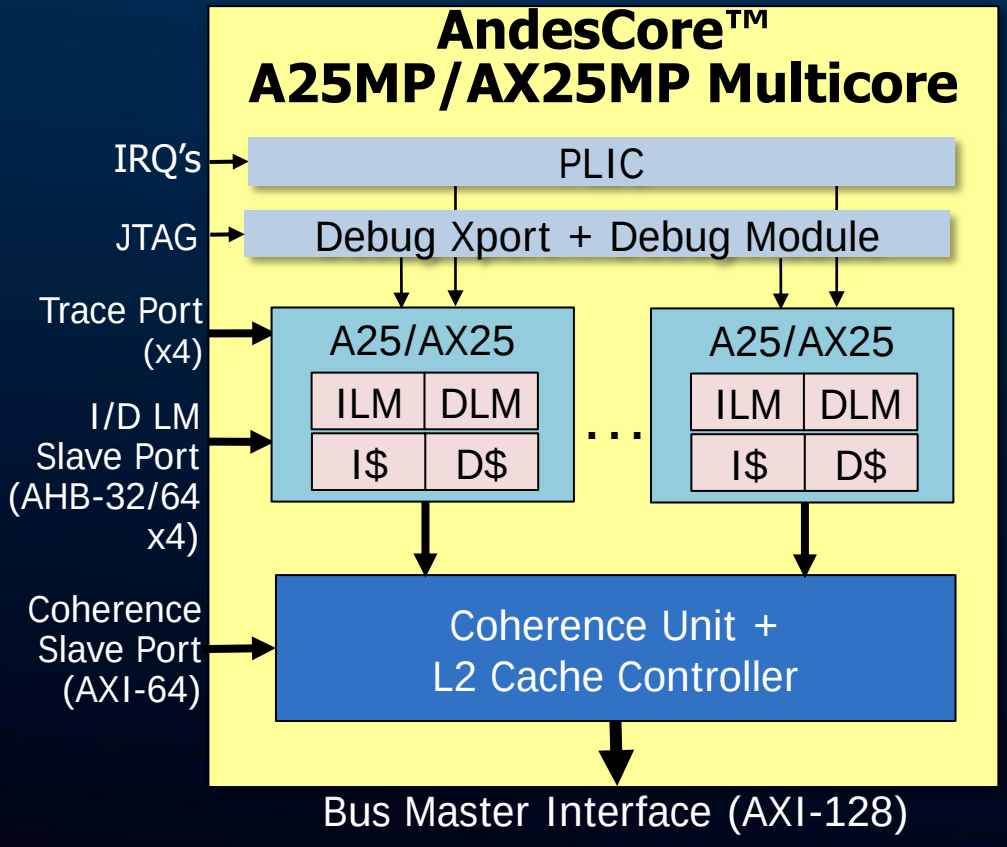
CPU Cores	M3	**N22 (same seg config)**	M0+	**N22 (same seg config)**
ISA	ARM V7m	**Andes V5**	ARM V6m	**Andes V5e**
CoreMark/MHz	3.34	**3.97 (+19%)**	2.46	**3.11 (+26%)**
DMIPS/MHz (no-inline)	1.25	**1.80 (+44%)**	0.95	**1.11 (+17%)**
CSiBE Code Size (KB)	1,330	**1,185(-13%)**	1,315	**1,305**

A(X)25MP: Cache-Coherent Multicore



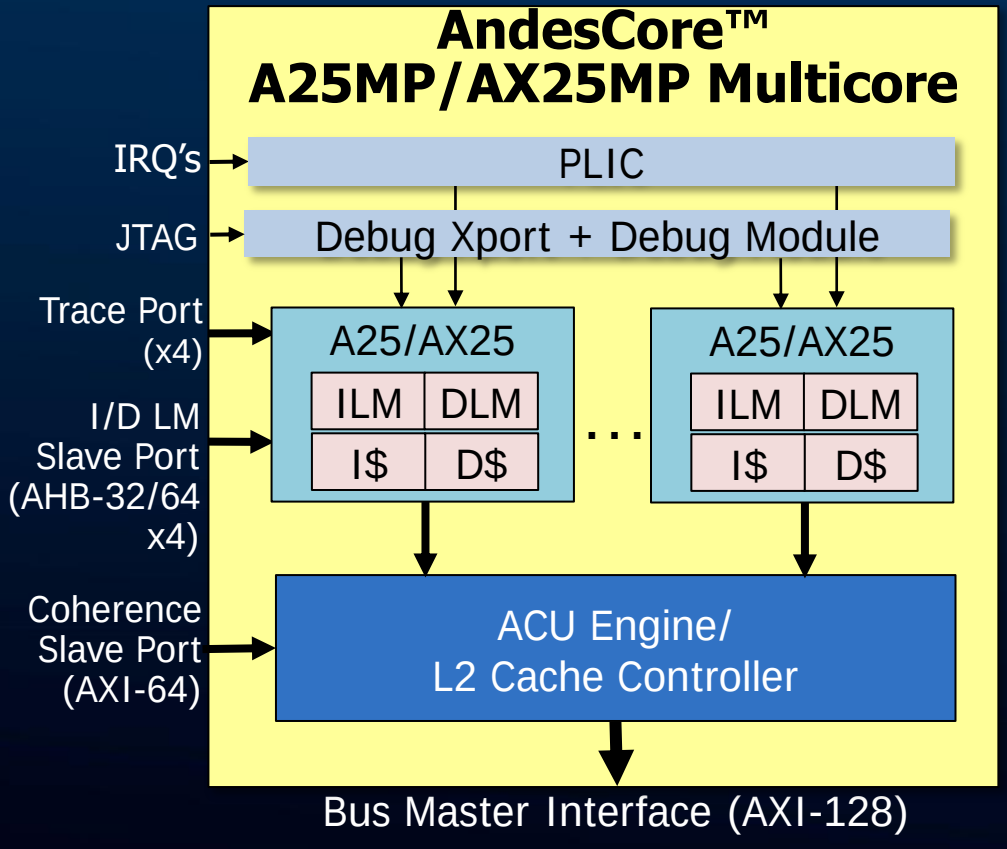
- **1~4 A25/AX25 CPUs:**
  - RV-IMACFD ISA + V5 extensions
  - P-extension draft
  - Supporting SMP Linux
- **Bus Interfaces**
  - LM slave port
  - I/O Coherence slave port
  - Local memory slave port, for each A25/AX25 CPU
  - AXI bus master interface
    - N:1 synchronous clock ratio
- **PLIC (Platform Level Interrupt Controller) for interrupt handling**
- **Debug/trace support**

A(X)25MP: Cache-Coherent Multicore



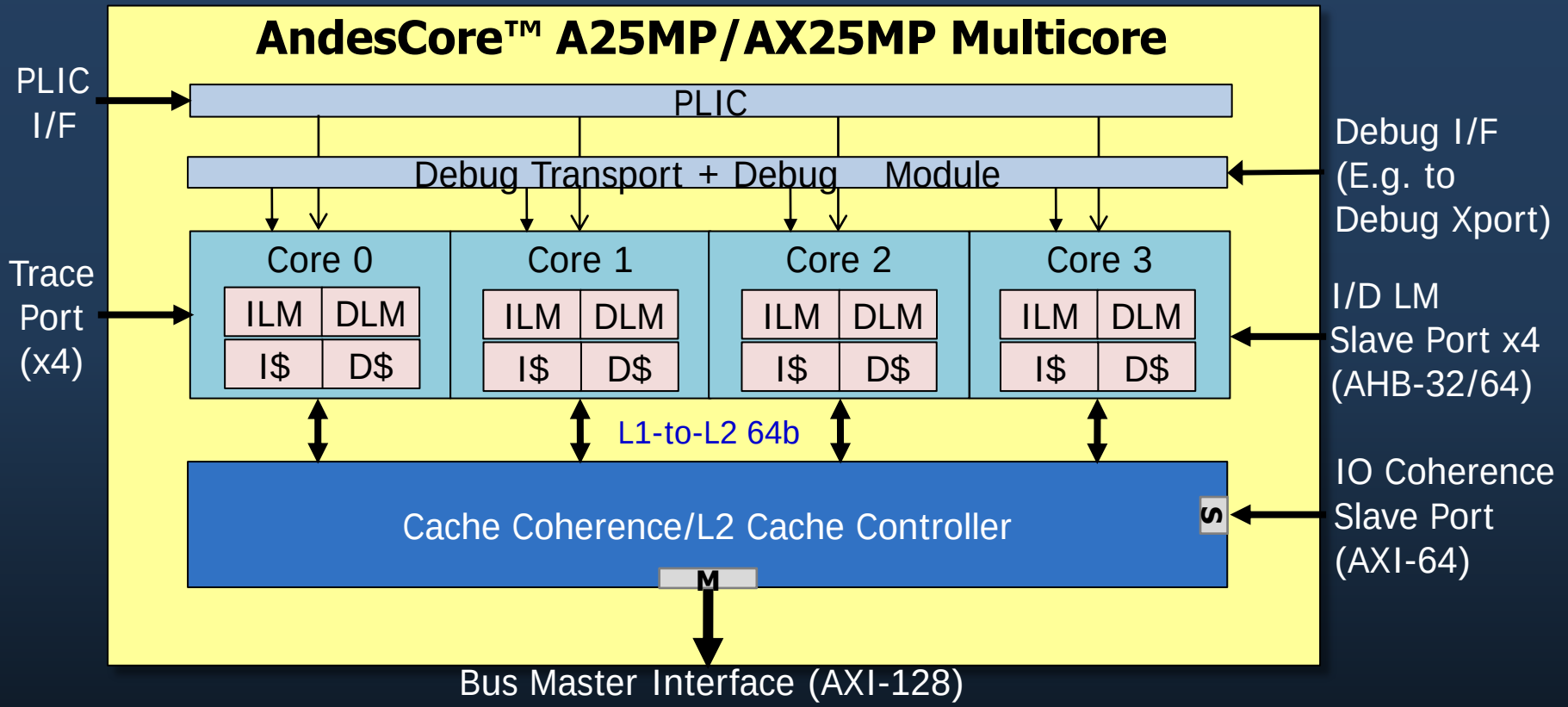
- **ACU Coherence Unit**
  - MESI cache coherence protocol
  - Duplicate L1 dcache tags
  - IO coherence for cacheless masters
- **L2$ Controller (optional)**
  - **Size**: 128KB to 2MB
  - **Line size**: 32B
  - **16-way** with pseudo random replacement and writeback
  - **Tag and data RAMs**
  - SRAM access cycles: ≥ 2 (configurable)
    - Bank interleaving:
      - 2 tag banks, 8 data banks
    - Fully pipelined with interleaving

A(X)25MP: Cache-Coherent Multicore



- **L2$ Controller (cont.)**
  - **Writeback/invalidate control**
  - **ECC protection** (SECDED): same as that for L1 memory
  - **Prefetching**
    - Instruction: 1/2/3 lines after a miss
    - Data: 2/4/8 lines after consecutive linear misses (tracking 8 address sequences)
- **Linux-capable configuration**
  - RV64, 32KB I/D$, 256-entry BTB, 128-entry STLB, 8-entry PMP
  - ~1 GHz at 28nm (worst case)
  - Size (gate count):
    - Core: >200K, ACU+L2: <200K

A(X)25MP: Cache-Coherent Multicore



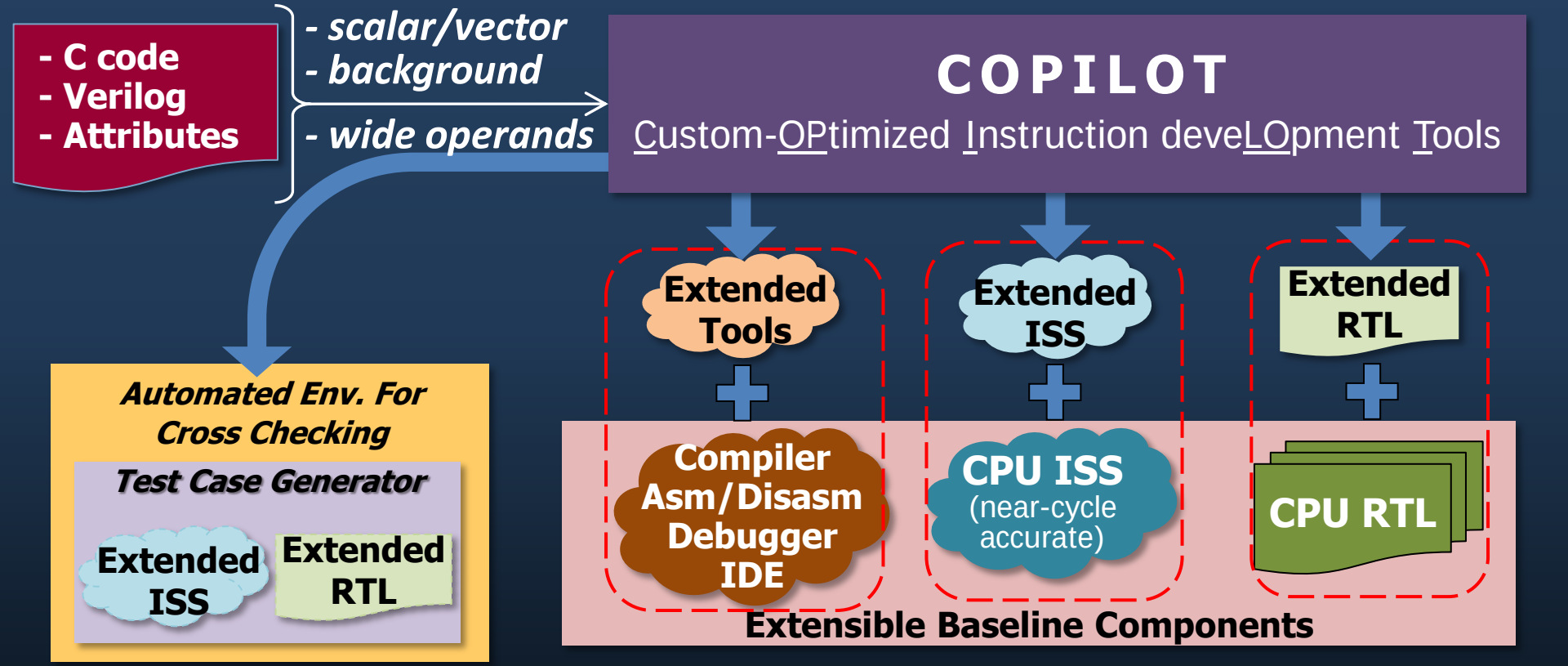
Specific Processors For DSA

- Extensibility in RISC-V enables DSA
- An ideal DSA architecture proposed:
  RISC-V standard+ Andes baseline extensions
  + Andes Custom Extension™ (ACE) for your custom instructions

Benefits of ACE

- **Users focus instruction semantics, not CPU pipeline**
- **Housekeeping tasks are offloaded to COPILOT**
  - ✓ opcode selection and instruction decoding
  - ✓ operand mapping/accesses/updates
  - ✓ dependence checking
  - **➔Adding instructions is similar to ASIC design**
- **Comprehensive support:**
  - ✓ Powerful instruction semantics: vector, background, wide operands
  - ✓ Auto-generation of verification environment, development tools and RTL code
- **SW invokes the instructions by using intrinsic functions**

ACE Framework



RISC-V Processors Introduced Today

Cores	AndeStar™ ISA	GPR bits	Priv. levels	Intr. Ctlr	MMU	I/D$	ECC	FPU	ACE	DSP (P)	MP
N22	V5/V5e	32	M+U	CLIC		I					
N25F	V5 (+RV-FD)	32	M+U	PLIC		I/D	✓	✓	#		
D25F	V5 (+RV-FD)	32	M+U	PLIC		I/D	✓	#	#	✓	
A25	V5 +RV-FD	32	M+U+S	PLIC	✓	I/D	✓	✓	#	✓	
A25MP	V5 +RV-FD	32	M+U+S	PLIC	✓	I/D	✓	✓	#	✓	✓
NX25(F)	V5 (+RV-FD)	64	M+U	PLIC		I/D	✓	#	#		
AX25	V5 +RV-FD	64	M+U+S	PLIC	✓	I/D	✓	✓	#	✓	
AX25MP	V5 +RV-FD	64	M+U+S	PLIC	✓	I/D	✓	✓	#	✓	✓

1. V5: RV*IMAC + Andes Extensions, V5e: RV*EMAC + Andes Extensions
2. Common features: PMP, branch prediction, CoDense™, PowerBrake, StackSafe™
3. ✓: included; #: separately licensable

Concluding Remarks

- **With the RISC-V offering from Andes Technology, every SoC design teams will have synergetic relationship, to take same broad spectrum of process advantage offered by TSMC**
- **ACE enables SoC designers to customize their own CPU instructions in developing ADAS, AI, IoT applications specific designs to boost performance, lower power, increase security leveraging particular TSMC processes**
- **Andes is:**
  - A pure-play processor IP vendor for RISC-V
  - Trusted Computing Expert to help shipping billions of SoC

Committed to be your reliable RISC-V CPU IP provider

Thank you !!

ANDES TECHNOLOGY

Andes RISC-V CPU IP Provide Synergism for TSMC Process Portfolio

Abstract

The central processor unit (CPU) that powers the electronics we take for granted today is undergoing a profound change. This is being brought on by the advent of RISC-V, the first open-source instruction set architecture (ISA). A leading supplier of small, low-power, high performance 32-/64-bit embedded CPU cores based on a proprietary ISA, Andes is a founding member of the RISC-V Foundation and a major champion in the development of this open-sourced ISA. RISC-V will have a synergetic relationship with the major semiconductor foundries, especially TSMC. Consider the product mix for TSMC at 65nm, LP and GP; at 55nm, LP, GP, and HV; at 45NM, LP; 40 LP; at 28nm, HPC, HPM, HPC+, HPL, and LP; and at 16nm FF+ and FFC. Before RISC-V, only the largest chip makers could take advantage of this broad spectrum of process offerings. These major companies could afford the high cost of tailoring a proprietary CPU ISA to make best use of a given process. With the RISC-V offering from Andes Technology, every SoC design team, no matter its company's size, has the same advantage. This is made possible by Andes Custom Extension™ (ACE) that enables SoC designers to create their own CPU instructions to boost performance, lower power, increase security at the chip level, and enable design teams proprietary competitive advantage. This presentation will describe how Andes customers, developing ADAS, AI, IoT applications are using this capability to tailor their designs for particular TSMC processes. One Andes RISC-V core running TSMC 7nm process on nearly 1.5GHz high speed design example will be specified.

Why Andes - 3: Best RISC-V Extensions

AndeStar V5: RISC-V + Andes Extensions

- **Baseline ISA extensions:**
  - Faster memory accesses
  - Faster branches
  - More compact code on top of RV-C
- **Andes Custom Extension™ (ACE) frameworks for DSA**
  - Powerful tools
  - No CPU design experience needed
- **PLIC extension:**
  - Vectored dispatch
  - Priority-based preemption
  - Save >50% of instructions
- **Cache Support:**
  - Management operations (flush, invalidate, etc.) at the line level
  - Uncached accesses
  - Write-back and write-through
- **StackSafe™:** Stack protection mechanism
- **QuickNap™:** Fast power-down/wake-up support for caches
- **PowerBrake:** Digital power throttling