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* Availability of the above function blocks varies on each core

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AndeSight™
Software Developer’s Environment

General Description
AndeSight™ is an Eclipse-based integrated development environment (IDE) which provides an efficient way to develop embedded applications for AndesCore™ based SoCs.

Features
AndeSight™
- Eclipse-based IDE
- Project management
- Managed build system
- Feature-rich editor
- Source level debugger
- Profiling analysis
- In-System programming
- RTOS awareness debugging
- Break and display on exceptions
- Register Bitfield viewing and update
- Multicore development support
- Custom UI
- AndeStar™ V5 CPU support
- Extensive demo projects
- Flexible license control
- Corvette F1 (Arduino-Compatible board) support

Compilation Tools
- Compiler
- Assembler
- Linker

Library
- newlib
- glibc
- mculib

RTOS
- FreeRTOS
- Commercial

Debug/Analysis
- Debugger
- Profiler
- Code Coverage
- Code Size Analysis

Target Systems
- Real Evaluation Platform
- In Circuit Emulator (AICE)
- Virtual Evaluation Platform

AndeSight™ Versions:
STD
A comprehensive IDE with highly-optimized compilers, all GUI features, and Linux support.

RDS
Based on AndeSight™ with additional customization features for customers’ redistribution.

Toolchains
- Compiler for ELF and Linux targets
- Andes efficient ROM patch solution
- Highly optimized DSP library functions
- Highly optimized libc functions

Simulator
- CPU simulator(near-cycle accurate)
- Models of AndeShape™ SoC platform

ICE
- AICE debugger (4-wire/2-wire) with OpenOCD support

Supported Host Platforms
- Windows 7 / Windows 10
- Ubuntu Linux 18.04 / CentOS 7.0/
  Red Hat Linux 7.0
AndeStar™ Architecture

The AndeStar™ V5, the latest generation of Andes architecture, consists of both 32-bit and 64-bit register architectures with mixed-length 16/32-bit instructions. It adopts the RISC-V technology as its subset and benefits from the fast growing RISC-V ecosystem. Together with the merits of performance enhancement extensions inherited from V3, the third generation RISC-style architecture, the AndeStar™ V5 brings compact, modular and customizable advantages to SoC applications. As a founding Premier member of the RISC-V International Association, Andes is determined to take RISC-V to the mainstream.

AndeSoft™

Building Blocks for System - AndeSoft™ Software Components

With AndeSight™ IDE, users can develop software with hardware in a seamlessly integrated environment efficiently. To speed up the development process, Andes further provides a rich set of software components, from Real-Time Operating System, Linux kernel and drivers, libraries, and middleware, to application frameworks, running on AndesCore™ processors under the name AndeSoft™. Users can leverage those well-prepared and verified building blocks based on their needs and focus on tackling products to greatly improve time-to-market.

**Fundamental**

- Compiler and toolchain are contributed to and supported officially by GNU and LLVM communities
- Optimized C libraries: MCUlib, newlib and glibc
- Optimized low-level compute libraries for NN, DSP and vector processing: libnn, libdsp, libvec
- Concise linker script and its tools, Linker Scattering-and-Gathering (LdSaG)
- Bare-metal drivers and demo programs to demo AndesCore™ features
- Virtual platforms: AndeSim™ (near cycle-accurate), AndeSysC™ (SystemC library), Qemu

**Real-Time Operating System**

- Open source port on Andes: Zephyr, FreeRTOS
- Commercial port on Andes: Azure RTOS ThreadX, RT-Thread, SylixOS

**Linux, Middleware and SW Framework**

- Linux kernel since 4.17 and LTS v5.4, device drivers and advanced features: strace, ftrace, Perf, SMU, power throttling, suspend-to-RAM and kernel module
- U-Boot, OpenSBI and BBL
- Andes6: connect LPWAN to IPv6 seamlessly
The AndeShape™ development platform includes a variety of hardware entities, such as pre-platform IPs, ICE debuggers (AICE), and hardware evaluation boards for AndesCore™ processor-based system development. To satisfy the best quality-of-result (QoR) requirements for different system applications, various platform IPs are available with different bus and datapath structures. In addition to a basic set of connectivity and storage devices, the rich set of hardware options in both board and SoC levels enable versatile flexibility in hardware/software co-development and early prototyping.

The comprehensive debugging support, including in-system programming, self-diagnosis, and embedded ICE, greatly reduces the system development cycle while maintaining the quality of design.
About Andes Technology

Andes Technology, a Founding Premier member of RISC-V International and publicly listed CPU IP provider (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099), has been devoting to the development of innovative high-performance/low-power 32/64-bit processors and associated SoC platforms since its foundation in 2005. Its powerful CPU lineup covering entry-level, mid-range, high-end, extensible and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 10 billion SoC shipment containing Andes IP as of 2021. Andes is the first mainstream CPU vendor adopting the open RISC-V. While delivering advanced features based on proprietary ISAs, Andes also provides customized CPU service. For more information about Andes’ products, technologies and services, please visit www.andestech.com or contact us through the following.

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