AndeSysC™
A Flexible RISC-V Processor Model for SoC Virtual Prototyping

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Agenda

- Andes and RISC-V
- Virtual Prototyping
- AndeSysC™
- Virtual SoC Example
Andes and RISC-V

Who We Are

- **CPU**: Pure-play CPU IP Vendor
- **RISC-V Founding Premier Member**
- **Major Open-Source Contributor/Maintainer**
- **16-year-old Public Company**
- **RISC-V Ambassador**
  - Running Task Groups
  - TSC Vice Chair
  - Director of the Board

Quick Facts

- **100+ years** CPU Experience in Silicon Valley
- **80%** R&D
- **200+ Licensees**
- **20K AndeSight IDE installations**
- **7B+ Total shipment of Andes-Embedded™ SoC**
Successful Stories with Andes

Renesas: ASSP MCU with configurable V5 cores
- Scalable/configurable performance
- Selectable safety features
- Customization options
- Feature-rich AndeSight IDE

Picocom: 5G Open RAN small cells
- N25F
- Bus Matrix (16xN)
- Mem
- CSR

Telink: IoT and Wireless Audio with D25F embedded
- Strong integer/DSP performance
- Efficient small data processing
- Good development tools

AI Accelerators for Servers with >10 NX27V Cores
- RVV with 512-bit VLEN/SIMD
- Custom instructions
- LLVM compiler

Andesa: Taking RISC-V® Mainstream
Virtual Prototyping
Virtual Prototyping

- A method in the process of product development
- Using software to validate a design before committing to making a physical prototype
  - Behavior, function and cycle analysis
Benefit of Virtual Prototyping

Enable parallel development of hardware and software
- Enable earlier feedback between HW and SW teams
- Support co-verification of hardware and software
- Make chip re-spins much less likely
- Reduce project time and cost
Electronics System Level (ESL)

- Defined by Gartner Dataquest in 2001
- Methodologies for HW/SW Co-design and Co-verification
- Higher level abstraction above RTL
  - C, C++
  - SystemC/TLM2.0 (IEEE 1666 -2011)
  - UPF 3.0 (IEEE 1801-2015)
  - IP-XACT (IEEE 1685 –2014)
  - and more

“the utilization of appropriate abstractions in order to increase comprehension about a system, and to enhance the probability of a successful implementation of functionality in a cost-effective manner.”

SystemC and TLM2.0

• SystemC is defined and promoted by Open SystemC Initiative (Accellera)
  – A system level modeling language which provides event-driven simulation interfaces
  – Set of C++ classes and macros
  – Modules, Ports, Signals, Processes, Channels etc...

• Transaction Level Models 2.0 defines communicating processes
  – Calculate and represent all the operations, state changes, data movements and computations
AndeSysC™

• Andes virtual platform solution based on SystemC
• Near-cycle accurate, extensible and flexible models of AndesCore™ V5 RISC-V processor IP’s
• AndeShape™ platform IP components
• Andes Custom Extension™ (custom instructions)
• AndeSight™ IDE and AndeSoft™ SW stack
Supported AndesCore™ Features

- **CPU IPs**
  - AndesCore™ RISC-V V5 Cores
  - All 22-/25-/27-/45-series

- **Architecture features**
  - Interruption Architecture (PLIC)
  - Performance Monitoring
  - Hardware Stack Protection
  - Control and Status Registers
  - Optional:
    - MMU/MPU
    - Icache and Dcache
    - Floating Point Unit
    - Digital Signal Process Unit
    - ...

AndesCore™ V5

Dependent IPs:
- 45-series uCore, PMP/PMA
- A(X)27 uCore, PMP
- 25-Series uCore, PMP, MMU (aX12)
- 22-Series uCore
Supported Interfaces

- Clock and Reset Pin
- DLM Port
- ILM Port
- Interrupt Pins
- Slave Port
- Bus Interface Unit
- ACE Interfaces (e.g. ACM and ACP)
Supported Platform IPs

- DMA Controller (DMAC)
- GPIO
- LCD Controller (LCDC)
- Real Time Clock (RTC)
- Secure Digital Host Controller (SDC)
- Synchronous Serial Port (SSP)
- Timer
- UART Controller
- Watchdog Timer (WDT)
Virtual SoC Example
Streaming Port

NX27V SystemC Model

CoProcessor SystemC model

Command Channel

Data Channel

Data Pre-process

Data Post-process
Execute AndeSysC of Streaming Port

1. Executing SystemC simulator

```
SystemC 2.3.3-accellera --- Mar 8 2021 10:57:53
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ALL RIGHTS RESERVED
AndeSystemC v1.1.182.495 (d71f87c)(nds_vcore.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(v5_wrapper.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(v5_pseudo_bus.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(v5_pseudo_bus.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(nds_tl2_adapter.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(nds_tl2_adapter.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(nds_tl2_adapter.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(nds_tl2_adapter.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(v5_tl2_idim_slave.cxx)
AndeSystemC v1.1.182.495 (d71f87c)(v5_tl2_idim_slave.cxx)
socketbase: using fd 4
socketbase: server at ::9900
GDB init ...
Ib init skipped
Log Nx27V(9900)
```

2. Running Design

```
----- ISS FINISHED ----
Config_NX27V total icount : 00011821
Config_NX27V total cycle : 00109963
Config_NX27V stall cycle : 00098142
Config_NX27V icache access : 00000000
Config_NX27V icache miss : 00000000
Config_NX27V dcache access : 00000000
Config_NX27V dcache miss : 00000000
Config_NX27V Branches Num : 00003822
Config_NX27V BTB mispred : 00000103
socketio: leof1
GDB init skipped
[AndeSysC] Simulation Finished
```

3. Execution Finished
AndeSysC and AndeSight

SystemC Virtual Platform

- AndeSysC
- COP Model
- RTOS
- Memory Model
- Peripheral Model
- Peripheral Model

GDB

debug mode

Taking RISC-V® Mainstream
AndeSysC™ Summary

• **Compatibilities with Flexibility**
  – Supported by AndesCore™ and AndeShape™ Platform models
  – Compatible with 3rd parties’ IP’s/tools using TLM2.0 protocol
  – Flexibility to configure and construct any virtual SoC

• **Near-Cycle Accurate Simulation**
  – Early profiling during the rapid prototyping stage
  – High level estimation of performance for the eventual real devices

• **Development Acceleration**
  – Interact directly w/ feature-rich AndeSight™ and AndeSoft™
  – Facilitate HW/SW Co-design through virtual prototyping