Faraday RISC-V Based ASIC Solution for Edge AI and IoT SoCs

Oct 2019

FARADAY

Synergy for Excellence

Confidential

Agenda

- Company Profile
- AIoT SoC Achievements
- Faraday's Solution to AIoT ASIC Design

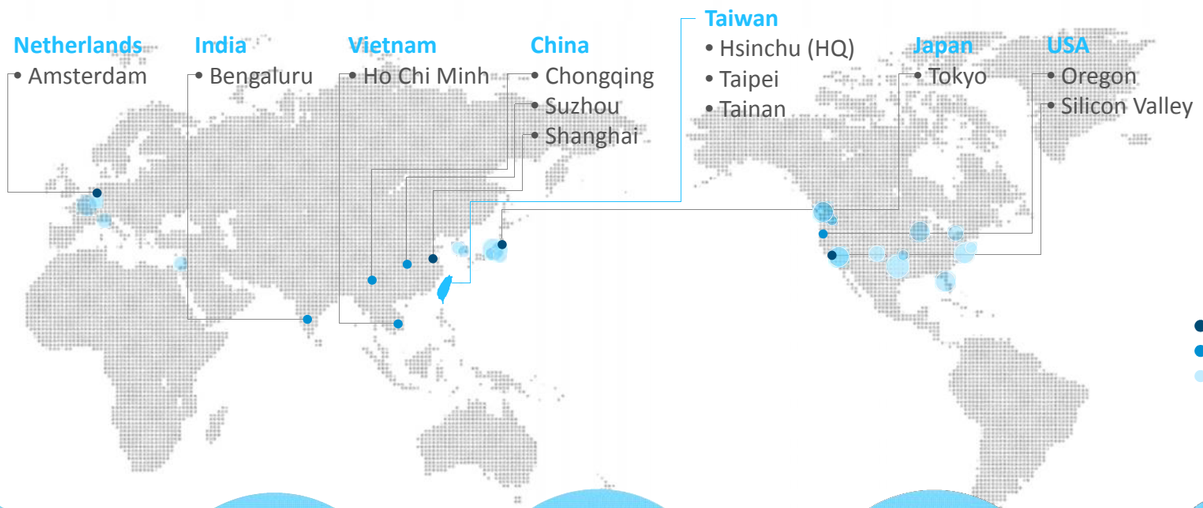
Faraday at A Glance

Established since Y1993
- Taiwan IPO since Y1999 (TWSE: 3035)
- Commitment in ASIC & IP business

Financial status
- Capital: US$80M
- Revenue: US$163M (Y2018)

Top management
- Chairman: Stan Hung
- President: Steve Wang
- COO: Flash Lin

Global Deployment



2200+ ASIC projects taped-out

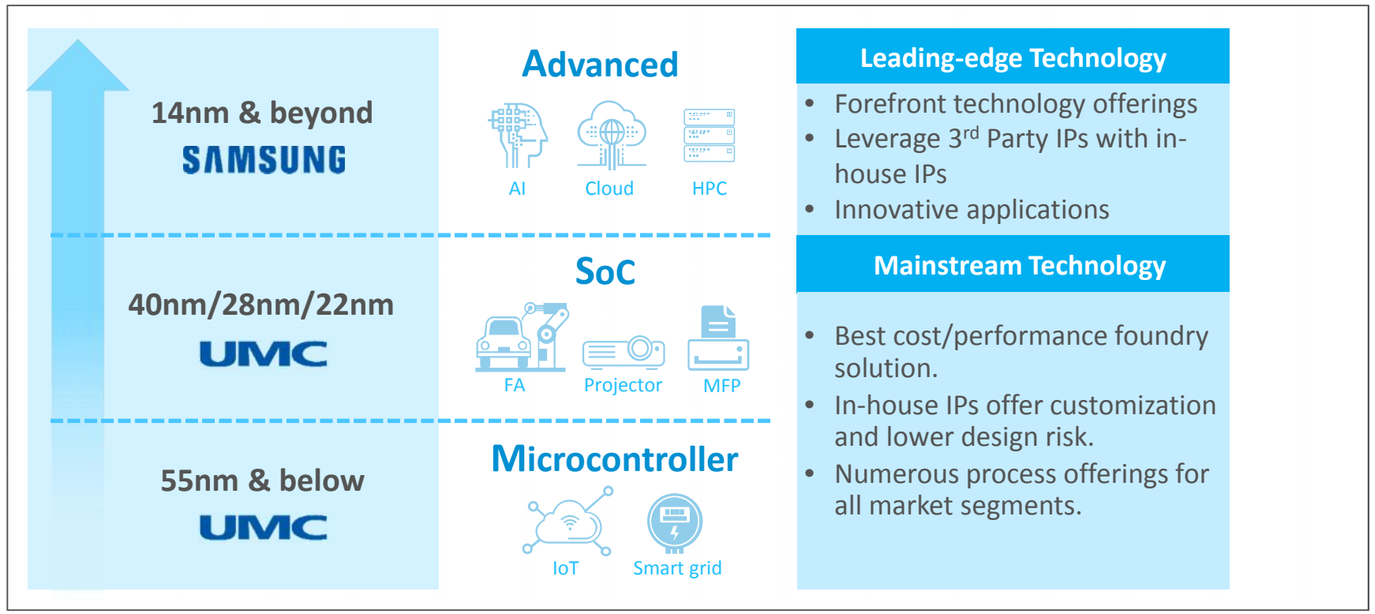
850+ Employees worldwide

5 Global sales offices with 20+ Sales Rep.

8 Design centers

3000+ IPs silicon-proven

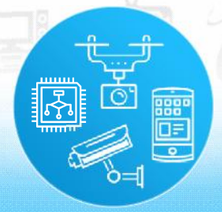
Strategic Partnership with UMC and Samsung Foundry



Diversified Application Coverage

Communication

- Femtocell
- Switch
- Networking security
- Pre5G/5G
- Home gateway



Consumer/ Multimedia/ PC peripheral

- DSC
- IP Cam
- Drone
- Consumer MCU
- Speech controller
- Calculator
- USB dongle/Hub
- eMMC/NAND flash/UFS

AIoT

- **AI**
- **Pico projector**
- **Enterprise SSD**
- **3D Sensing**
- **Security IC**
- **HPC**
- **Smart home**
- **SSD**
- **Wearable**
- **Ethernet MCU**
- **Pressure sensor**
- **Sweeping robot**

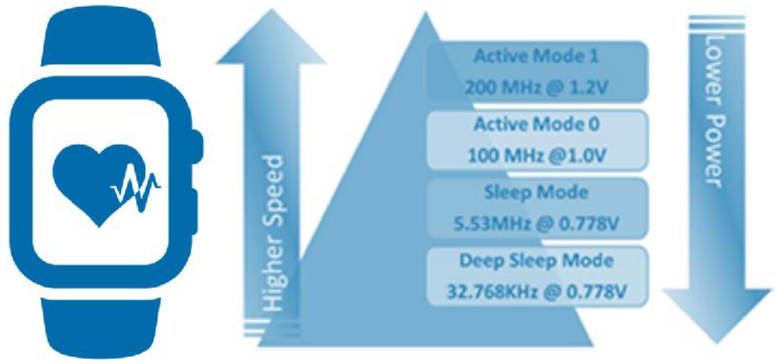
Industrial

- Agriculture
- Automotive
- Aviation
- Medical
- MFP
- Robot
- FPGA
- Factory automation
- Solar power

AIoT SoC Achievements

Wearable

- **Enabling AI Technology in Wearable Devices**
  - Neural Network Hardware Accelerator
  - Support ECG, ECG Pro and Arrhythmia
- **IP customization service**
  - CPU hardness expertise
  - Analog IP customization
- **Ultra low-power SoC Design**
  - UMC 55uLP process
  - Support AON (Always ON)
  - Low operating voltage for long battery life
- **Proven software design kit based on FreeRTOS**



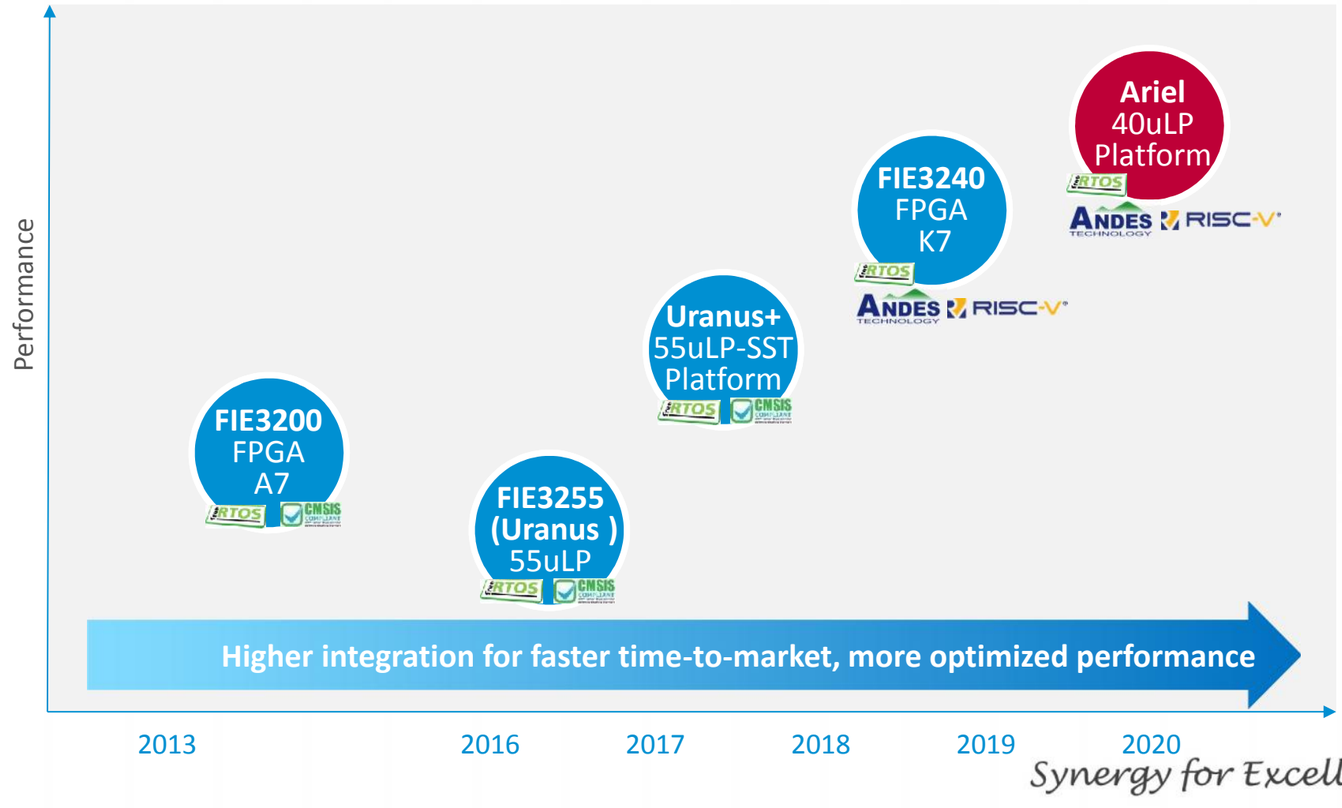
Medical Image Processing

- **Project Challenges**
  - Integrate multiple chips into an ASIC
    - MCU + FPGA + USB PHY + PCIe
  - Smaller form factor and Ultra low power
  - Boost throughput and bandwidth for higher resolution sensors
- **Methodology solutions**
  - Multi-mode, Multi-corner timing optimization and analysis
  - Low-power function verification and layout verification
  - Crosstalk noise prevention, analysis, and repair
  - PCIe IP replacement and driver porting
  - Upgrade USB protocol to USB3
  - PLL and LVDS customization
  - Software porting for PCIe and DDR

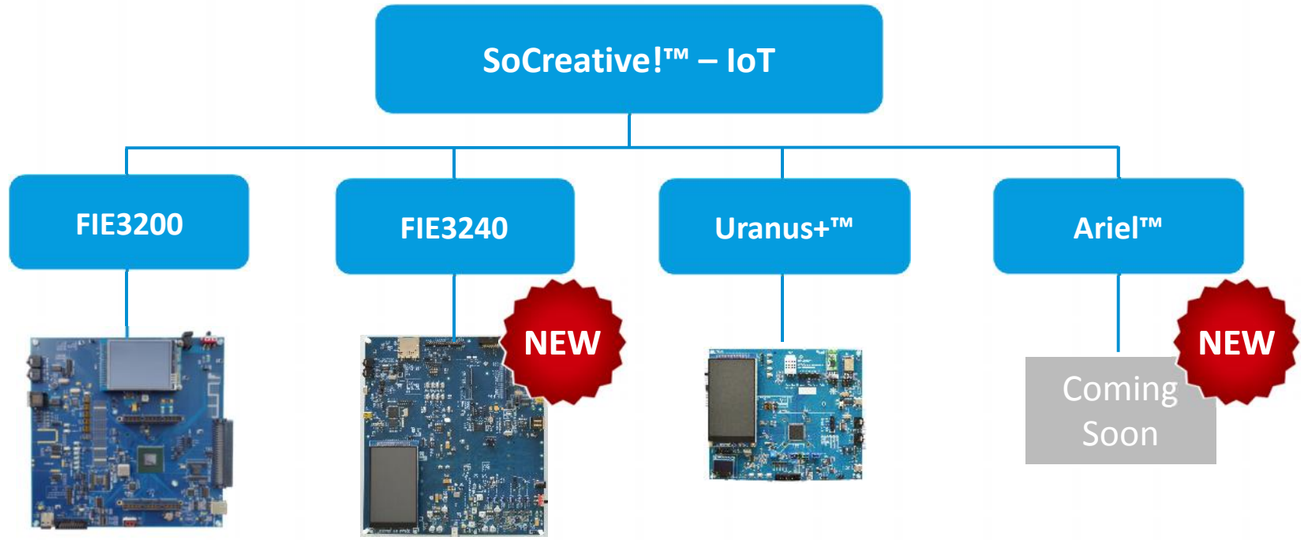
Confidential

Faraday's Solution to AIoT ASIC Design

SoCreative!™ IoT SoC Platform Development Roadmap



SoC Platform Product Tree



- FPGA
- Artix 7-200T
- RISC-V Support
- SDK (CMSIS)

- FPGA
- Kintex 7-325T/K7-410T
- **RISC-V Demo**
- SDK (CMSIS)

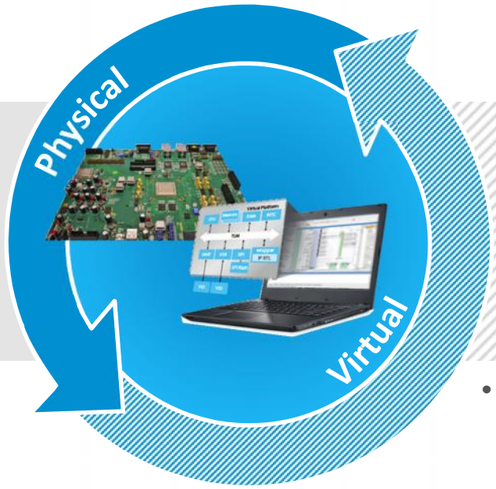
- 55uLP SoC
- CM4
- Up to 100MHz
- 1MB eFlash

- 40LP- SoC
- **Andes N25F**
- Up to 200MHz
- 1MB eFlash

Physical or Virtual SoC Development Platform

SoCreative!
SoC EVB Platform
Real Performance Logic and system verification

- Proven system
- Up-to-date IPs
- Pre-verified SW package
- Good for IP hardware verification



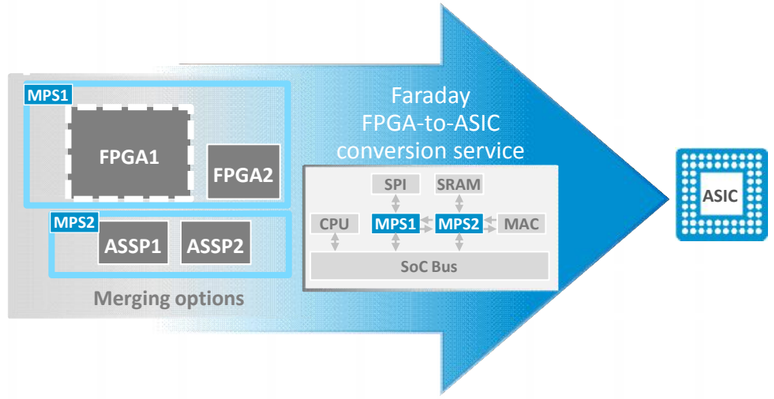
SoReal!
Virtual Platform
Enable early software development

- Pre-built IP models from Faraday, ARM fast model, and Synopsys
- System C & HDL co-simulation
- Virtual IO support
- Suitable for boot code, OS, driver, middleware and application development

FPGA-to-ASIC Service Accelerates Time-to-market

- **Seamless conversion for existing FPGA solutions improving performance, power and area**
  - Security enhancement
  - Private labels
  - Package derivatives for different markets
  - Lower system BOM cost
  - Form factor reduction
  - Obsolete part replacement
  - Supply chain stability

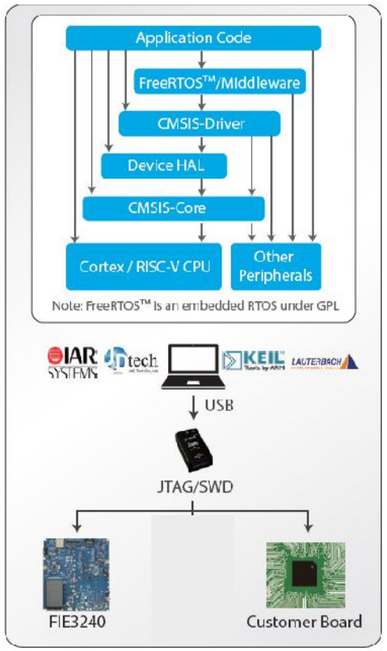
Faraday's Micro-programmable Sequencing engine (MPS) for quick circuit function replacement & implementation



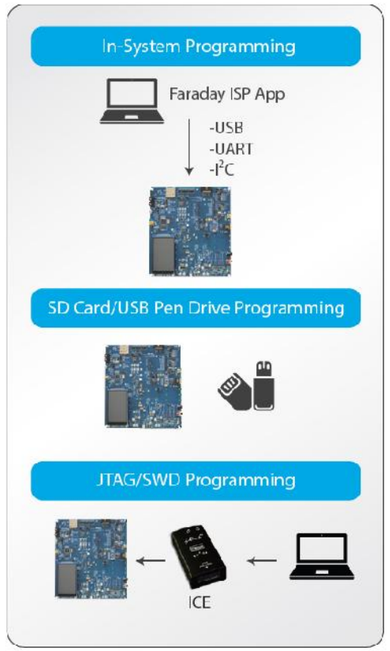
4 months from Final Spec Handoff to Tape out

FIE3240 Development Environment

Development stage

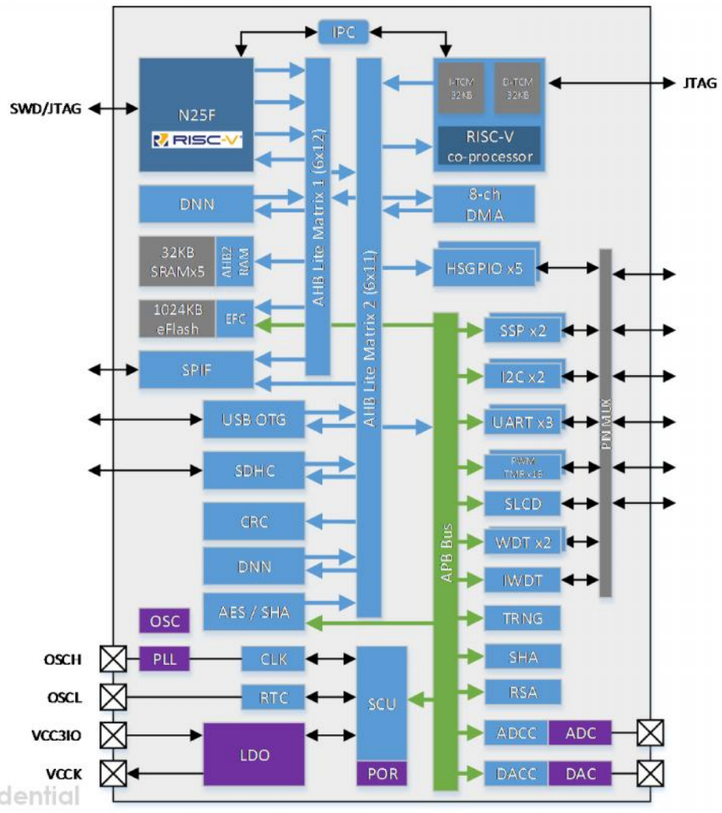


Mass production and update stage



- **Features:**
  - Enlarge FPGA logic resource
    - FIE3200 : A7-200T; FIE3240 : K7-325T/K7-410T
    - 1.5 ~ 2x gate count
  - Supports PCIe-to-PCIe interconnect
    - High speed connector by type-C
    - FPGA2FPGA, FPGA2ASIC communication
  - HAPS daughter board re-use
    - Enable USB3, MIPI, GPHY, DDR function for future project support
  - Multiple Voltage IO bank support
    - Support 1.8V/2.5V/3.3V

Ariel™ Platform (Q2 2020)

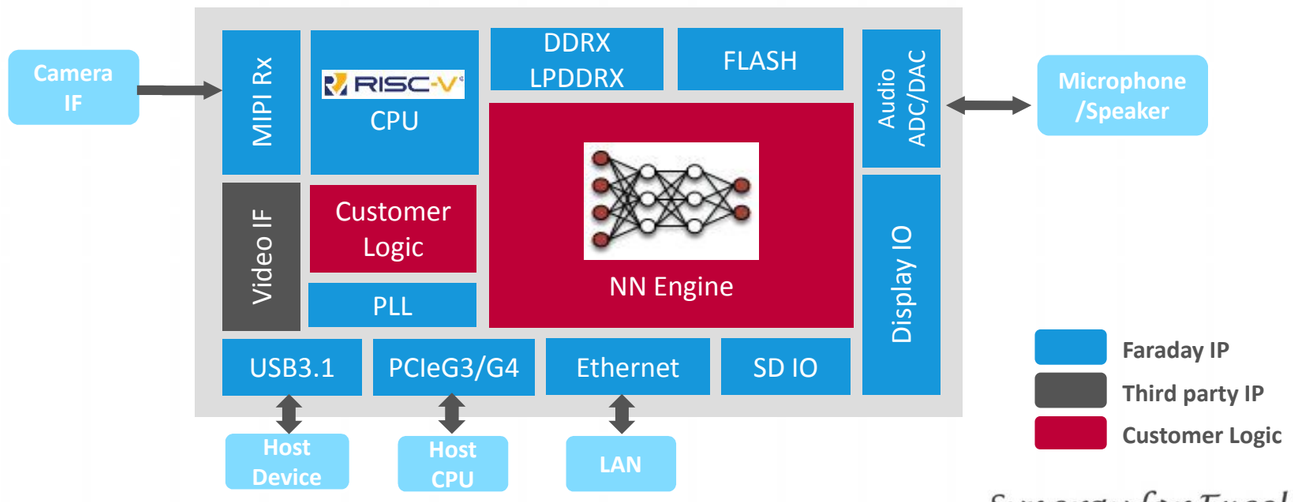


- **Features:**
  - RISC-V Cores
    - Andes N25F
    - Develop assistant-processor applications
    - SDK Ecosystem (Tool-chain, IDE, Device Drivers)
  - 40LP @0.9V/1.1V
    - 0.9v low power kit
    - Numerous IP blocks: Analog IPs/IO cell /Core cell/SRAM
  - Memory
    - 1024KB eFlash
    - 160KB SRAM
  - DNN Engine
    - Enable voice conversion application
  - Peripherals
    - USB OTG/DMA/SDHC/SLCD
    - HSGPIO
    - I^2C, SSP, UART, SPIF
    - 12-bit ADC/10-bit DAC
    - SHA/AES/RSA/TRNG/CRC

Confidential

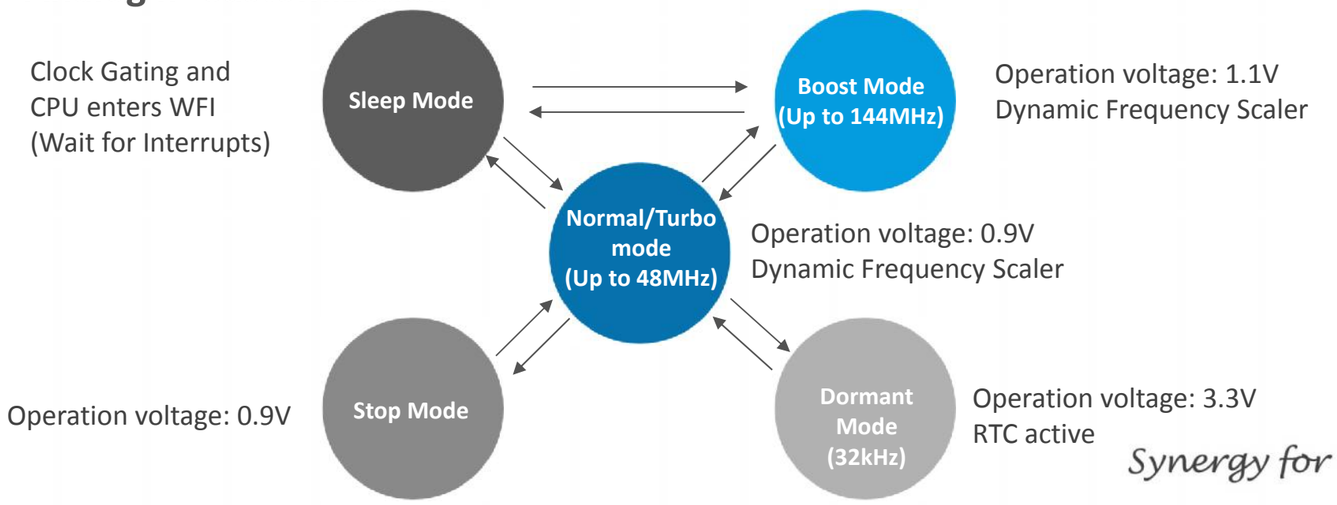
Total Solution Block Diagram of AI Edge Computing

- **Broad Applications :** Security, Surveillance, Wearable, Voice Recognition…etc
- **Comprehensive IP Coverage :** DDR, MIPI, USB, PCIe, Ethernet, ADC/DAC
- **CPU Harden for high performance**
- **Wide Technology Adoption:** 55nm/40nm/28nm/14nm/10nm/8nm
- **FPGA2ASIC Conversion Service**



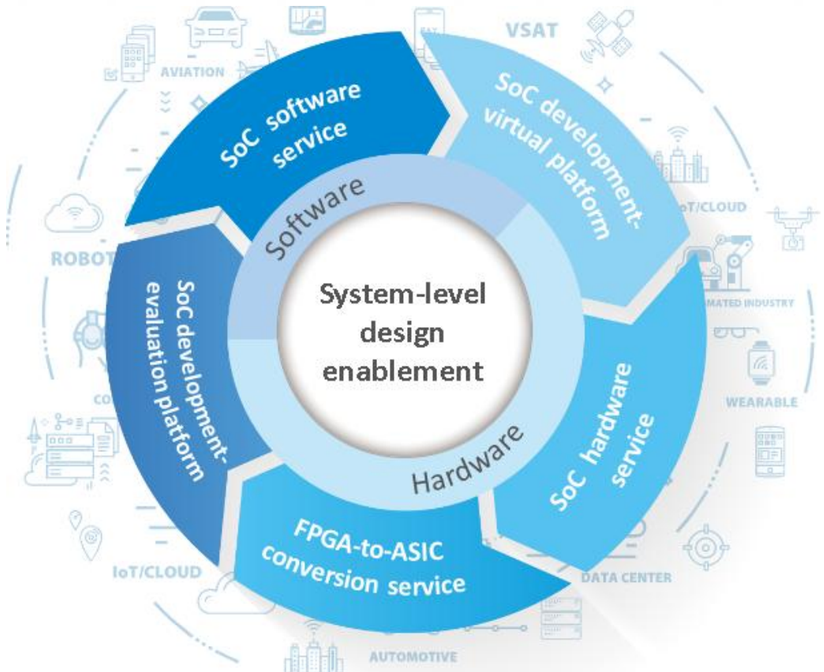
Low Power SoC Design and DVFS

- Multi-Vt Device
- DVFS (dynamic voltage and frequency scaling)
- Power Domain Partition
- Faraday PowerSlash™ IPs offer fundamental building blocks for a low-power design
- Micro program sequence engine for power saving
- Analog IP Customization



Confidential

Summary: Why Faraday?



- **Diversified successful stories**
- **Comprehensive IP portfolio**
- **IoT SoC development platforms**
  - RISC-V based
  - Logic and system verification
  - Enable software evaluation
- **FPGA-to-ASIC conversion service**
- **Low power high performance design**

- ## Confidential information

  The material is being disclosed to you pursuant to a non-disclosure agreement between you or your employer and Faraday. Information disclosed in this presentation may be used only as permitted under such an agreement.

- ## Legal notice

  The information contained in this presentation is intended to provide a general guide as to which product is suited for a given requirement and shows suggested product applications. Specified functions and properties for products are only valid when handling instructions and other stated conditions and recommendations have been considered and followed. All descriptions, illustrations and dimensions in the information represent general particulars and do not form part of any contract. All information is provided “as is”, with no guarantee of completeness, accuracy, timeliness or of the results obtained from the use of the information, and without warranty of any kind, express or implied, including but not limited to warranties of performance. All information is subject to change without prior notice. Faraday assumes no responsibility whatsoever for any errors or inaccuracies about the information.