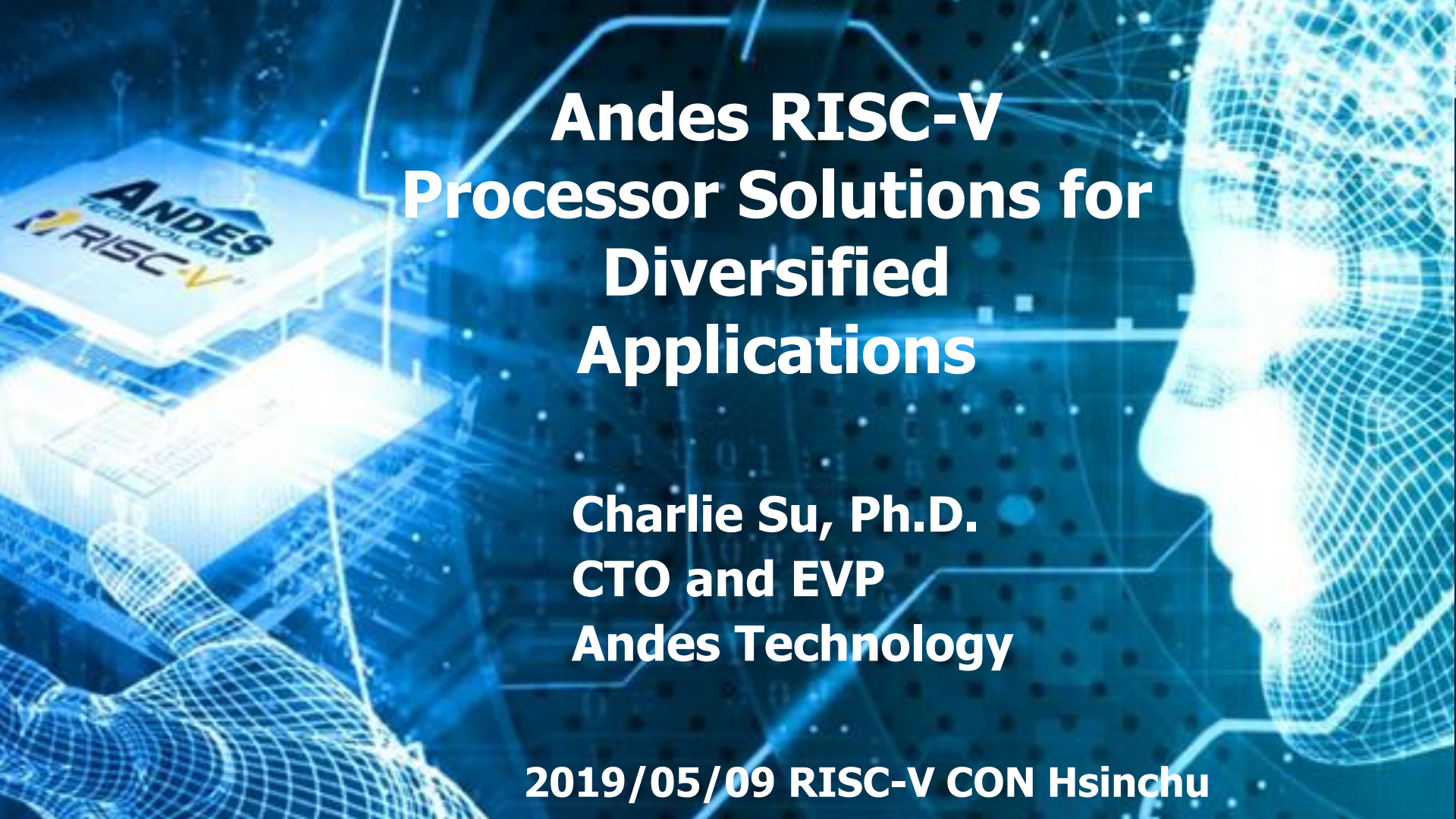


Andes RISC-V Processor Solutions for Diversified Applications

Charlie Su, Ph.D.
CTO and EVP
Andes Technology

2019/05/09 RISC-V CON Hsinchu

Overview of the Talk

- **Rich Experience of CPU Usage**
- **Latest AndeStar™ V5 Lineup**
  - New: Ultra-Compact Low-Power Processor
  - New: 1st RISC-V Processor Family with DSP/SIMD ISA
  - New: Multicore Processors with Cache-Coherence
- **RISC-V Open Source SW**
  - Compilers
  - Linux and U-Boot
  - FreeRTOS
- **Concluding Remarks**

Rich Experience on CPU Usage

- **14-year, 100-customer and billion-SoC experience**
  - Interrupt sources: <16? Or >100?
  - Interrupt latencies: care and don't care
  - Data processing:
    - Efficiency: DSP+SIMD based on existing GPR's
    - Performance: scalable vectors with more resources
  - Write-back and write-through caches
  - Loading RO-data from icache !
  - Hardwired engines and "coprocessors"
  - Different memory architectures
  - Small cores in MCU's or large SoC's
- **Andes:**
  - A leader who understands diversified needs

AndeStar™ V5 Processor Lineup

Cache-Coherent Multicores	**A25MP**[a] 1/2/4 **A25**, L2$, L1/IO coherence	**AX25MP**[a] 1/2/4 **AX25**, L2$, L1/IO Coherence	LM/Caches, Branch Pred, Vec. Intpt	**5-stage >1 GHz**[b]
Linux with FPU/DSP	**A25** **N25F**, MMU, DSP	**AX25** **NX25F**, MMU, DSP		
Fast/Compact with FPU/DSP	**N25F/D25F** V5/32b, FPU, PMP, DSP (**D25F**)	**NX25F** V5/64b, FPU, PMP		
Slim and Efficient	**N22** V5[e]/32b 32/16 GPR			**2-stage 700MHz**[b]

a. A(X)25MP: available Q2/2019; b. 28nm RVT, SS, 0.81V, 0C, with I/O constraints.

AndeStar™ V5 Processor Lineup

Cores[1]	AndeStar™ ISA[2]	GPR bits	Priv. levels	Intr. Ctlr	MMU	I/D$	ECC	FPU[3]	DSP (P)	ACE[3]	MP
N25(F)	V5	32	M+U	PLIC		I/D	✓	#		#	
A25	V5	32	M+U+S	PLIC	✓	I/D	✓	✓	✓	#	
NX25(F)	V5	64	M+U	PLIC		I/D	✓	#		#	
AX25	V5	64	M+U+S	PLIC	✓	I/D	✓	✓	✓	#	

1. Common features: PMP, branch prediction, CoDense™, PowerBrake, StackSafe™
2. V5: RV*IMAC + Andes Extensions, V5e: RV*EMAC + Andes Extensions
3. ✓: included; #: separately licensable

V5: Best Extensions to RISC-V

AndeStar™ V5: RISC-V + Andes Extensions

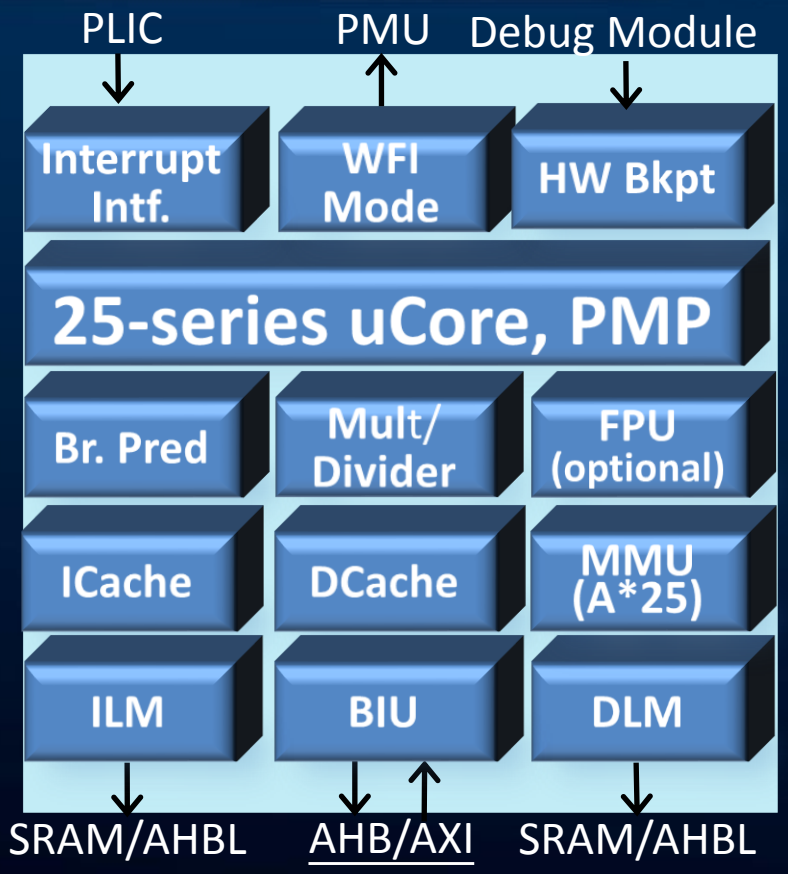
- **Baseline extensions:**
  - Baseline performance extensions
  - CoDense™ extensions
  - Vector interrupt controller with priority-based preemption → Fast Interrupt TG
  - Cache management features
  - Performance monitor enhancement
  - Point features:
    - StackSafe™, QuickNap™, PowerBrake
- **DSP/SIMD extensions**
  - Contributed to RISC-V P-ext. as a draft
  - Andes serving as Chair for P-extension TG

- **Andes Custom Extensions™:**
  - Powerful tool to enable user-defined instructions
  - No CPU background needed
  - Solution for growing demands for Domain-Specific Architecture (DSA)

AndesCore™ 25-Series:
1st DSP-capable RISC-V CPU Family
(D25F/A25/A25MP, AX25/AX25MP)

25-Series: Overview

- **AndeStar V5 architecture:**
  - RV32/RV64-I/E-MAC + Andes Extensions
  - Optional FPU: F, FD
  - Optional S-mode/MMU: SV32/39/48
    - Support all page sizes
- **5-stage pipeline, single-issue**
- **Configurable multiplier**
- **Optional branch prediction**
- **I/D caches and Local Memory**
  - Optional parity or ECC protection
  - Hit-under-miss caches
  - HW unaligned load/store accesses
- **Bus interface**
  - A master port (AHB/AXI)
  - An optional slave port (AHB)

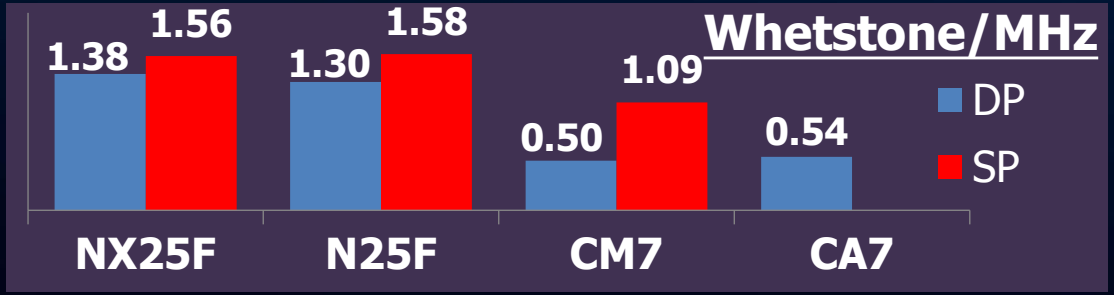


25-Series: Benchmarks

Features	Base	FP	Linux
32KB I$/D$ + 256 BTB	Yes	Yes	Yes
SP/DP FPU	--	Yes	Yes
MMU and S-Mode	--	--	Yes
Worst-Case Freq. (GHz)[1]	1.2	1.2	1.2
Coremark/MHz[2]	3.57 (rv32), 3.53 (rv64)		
DMIPS/MHz[2]	1.97 (rv32), 2.13 (rv64)		

1: **28nm** RVT 9T library and high-speed memory. Frequency at 0.81v/-40ºc.
2: **AndeSight v320** toolchain; DMIPS/ground rule uses no-inline option.

- **Benefits of V5 extensions**
  - ~20% higher Coremark & DMIPS
  - 12% smaller code size (CSiBE)
- **FP performance**
  - Up ~20% since initial release
- **RTL code**
  - CAD tool friendly
  - Tool-configured by customers



P-Ext. (DSP/SIMD) Examples

Types	Instruction Operations	Cycles
SIMD	Four 8x8 multiplications: 16= 8x8; 16= 8x8; 16= 8x8; 16= 8x8 Two 16x16 multiplications: 32= 16x16; 32= 16x16	1
Partial SIMD	Four 8x8 multiplications with 32b accumulation: 32= 32 + 8x8 + 8x8 + 8x8 + 8x8; 32= 32 + 8x8 + 8x8 + 8x8 + 8x8 (2nd op: RV64 only) Two 16x16 multiplications with 32b accumulation: 32= 32 + 16x16 + 16x16 32= 32 + 16x16 + 16x16 (2nd op: RV64 only)	2
RV64 Only	Two 32x32 multiplications with 64b accumulation: 64= 64 + 32x32 + 32x32	3

25-Series: P-Ext. Speedups

- **DSP libraries for RV32-P** (>200 functions in 8 categories)

Speedup	Basic	Cmplx	Ctlr	Filter	Matrix	Ststcs	Xform	Utils	ALL
AVG	2.40	1.62	1.84	2.26	1.62	2.44	1.29	1.08	**1.82**
MAX	5.16	4.09	2.13	4.11	2.75	4.39	1.78	1.43	**5.16**

Note: Compared with CM4 (similar code size), 50% faster in Q functions, 38% faster in F32

- **DSP libraries for RV64-P** (>200 functions in 8 categories)

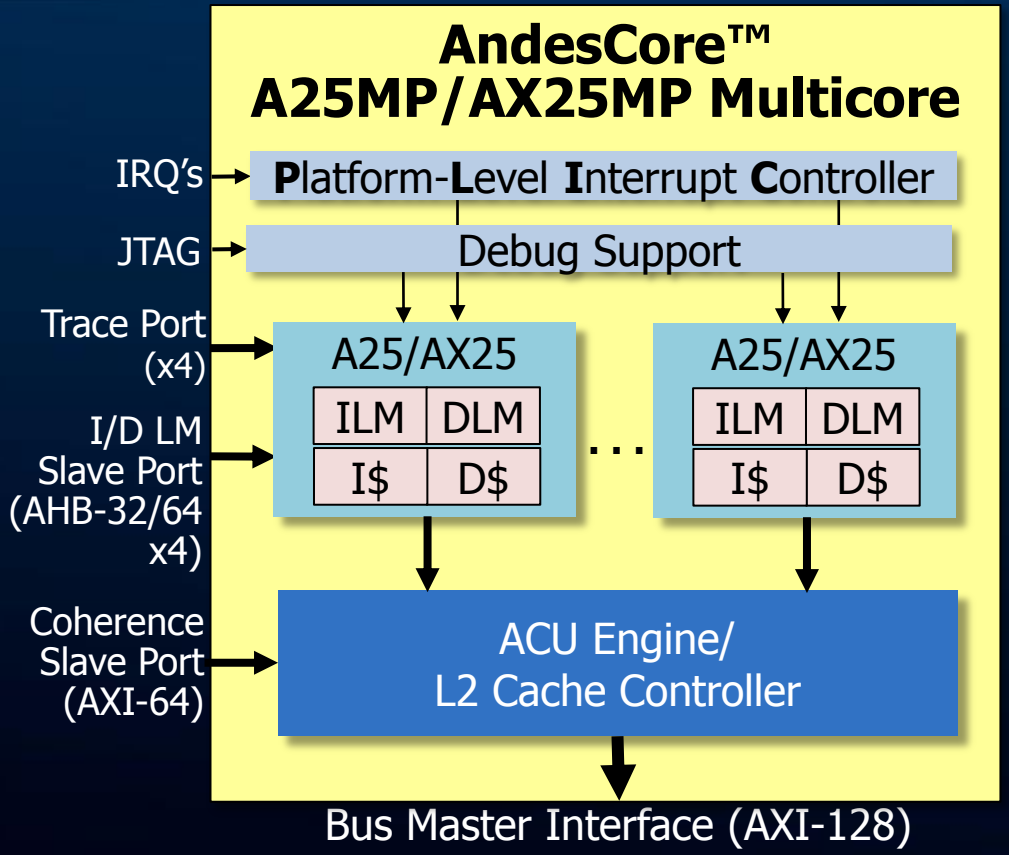
Speedup	Basic	Cmplx	Ctlr	Filter	Matrix	Ststcs	Xform	Utils	ALL
AVG	4.73	1.92	1.31	2.41	3.04	4.14	1.28	1.19	**2.50**
MAX	10.81	4.14	1.59	5.04	6.83	8.51	1.67	2.72	**10.81**

- **Speedups for various applications**

Cores	RV64-P		RV32-P	
APP	CIFAR10 (image classification)	PNET (90% of face detection)	AMR voice codec	MP3 decode
Speedup	**10.99**	**7.57**	**3.67**	**1.84**

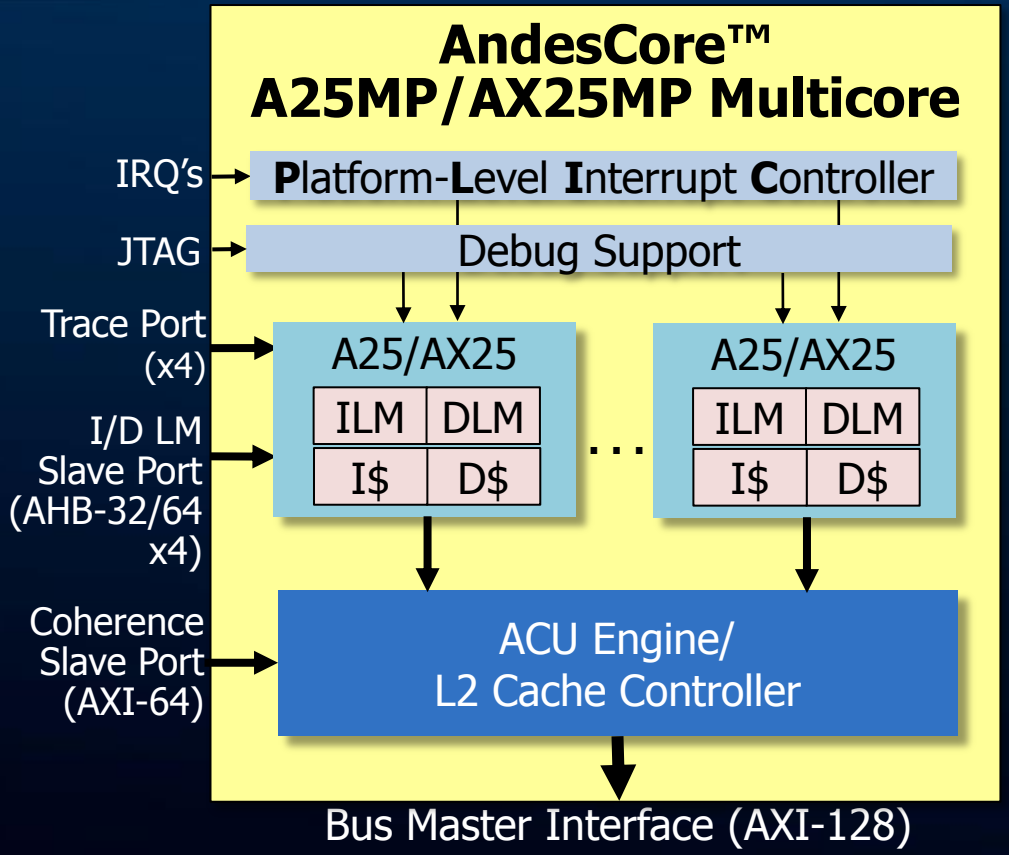
AndesCore™ A(X)25MP:
Cache Coherent Multicore

A(X)25MP: Cache-Coherent 多核芯



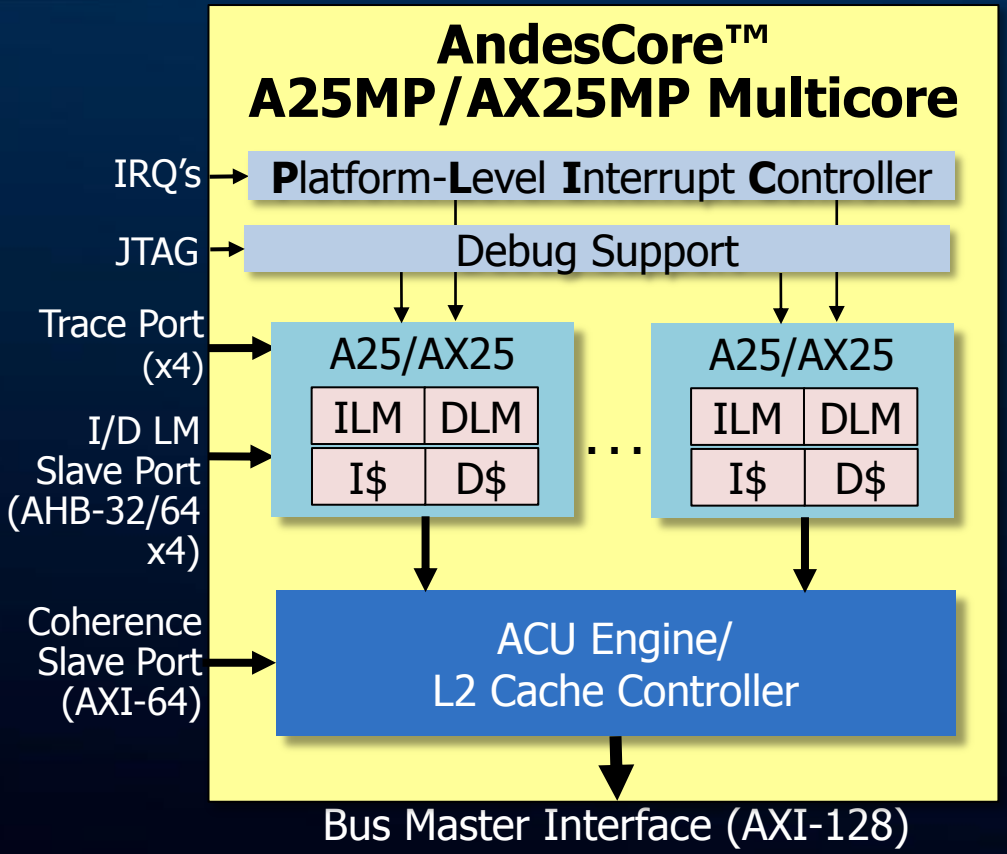
- **1~4 A25/AX25 CPUs:**
  - RV-IMACFD ISA + V5 extensions
  - P-extension draft
  - Supporting SMP Linux
- **Bus Interfaces**
  - LM slave port
  - Coherence slave port
  - AXI bus master interface
    - N:1 synchronous clock ratio
- **PLIC for interrupt handling**
- **Debug/trace support**

A(X)25MP: Cache-Coherent 多核芯



- **ACU Coherence Unit**
  - MESI cache coherence protocol
  - Duplicate L1 dcache tags
  - IO coherence for cacheless masters
- **L2$ Controller (optional)**
  - **Size**: 128KB to 2MB
  - **Line size**: 32B
  - **16-way** with pseudo random replacement and writeback
  - **SRAM optimization:**
    - SRAM access cycles: ≥2 (configurable)
    - Bank interleaving:
      - 2 tag banks, 8 data banks
    - Fully pipelined without contention

A(X)25MP: Cache-Coherent 多核芯



- **L2$ Controller (cont.)**
  - **Writeback/invalidate control**
  - **ECC protection** (SECDED): same as that for L1 memory
  - **Prefetching**
    - Instruction: 1/2/3 lines after a miss
    - Data: 2/4/8 lines after consecutive linear misses (tracking 8 address sequences)
- **Linux-capable configuration**
  - RV64, 32KB I/D$, 256-entry BTB, 128-entry STLB, 8-entry PMP
  - 1 GHz at 28nm (worst case)
  - Gate count:
    - Core: >200K, ACU+L2: <200K

Latest Status of RISC-V Open Source SW

GNU Toolchain

- **bintuils 2.32: released at Feb, 2019**
- **GCC 9: release at Apr, 2019**
  - **RV32E (16 GPR)**
  - **Interrupt attribute enables pure-C ISA**

```
void __attribute__ ((interrupt))
foo (void) {
  . . .
}
```

  - **ELF attribute**: Record more info in object file
    - Arch info, stack alignment, or version of privilege spec
    - Disassembler: "How can I interpret the ELF correctly?"
    - Linker: "Can I link those ELF objects?"
    - Loader/debugger: "Can I load the ELF objects and run them?"

LLVM Compiler

- **LLVM**
  - RV32/RV64-IMAC-FD code gen
  - Working on hard-float calling convention
    - Expected to be completed this year

- **LLD:**
  - Maintainer: Andes
  - Faster and smaller implementation than GNU's linker (LD)
  - RISC-V support is included in LLD 8 !

Linux: U-Boot

U-Boot

- Maintainer: Andes
- SMP support (Reviewing)
- S-mode support
- More driver support for AE350
  - mmc, mac, smc, spi
- Merged/verified patchsets from contributors
- FU540 board support

```
U-Boot 2018.11-00208-ga8cb78f (Nov 20 2018 - 17:29:58 +0800)

CPU:   rv64imafdc
Model: andestech,ax25
DRAM:  1 GiB
Flash: 64 MiB
MMC:   mmc@f0e00000: 0
Loading Environment from SPI Flash... SF: Detected mx25u1635e with page size
MiB
OK
In:    serial@f0300000
Out:   serial@f0300000
Err:   serial@f0300000
Net:   no alias for ethernet0

Warning: mac@e0100000 (eth0) using random MAC address - 5e:cc:27:0d:56:31
eth0: mac@e0100000
RISC-V #
```

Linux: Glibc Library

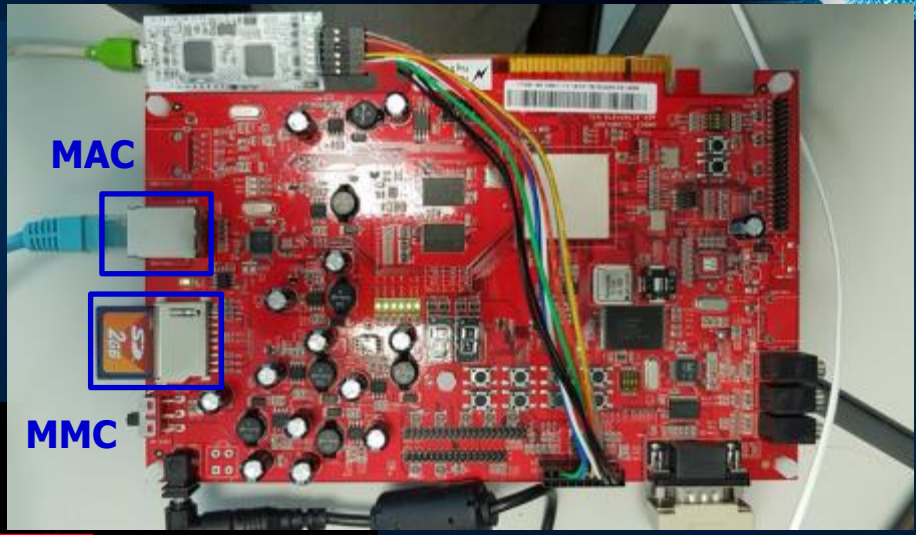
- **RV64 support:** in v2.27 at Feb, 2018
- **RV32 support**
  - Ported by Andes
  - Ready to upstream!
    - Waiting Y2038 patches for Linux kernel
  - Latest stable branch:
    - https://github.com/riscv/riscv-glibc/tree/riscv-glibc-2.29

Linux: Tool Support

- **Ftrace tool**
  - For developers to debug
  - Support dynamic ftrace
- **Perf tool**
  - For developers to evaluate the bottleneck of the whole system
- **Module support (dynamic loading)**
  - Support all relocation types for RV32 and RV64
- **Power Management support by sysfs commands**
  - Suspend2ram: suspend a process, and woken up by interrupt
  - PowerBrake: slow down execution to reduce power consumption
- **Kernel verification:**
  - Qualified by LTP (Linux Test Project)

Linux: Fedora on RISC-V

- **Fedora on Andes AE350**
  - AndesCore™ **AX25** (rv64)
  - A platform with mmc and mac
  - Able to run Fedora distribution
  - Able to install packages



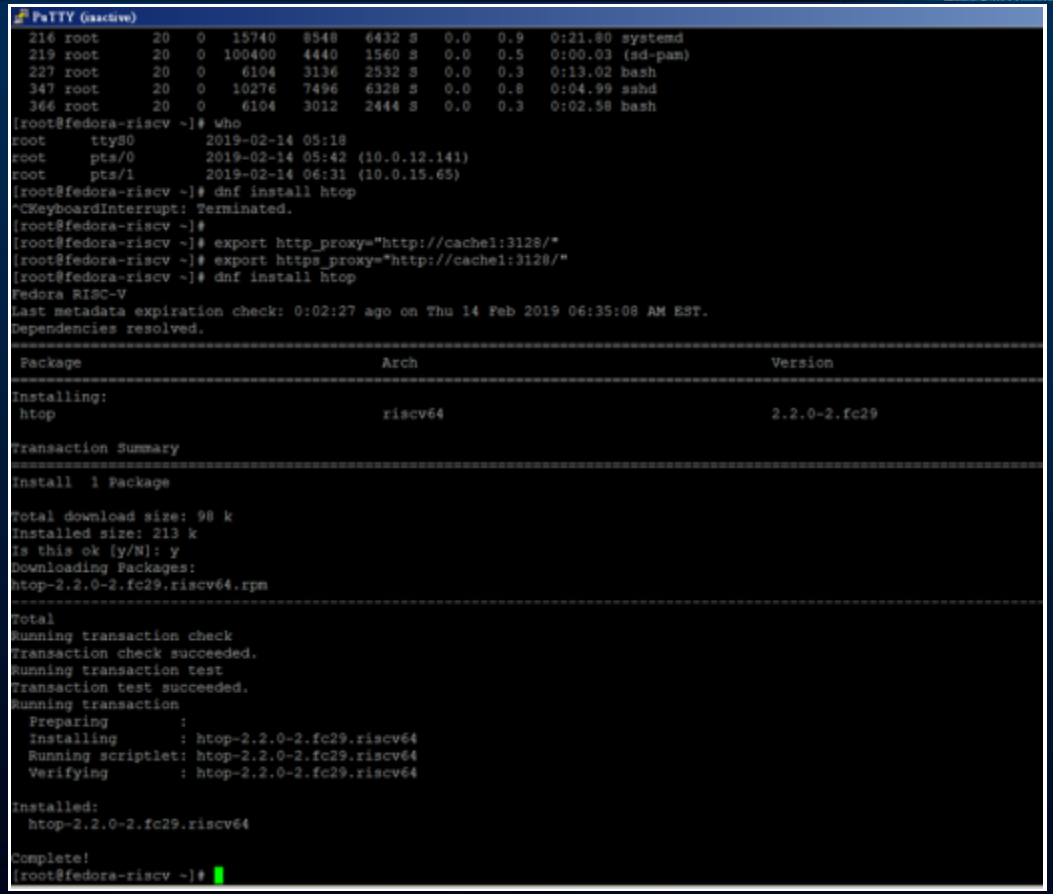

```
[root@fedora-riscv ~]# cat /proc/cpuinfo
hart    : 0
isa     : rv64i2p0m2p0a2p0f2p0d2p0c2p0xv5-0p0
mmu     : sv39

[root@fedora-riscv ~]# uname -a
Linux fedora-riscv 4.17.0-00250-gd63b2bc-dirty #4 PREEMPT W
[root@fedora-riscv ~]#
```

rv64-imafdc-v5

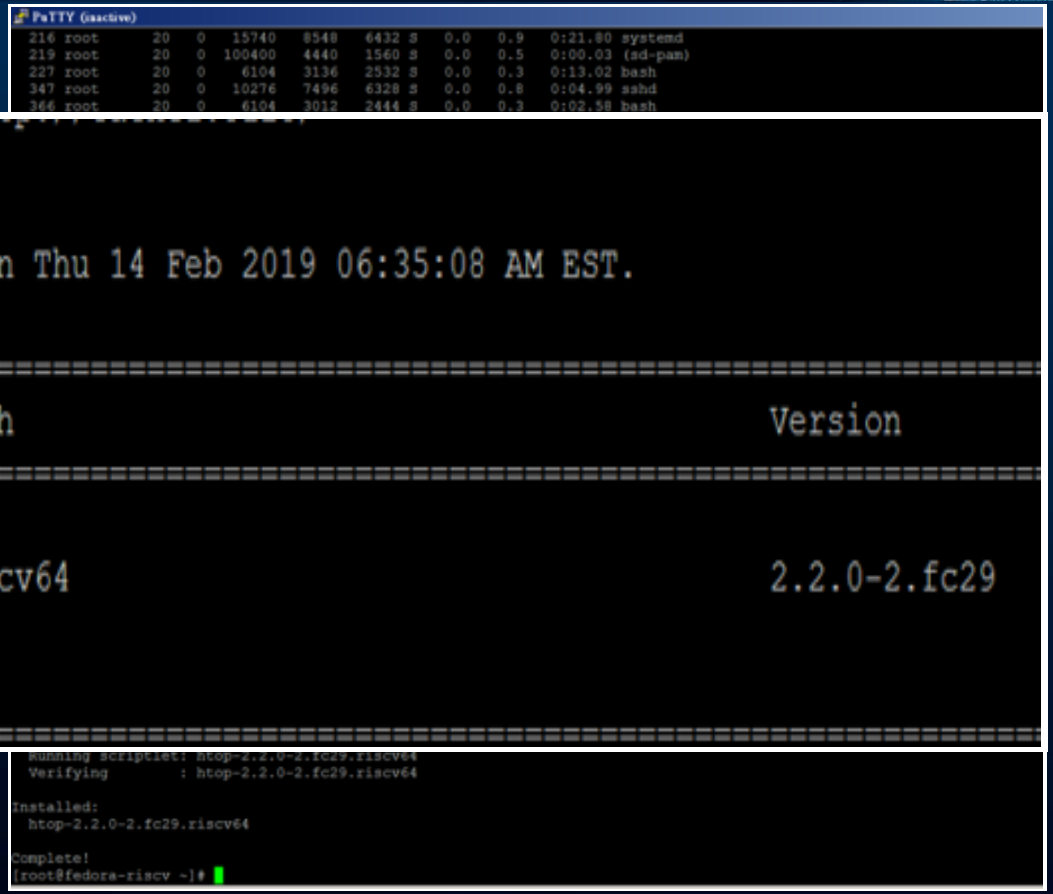
Linux: Fedora on RISC-V

- Use dnf to install htop rpm



Linux: Fedora on RISC-V

- Use dnf to install htop rpm



Linux: Fedora on RISC-V

- Use dnf to install htop rpm

```
[root@fedora-riscv ~]# dnf install htop
Fedora RISC-V
Last metadata expiration check: 0:02:27 ago on
Dependencies resolved.
================================================================================
 Package                                                    Arch
================================================================================
Installing:
 htop                                                       risc

Transaction Summary
================================================================================
```

```
Transaction Summary
================================================================================
Install  1 Package

Total download size: 98 k
Installed size: 213 k
Is this ok [y/N]: y
Downloading Packages:
htop-2.2.0-2.fc29.riscv64.rpm
--------------------------------------------------------------------------------
Total
Running transaction check
Transaction check succeeded.
Running transaction test
Transaction test succeeded.
Running transaction
  Preparing        :
  Installing       : htop-2.2.0-2.fc29.riscv64
  Running scriptlet: htop-2.2.0-2.fc29.riscv64
  Verifying        : htop-2.2.0-2.fc29.riscv64

Installed:
  htop-2.2.0-2.fc29.riscv64

Complete!
[root@fedora-riscv ~]#
```

FreeRTOS Advancement

- **Low power support**
  - Based on **FreeRTOS tickless-idle mode**
  - Based on RISC-V standard mtime/mtimecmp
  - Reduce power consumption by stopping periodic tick interrupt in the idle mode
- **Pass FreeRTOS testsuite**
- **Support AE250/AE350**

Concluding Remarks

Concluding Remarks

- **FREE RISC or RISK FREE**
- **Any viable vendor must focus on its main products**
- **Andes is committed to serve demands for RISC-V SoCs**
  - Strong processor IP offerings
  - Comprehensive development tools and SW
  - Solutions from close partners and RISC-V ecosystem
- **Andes V5 cores are used in diversified applications:**
  - AI, FPGA, IoT, MCU, Security, Storage, Wireless

Andes: Trusted Computing Expert and Your Best RISC-V Partner !

Thank You !!