



Powering RISC-V SoC with 1 to 1000s Cores

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**RISC-V CON SILICON VALLEY
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Agenda



- Andes RISC-V (V5) Business Status
- Andes V5 Products
- Andes Custom Extensions™ (ACE)
- Summary



Andes RISC-V (V5) Business Status

Tier-One Adoptions of RISC-V

Qualcomm Technologies, Inc., will be shipping RISC-V in product in

- Customers have strong requirement on differentiation of Sensor Hub

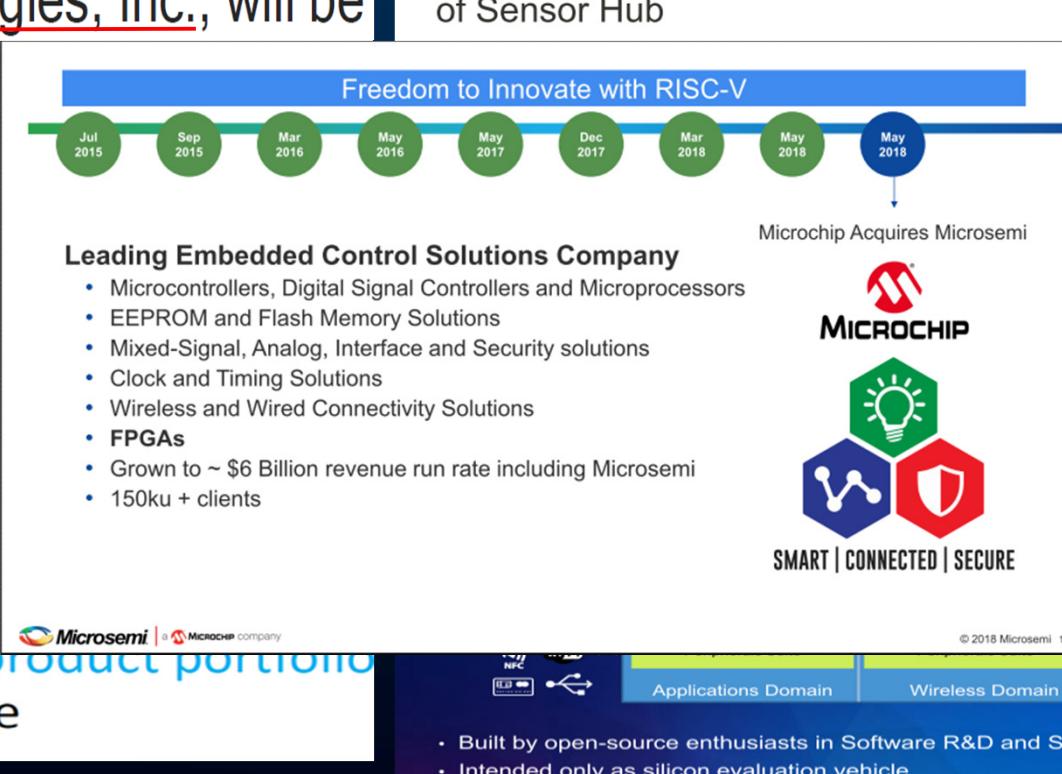
Page 14 in Unleashing Innovation from Core-to-Edge-Martin-Fink

DRIVING MOM

Western Digital shipped **1 Billion** cores p

...and we expect to

Transitioning our product portfolio to **RISC-V** over time



Taking RISC-V® Mainstream

RISC-V 4

Andes Advancement: V1-V3 to V5

■ Founded in 2005 as a pure-play CPU IP company

- Core R&D team from AMD, DEC, Intel, MIPS, nVidia, and Sun
- Developed our own patented ISA **AndeStar™ V1/V2/V3**
- Upstreamed GNU toolchain and Linux kernel
- High-volume shipment from a large number of licensees worldwide
- Healthy growth



■ 2014: Noticed the existence of RISC-V

■ 2015: Paid more attention, started playing with RISC-V GCC

■ 2016: Joined the RISC-V Foundation as a founding member

■ 2017: Announced the adoption of RISC-V as AndeStar V5

■ 2018: Released first V5 families

■ 2019: Released RVP and multicore support, and ...





V5 Adoptions: From Edge to Cloud

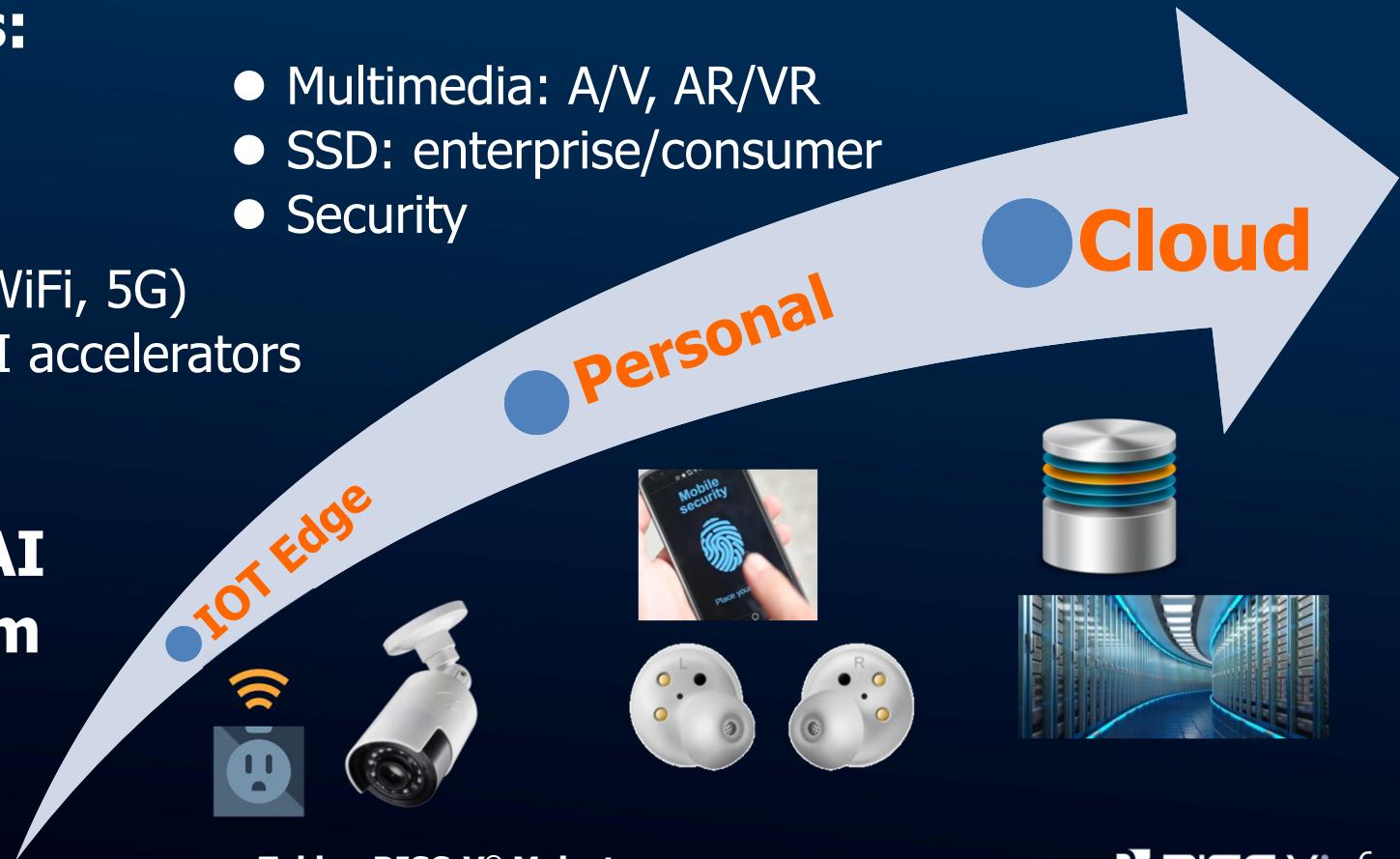


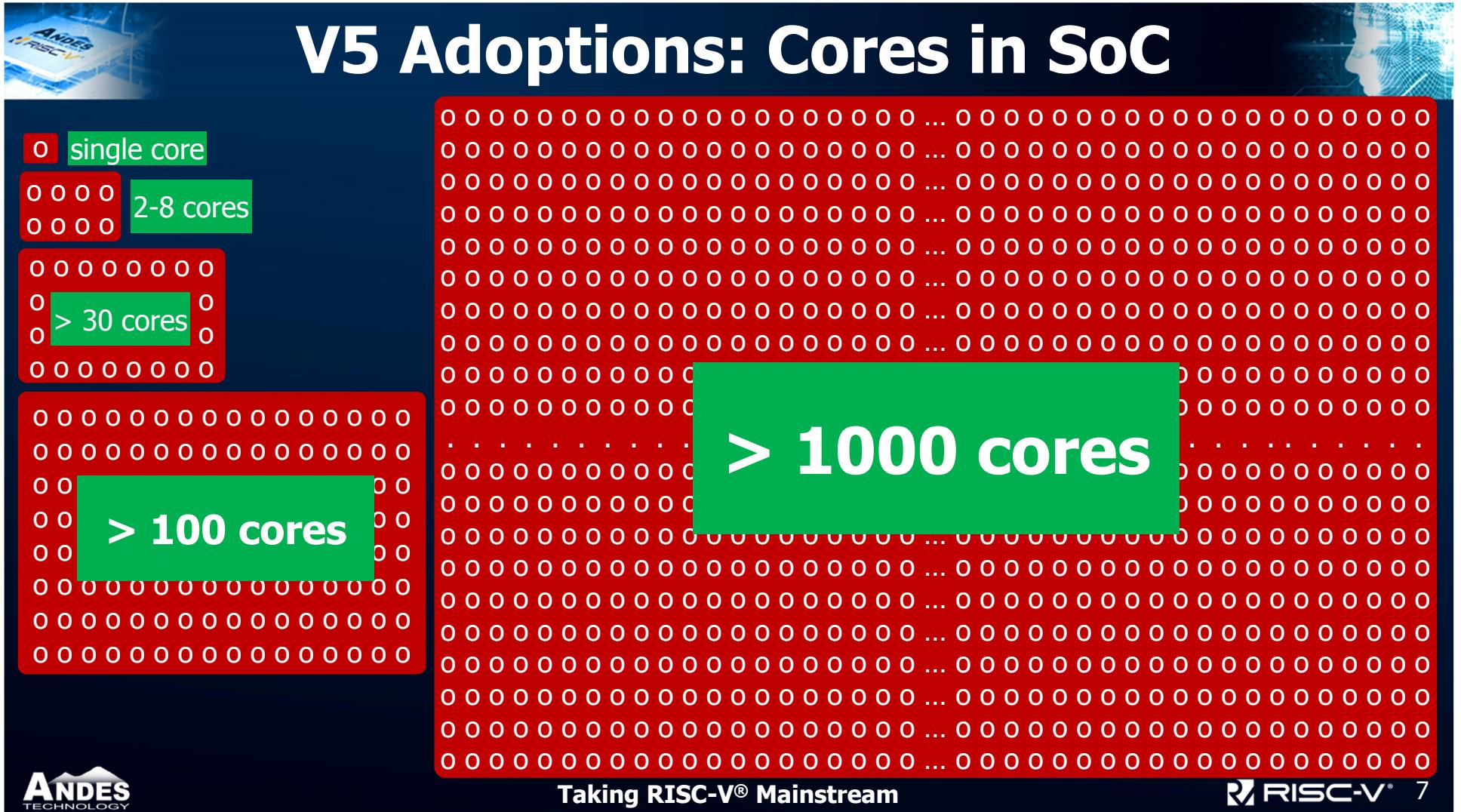
■ Applications:

- ADAS
- AIoT
- Blockchain
- Comm. (BT, WiFi, 5G)
- Datacenter AI accelerators
- FPGA
- MCU
- Multimedia: A/V, AR/VR
- SSD: enterprise/consumer
- Security

■ ~50% use AI

■ 40nm to 7nm





Highlight of Partnership

- Development Tools
- Runtime
- Security



Tested Targets



QEMU for AndeStar V5 &&
AndeShape Development Platform ADP-XC7KFF676

Fedora Images can run on the QEMU and
AndeShape FPGA board



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ANDES
TECHNOLOGY



Highlight of Developer Programs

■ AndeSight™ IDE Free Download

- Compiler, debugger, full-featured IDE and AndeSim™ simulator

■ RISC-V FreeStart Program

- RTL for free evaluation
- Commercial license with no license fee for AndesCore™ N22

■ RISC-V EasyStart Program

- Enable (15) design service partners to serve RISC-V customers better



Andes RISC-V Products



Taking RISC-V® Mainstream

RISC-V® 10

AndeStar™ V5: Best Extensions to RISC-V

V5= RISC-V + Andes Extensions

■ Andes Baseline Extensions:

- Baseline ISA extensions
- HW features for embedded systems
 - ◆ HW-handled misaligned load/store
 - ◆ Vector interrupt controller with priority-based preemption
 - ◆ Cache management features
 - ◆ StackSafe™: stack protection
 - ◆ QuickNap™, PowerBrake: power management

■ Andes Custom Extensions™ (ACE)

- Offer powerful tools to design custom instructions for acceleration:
 - ◆ No CPU background required
- Enable RISC-V for broader market

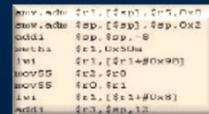


Andes V5 Product Overview

Highly optimized
designs with
leading

AndesCore™
Processors

Best extensions to RISC-V
AndeStar™ Architecture V5



AndeSight™ Tools
Professional IDE
Integrated code

Most Comprehensive RISC-V Offerings
based on 14-year development

Handy peripheral
IPs to speed up
SoC construction



AndeShape™ Platforms



Extensive SW stacks
from bare metal,
RTOS to Linux



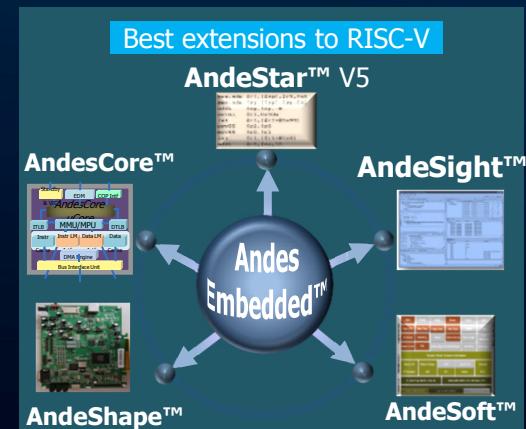
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RISC-V 12



Benefits of Andes V5 Solutions

- 20% better per-MHz performance
- 12% smaller code size for CSiBE due to CoDense™
- 15-20% higher frequency with slightly smaller gate count
- Rich and efficient support for embedded systems
- Efficient accesses on near and far memory
- Strong data processing support: SIMD, ACE, ...
- Flexible configurations supported by tools
- CAD tool friendly RTL
- Experienced support engineering





Andes V5 Processors

New products on the horizon

Cache-Coherent
Multicores

A25MP

1/2/4 **A25**, L2\$,
L1/IO coherence

AX25MP

1/2/4 **AX25**, L2\$,
L1/IO Coherence

Linux
with FPU/DSP

A25

N25F, MMU, DSP

AX25

NX25F, MMU, DSP

Fast/Compact
with FPU/DSP

N25F/D25F

V5/32b, FPU, PMP,
DSP (**D25F**)

NX25F

V5/64b, FPU, PMP

Slim and
Efficient

N22

V5[e]/32b
32/16 GPR

\$ / LM, BrPred, Custom Instr.

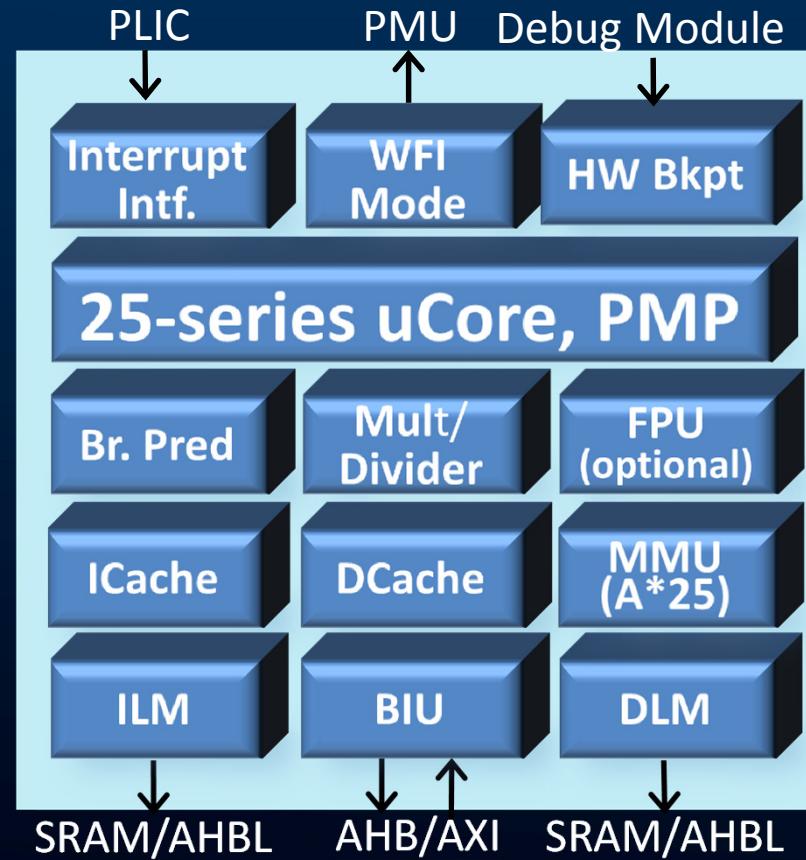
5-stage
RV*GCP

2-stage
RV32IMAC



AndesCore 25-Series

- 32-bit and 64-bit cores
- AndeStar V5 architecture:
 - RV-IMAC + Andes V5 Extensions
 - Optional: F/D and S-mode/MMU
- 5-stage pipeline, single-issue
- Configurable multiplier
- Optional branch prediction
- I/D caches and Local Memory
 - Optional parity or ECC protection
 - Hit-under-miss caches
 - HW unaligned load/store accesses
- Bus interface
 - 1 or 2 master ports (AHB/AXI)
 - An optional slave port (AHB)



25-Series: Performance

Features	Base	FP	Linux	Linux
32KB I\$/D\$ + 256 BTB	Yes	Yes	Yes	Yes
SP/DP FPU	--	Yes	Yes	Yes
MMU and S-Mode	--	--	Yes	Yes
RV-P ext. draft (DSP)	--	--	--	Yes
Worst-Case Freq. (GHz) ¹	1.2	1.2	1.2	1.1
Coremark/MHz ²	3.57 (rv32), 3.53 (rv64)			
DMIPS/MHz ²	1.97 (rv32), 2.13 (rv64)			

1: 28nm SVT 9T library and high-speed memory. Frequency at 0.81v/-40°C.
 2: AndeSight v320 toolchain; DMIPS/ground rule uses no-inline option.

■ Linux support

- RISC-V MMU and S-mode
 - ◆ SV{32,39,48}, all page sizes
- 4-way 32~128-entry STLB
- 4 or 8-entry ITLB and DTLB

■ FPU (RV-F or RV-FD)

- +, -, ×, ×+, ×-:
 - ◆ pipelined 5 cycles
- ÷, √ : run in background
 - ◆ SP: 15 cycles, DP: 29 cycles





First RISC-V Cores with RV-P



■ P-Extension ISA for efficient SIMD/DSP (based on XRF)

$$32 = 32 + 8 \times 8 + 8 \times 8 + 8 \times 8 + 8 \times 8$$

RV32 performs one set of the above; RV64 performs 2 independent sets

- lists.riscv.org/g/tech-p-ext/files/Specification/P-ext-proposal-v0.5.1-20191008.pdf

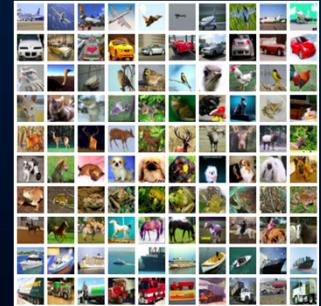
■ Speedups on 32-bit V5 cores

- MP3 decoder: **2.0x**
- AMR voice codec: **3.7x**
- **Keyword Spotting** (Tensorflow model): **5.2x**
- >200 DSP libraries: **5.2x / 1.8x** for max./avg.

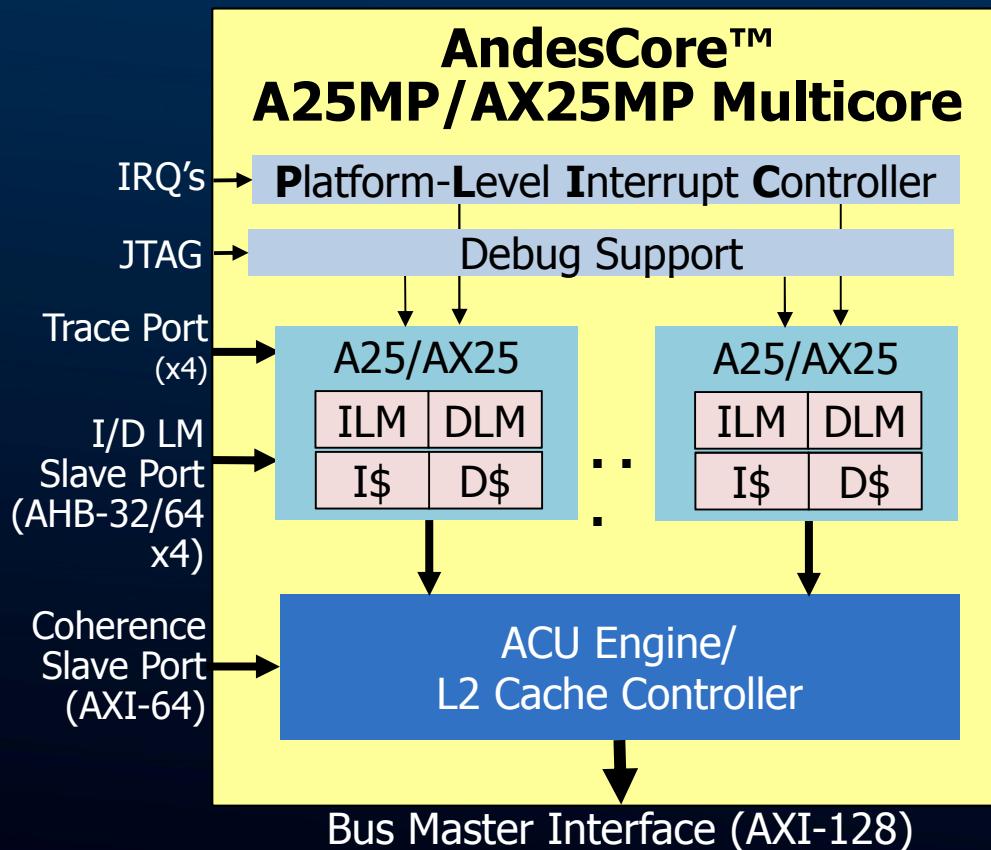


■ Speedups on 64-bit V5 cores:

- Image classification (CIFAR10): **11x**
- Face detection (P-net): **7.6x**
- >200 DSP libraries: **11x / 2.5x** for max./avg.



A(X)25MP: Cache-Coherent Multicore

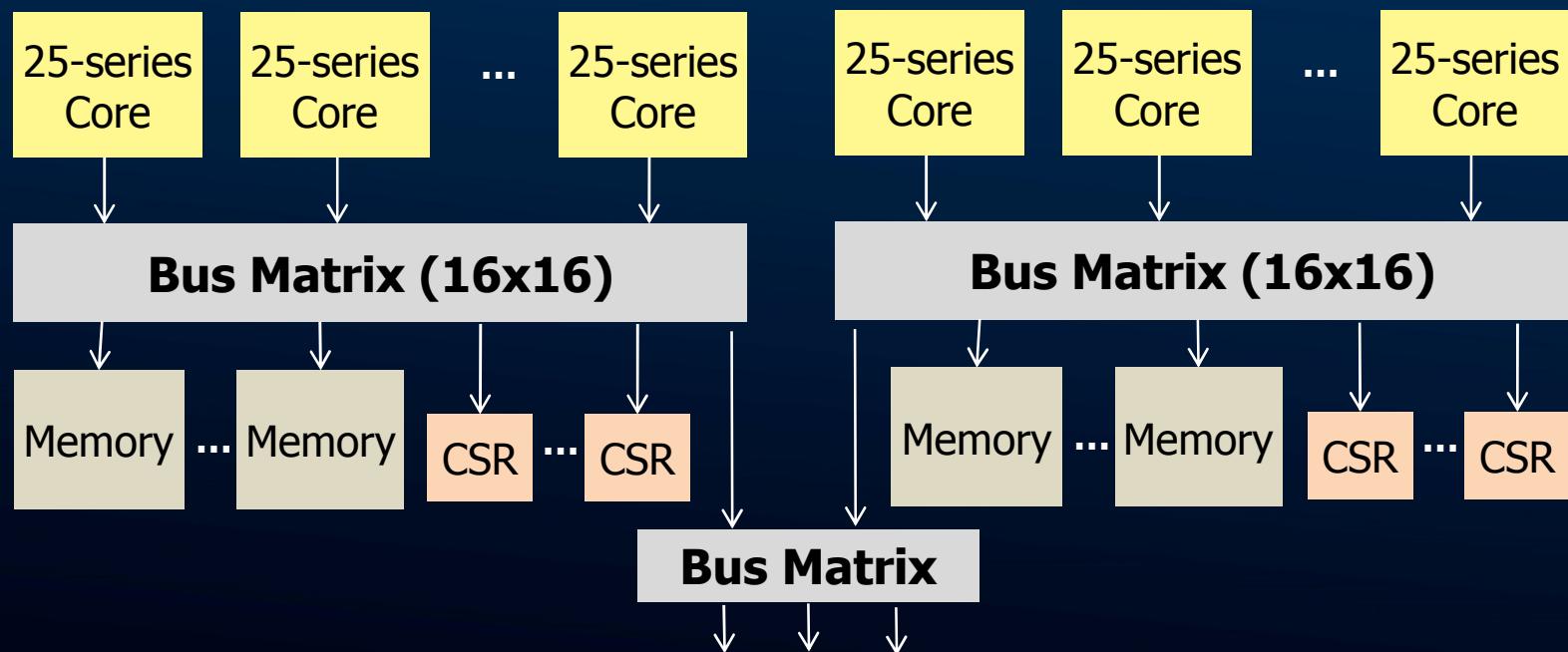


- **1~4 A25/AX25 CPUs:**
 - RV-GCNP + V5 extensions
 - Supporting SMP Linux
- **Dcache coherence with duplicated tags**
- **IO coherence port**
- **L2 cache controller**
 - 16-way with bank interleaving
 - I/D prefetch
 - Flexible SRAM timing
- **PLIC for interrupt handling**
- **Debug/trace support**



Memory Hierarchy for Multi-CPUs

- Medium scale of processors





Andes Custom Extensions™ (ACE) to boost performance, efficiency and security

(Thanks ARM for finally recognizing the importance)



Taking RISC-V® Mainstream

RISC-V® 20

Accelerating Data-Intensive Computation

■ Two parts:

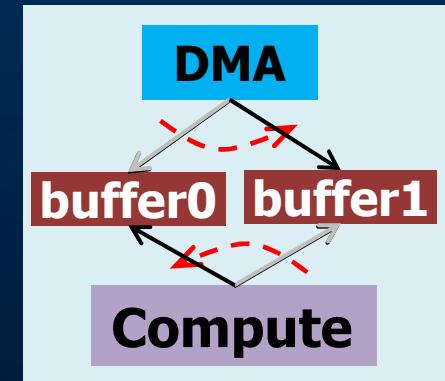
- Data IO
- Compute Acceleration

■ Data IO: DMA with double buffers

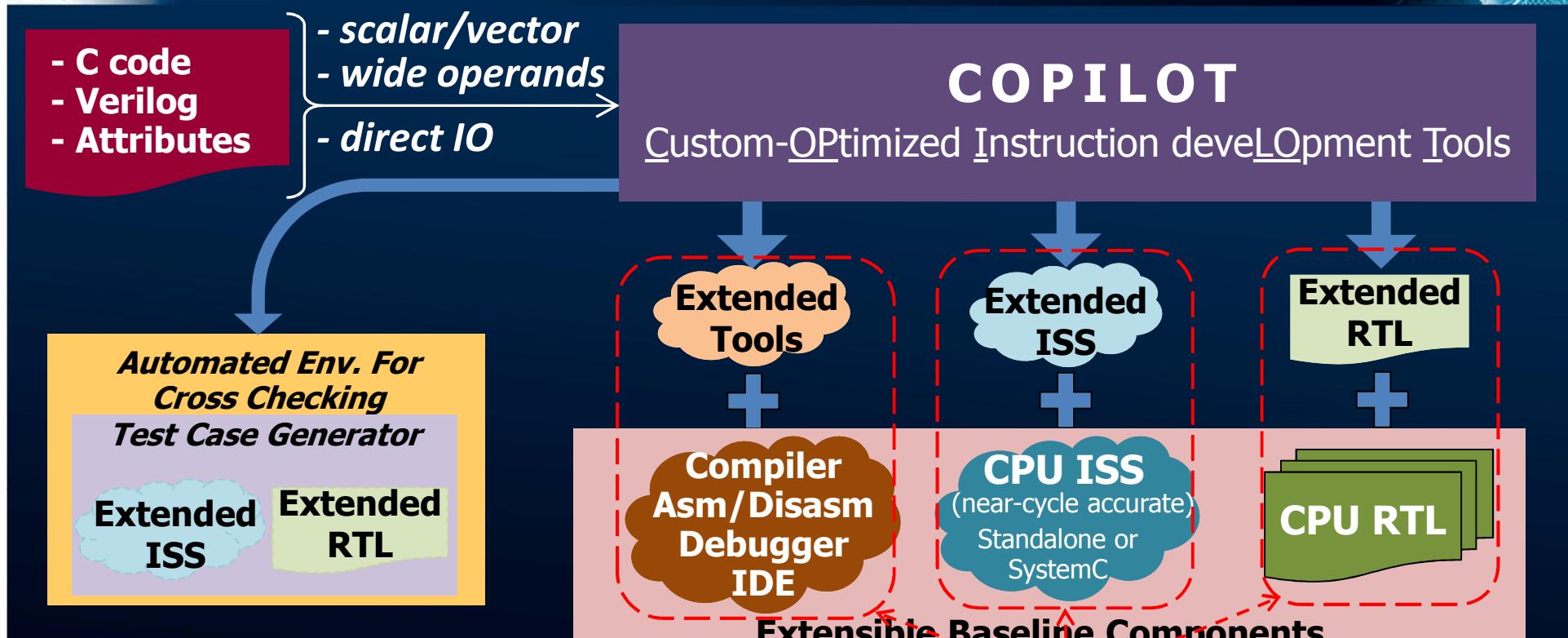
- Switch buffers on phase changes

■ Compute Acceleration: ACE

1. ACE to perform Computation. E.g.
 - ◆ Dot products of 2 64x8 vectors
 - ◆ Matrix convolution
2. ACE to control existing HW Engine. E.g.
 - ◆ Sending 90-bit commands in one cycle



Andes Custom Extension™ For DSA





Summary of ACE Features

Items	Description	
Operands	standard	immediate, GPR, baseline memory (thru CPU)
	custom	<ul style="list-style-type: none"> • ACR, ACM, ACP (ACE Register, Memory, Port) <ul style="list-style-type: none"> -- With an arbitrary width and number • ACR operands can be “implied” to save opcode
Instructions	scalar	single-cycle, or multi-cycle
	vector	for loop, or do-while loop
	background option	retire immediately, and continue execution in the background. Applicable to scalar and vector.
Auto Generation	<ul style="list-style-type: none"> - Opcode assignment: automatic based on <u>bits required for operands</u> - All required tools, and simulator (C or SystemC) - RTL code for instruction decoding, operand mapping, dependence checking, input accesses, output updates - Waveform control file 	
Fast turnaround time !		



■ Eclipse-based, enriched by 14-year effort

The screenshot displays the AndeSight IDE interface with several open windows:

- SoC Registers:** Shows memory map details for cr2 (DCM_CFG) and cr3 (MMU_CFG). A green arrow points from the cr3 section to the FreeRTOS Task List window.
- gprof:** A performance analysis tool showing samples and %Time for various functions. Functions include jdctint.c, jpeg_idct_islow, jdhuff.c, jpeg_color.c, ycc_rgb_convert, and build_ycc_rgb_table. The top row shows Summary, jdctint.c, jpeg_idct_islow, jdhuff.c, jpeg_color.c, and ycc_rgb_convert.
- Available Items:** A sidebar listing sections like USER_SECTIONS, LOAD_ROM, EXEC_ROM, Input Sections, ADDR, LOADADDR, STACK, VAR, ALIGN, and Group Input Section Pattern.
- Sections:** A list of memory sections including USER_SECTIONS, FLASH, EXEC, VAR, SDRAM, and stack details.
- FreeRTOS Task List:** Shows tasks like TaskWav, IDLE, TaskEmp, and DMA BH with their status (Running, Ready, Blocked, Suspended).
- FreeRTOS Event List:** Shows event queues with their addresses, item sizes, and waiting counts.
- ADC Analysis:** A waveform plot showing analog-to-digital conversion over time.
- Source Code Editor:** Displays the `djpeg.c` file with code related to JPEG processing.
- Function Code Size:** A report showing the total function code size (46928) and a list of functions with their sizes and paths.



Andes RISC-V Serving Emerging SoC from Edge to Cloud

Performance

- Leading PPA and smallest code size
- First to have complete SIMD/DSP instructions

Configurability & Extensibility

- Flexible configurations on rich features
- Tools to simplify design of custom instructions

Maturity

- Optimizations of compiler, and SW stacks
- Comprehensive features of IDE
- Product packages and custom engineering



Andes
Website



Thank you