

晶心科技

法人說明會 報告

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發言人

113年3月4日



投資安全聲明

除本文包含的歷史資訊外，本演示文稿中涉及的事項均為前瞻性陳述，涉及某些可能導致實際結果出現重大差異的風險和不確定性，包括但不限於天氣、競爭產品和定價的影響、半導體產品供需的全行業變化、快速的技術變革、半導體行業週期、和一般經濟狀況。

除法律要求外，晶心不承擔因新資訊、未來事件或其他原因而更新任何前瞻性陳述的義務。



報告標題

- 晶心公司簡介
- 財務與經營狀況
- 關鍵應用與趨勢
- 研發暨技術能量



晶心科技公司簡介

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數超過500人；80%為工程師。
- 獲得TSMC 2015年新的 IP OIP Award 。
- 晉升為RISC-V國際聯盟(前身為RISC-V基金會) 首席會員。(2020)
- 獲得AI Global Media頒發「2020年最傑出嵌入式處理器IP供應商」。
- EE Awards亞洲金選獎 - 「Taiwan 產品獎」, 「Asia 企業獎」(2021)
- 2023亞太區 前五百大高成長企業

晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

晶心利基

- 智能及環保之電子設備
- 雲端應用,人工智慧及物聯網

晶心科技公司現況

晶心科技指標性資訊

19 Years

Pureplay CPU vendor

500+

Employee , > 80% R&D

400+ Customers

Licensing AndesCore™

14Bn+ SoC

Total Customer Shipment

2023年營運數字

Revenue \$ Growth

1.04 Bn, NT\$

13.5% YoY

License \$ Growth

18.3% YoY

Royalty \$ Growth

-1.2% YoY

SoC Shipping Q'ty

2.1Bn

晶心科技參與RISC-V International (RVI) 組織的工作



Founding & Premier Member from 2016



Board of Directors



Chairs/Co-Chairs of Task Groups



Technical Steering Committee



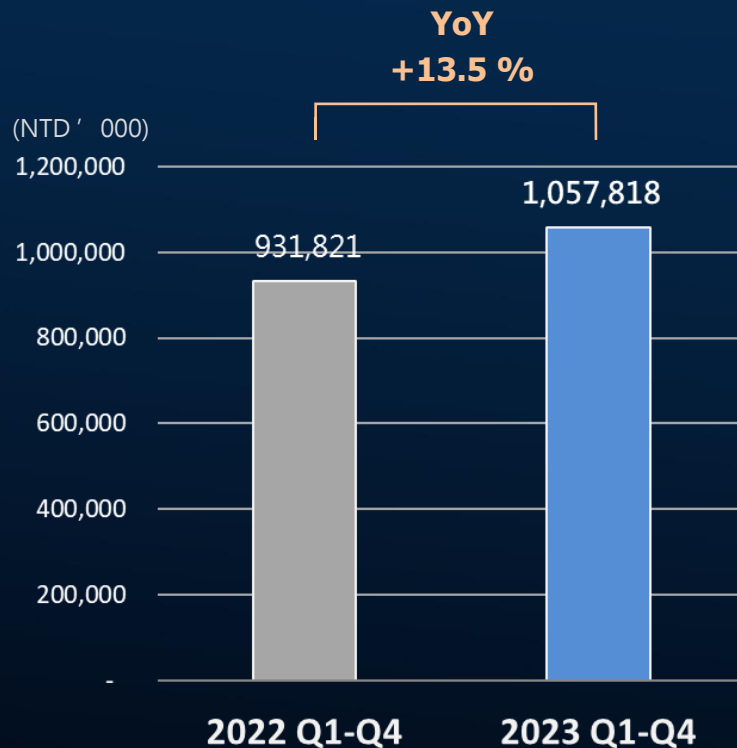
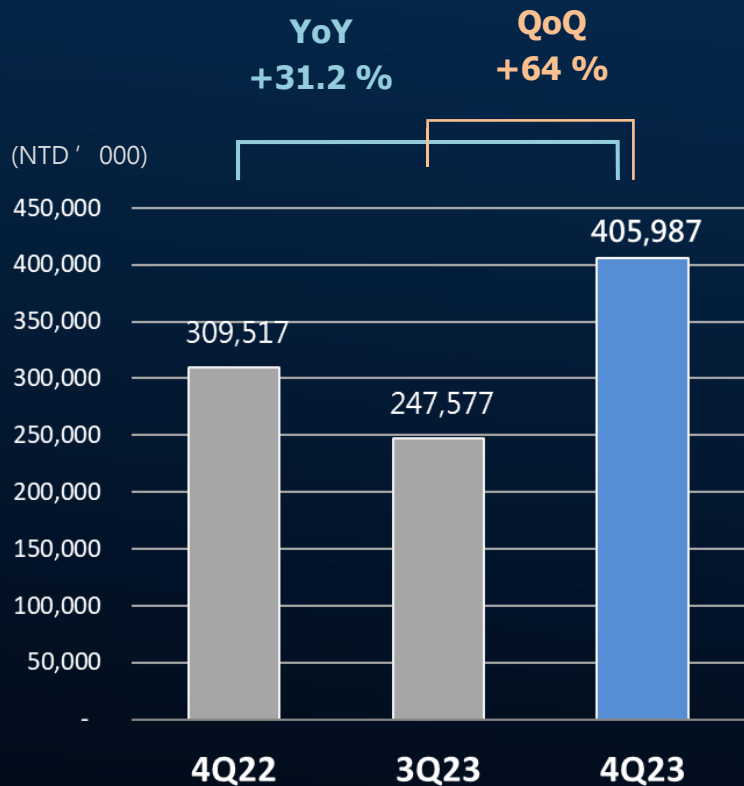
Ambassador



財務與經營狀況



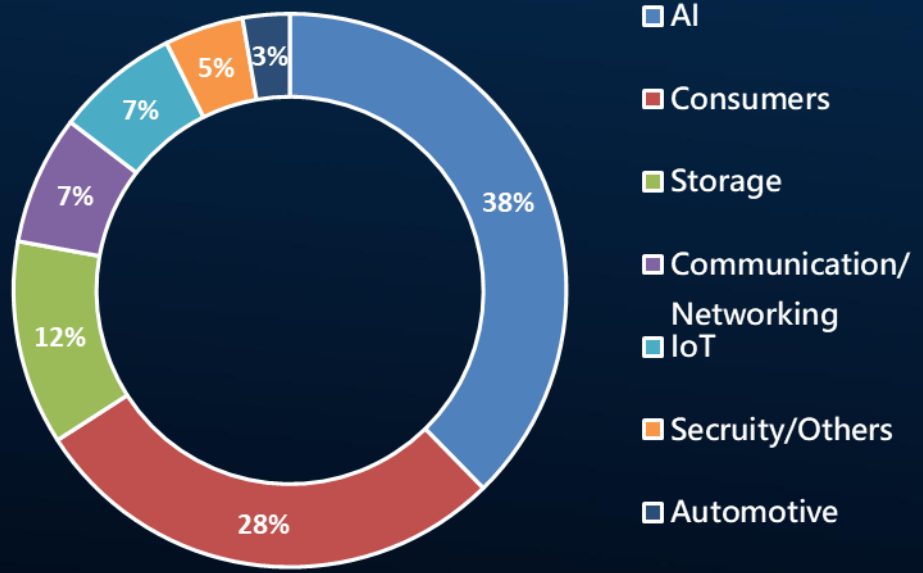
4Q23 整體營收分析





2023 Q1-Q4 營收應用類別分析

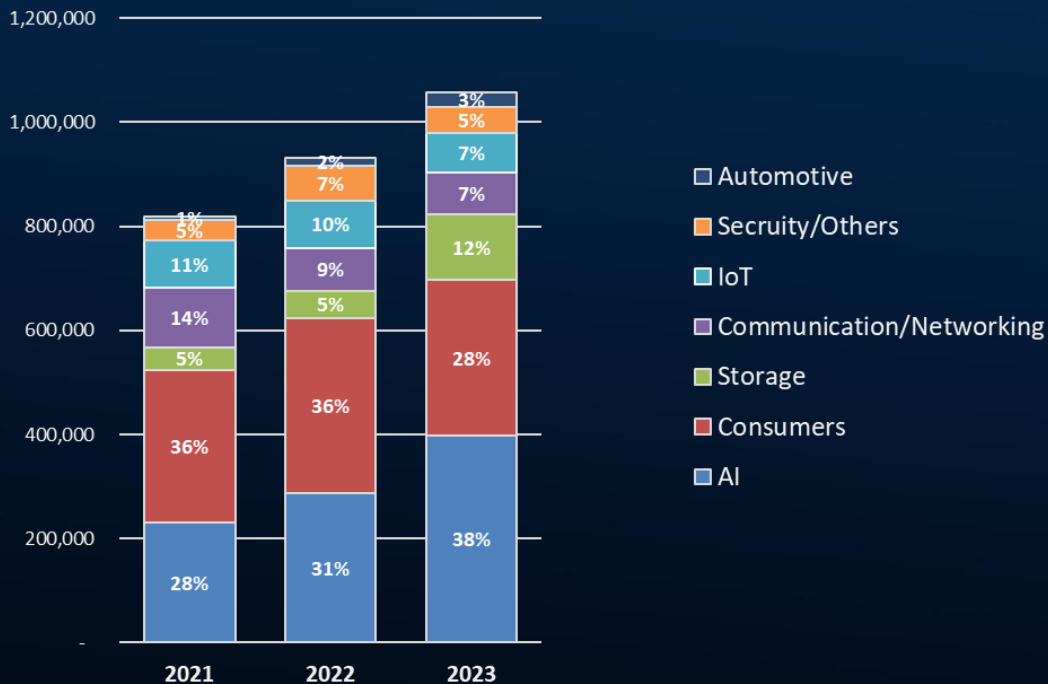
Revenue





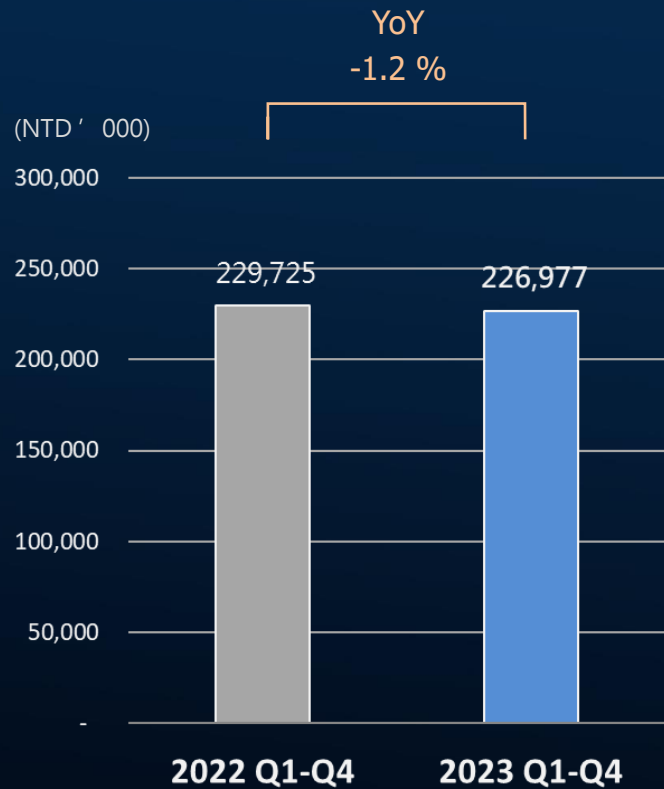
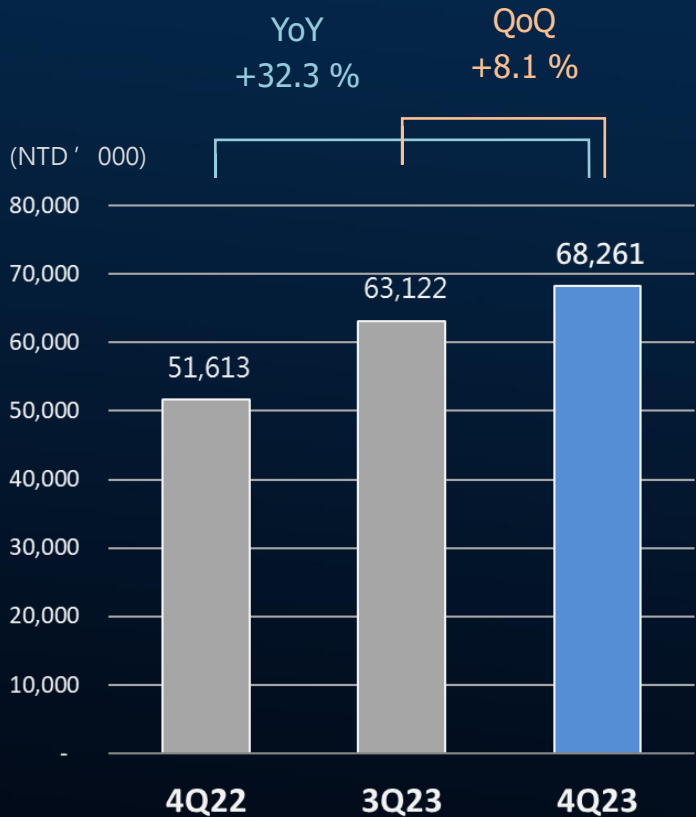
2021 to 2023 營收應用類別分析

(NTD ' 000)

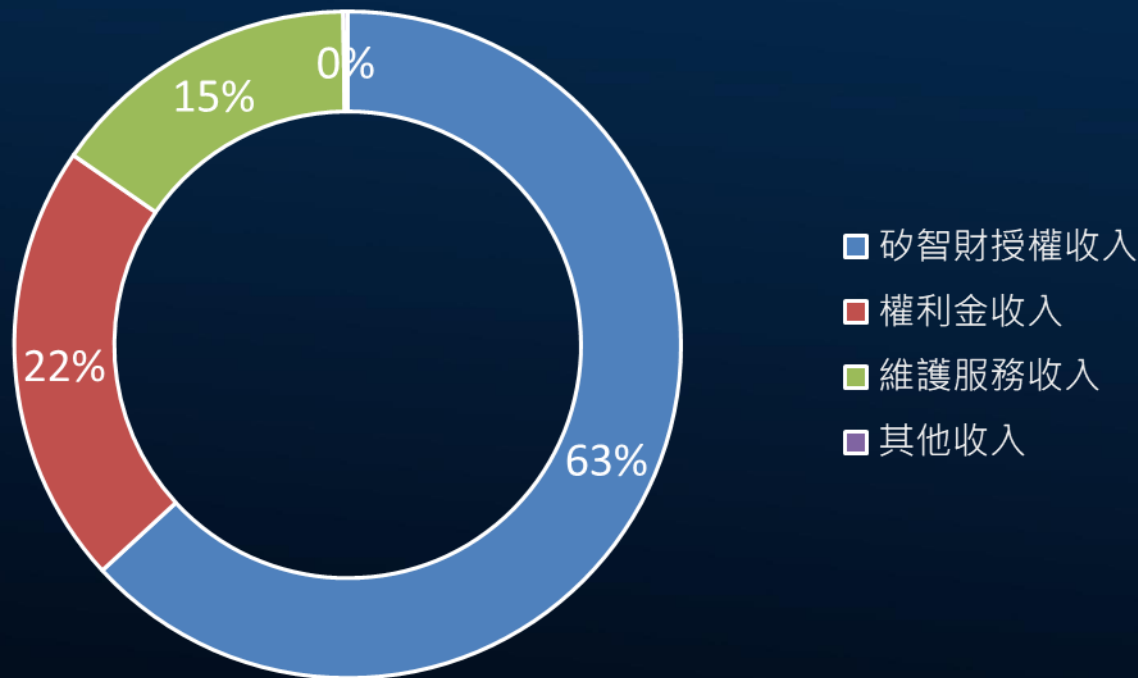




4Q23 權利金收入分析

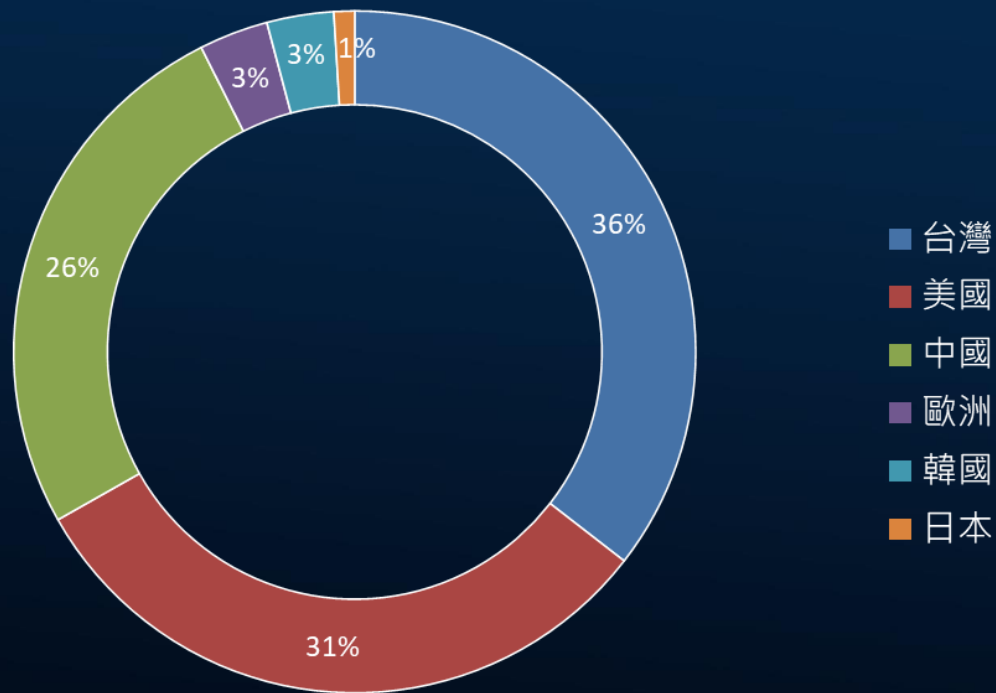


2023 Q1-Q4 營收商業模式分析





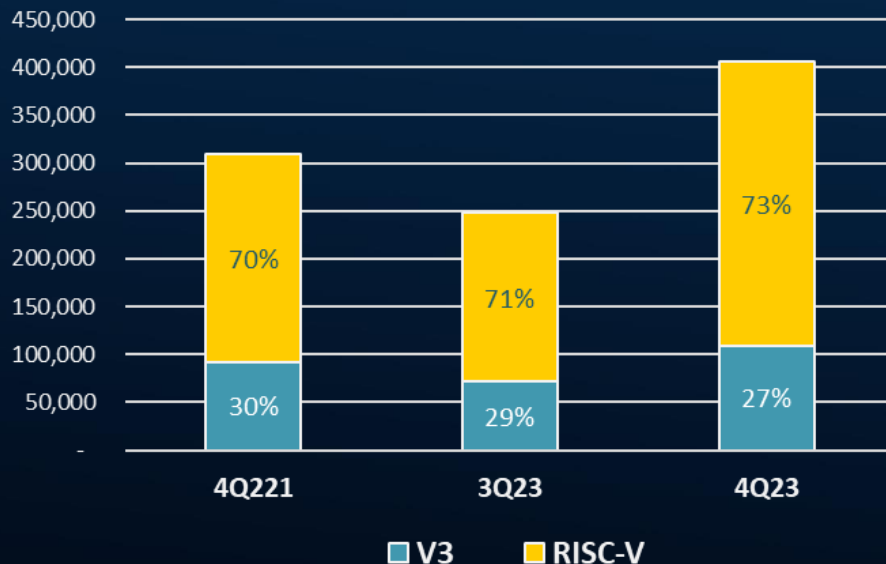
2023 Q1-Q4 地區別營收分析





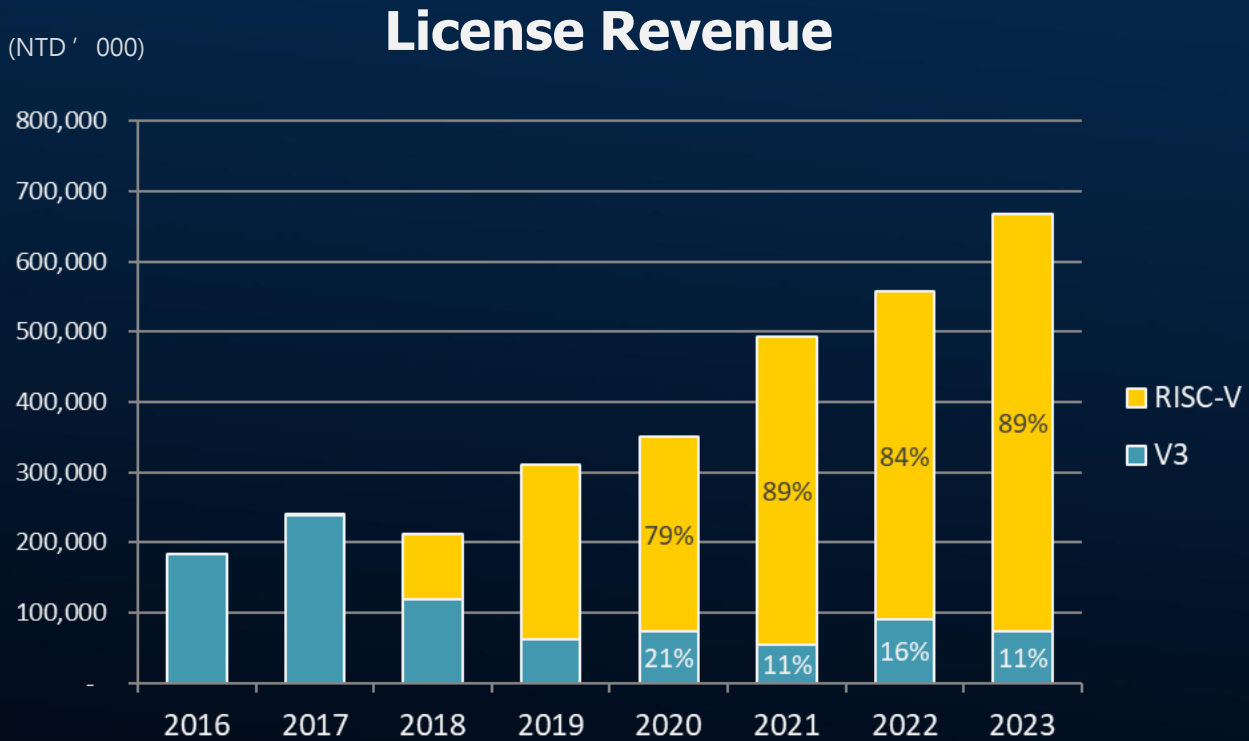
4Q23 RISC-V 營收佔比分析

(NTD ' 000)





歷年授權金收入分析

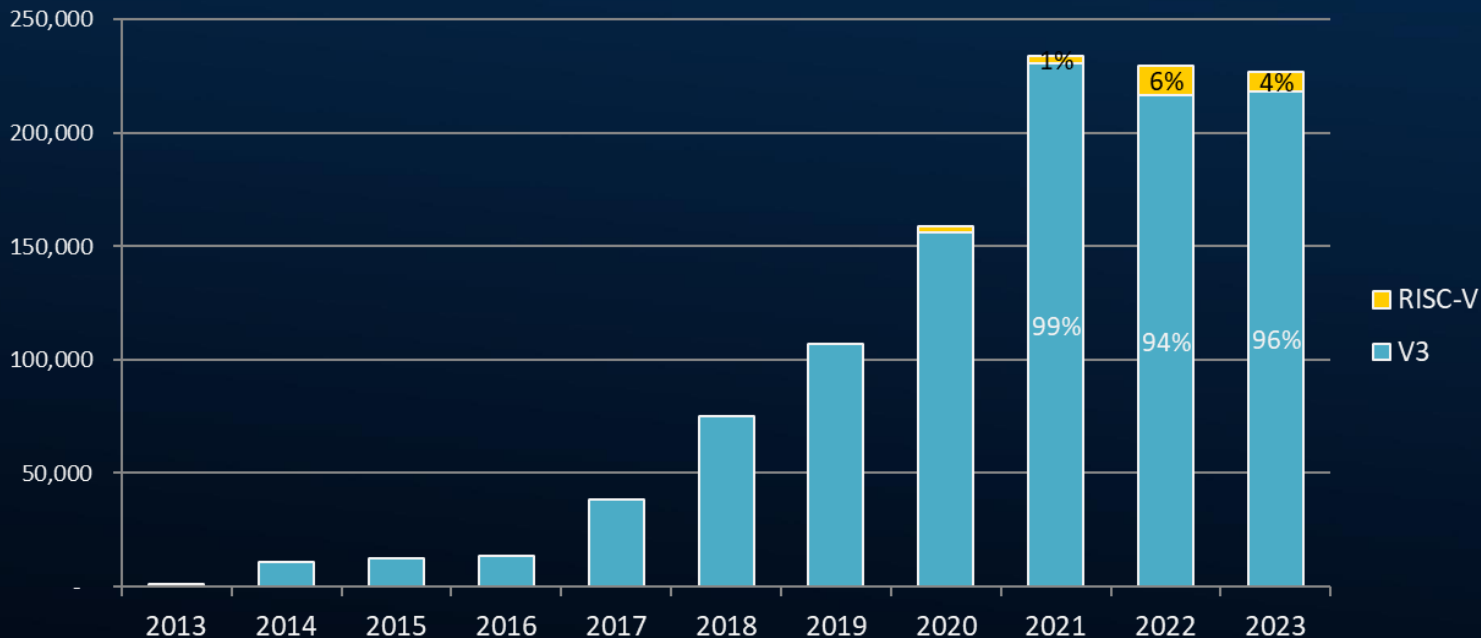




歷年權利金收入分析

Royalty Revenue

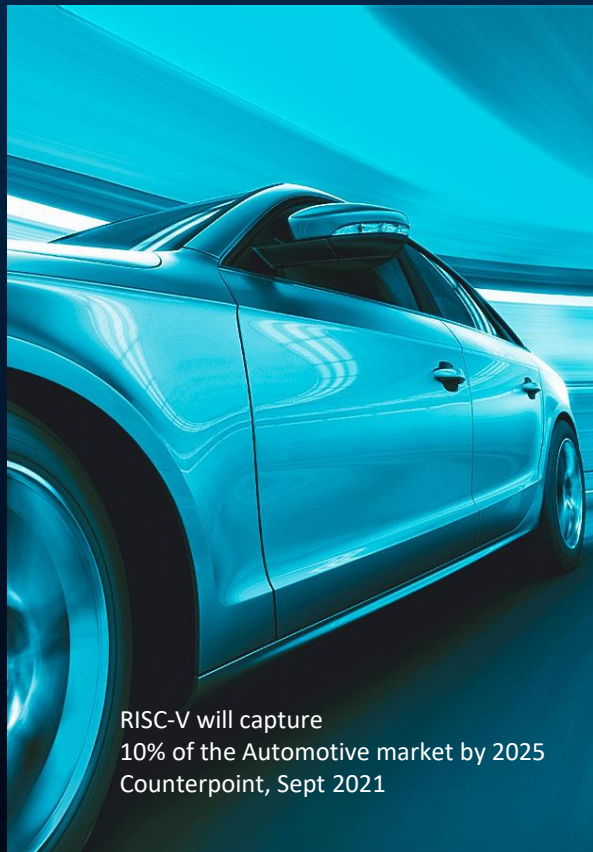
(NTD ' 000)





關鍵應用與趨勢

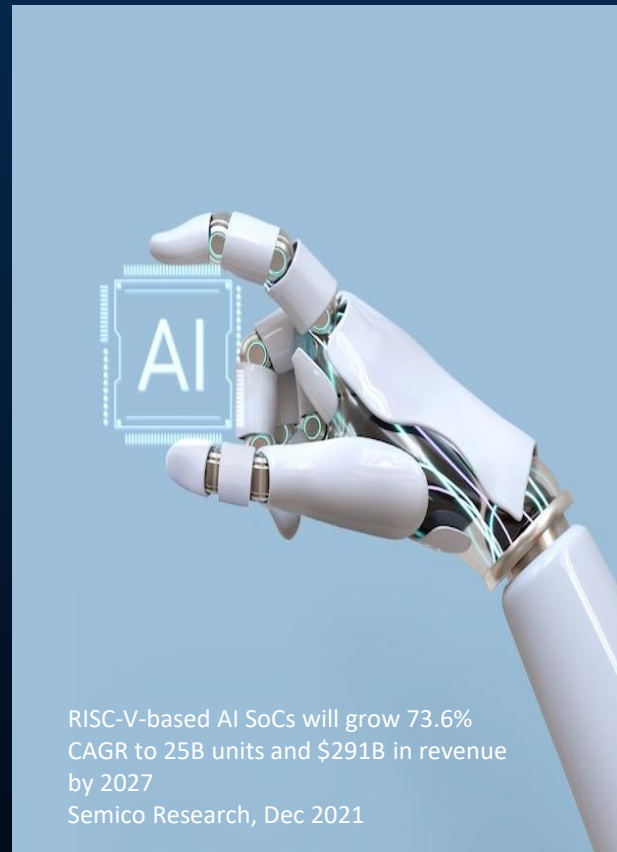
關鍵應用與趨勢



RISC-V will capture
10% of the Automotive market by 2025
Counterpoint, Sept 2021



RISC-V will command 28% of the
IoT market by 2025
Counterpoint, Sept 2021



RISC-V-based AI SoCs will grow 73.6%
CAGR to 25B units and \$291B in revenue
by 2027
Semico Research, Dec 2021

產業領導者引領RISC-V成長勢頭



Leading Semiconductor Industry Players Join Forces to Accelerate RISC-V
Aug. 2023



Renesas Extends Leading RISC-V Embedded Processing Portfolio with New Motor Control ASSP Solution
Sep. 2022



Intel Mobileye EyeQ Ultra RISC-V processor targets Level 4 autonomous driving
Jan. 2022



European processor project shows shift to RISC-V
Dec. 2021



NSITEXE achieves world's first RISC-V processor with vector extension certified for ISO 26262 ASIL D ready product
Aug. 2021



RISC-V crypto core is qualified to ASIL-D for automotive designs
Jan. 2020



Kneron Unveils Its First RISC-V SoC Built for Autonomous, Assisted Driving
Nov. 2021



Andes and IAR Together Enable Leading Vendor ILITEK to Accelerate the Development of its ISO 26262 Ready TDDI SoC ILI6600A
Feb. 2023



Andes and IAR Systems enable leading automotive-focused IC design companies to accelerate time to market
Mar. 2022



Andes Technology and Green Hills Software Team Up to Deliver Advanced Automotive Safety Platform for RISC-V
Aug. 2022



NSITEXE Selects ImperasDV for Automotive Quality RISC-V Processor Functional Design Verification
May 2022



VOSySmonitoRV, a Secure Monitor Layer for RISC-V Architecture Mixed-Critical Systems



Andes Technology and Parasoft Collaborate to Provide Seamless Software Testing Tools for Automotive Functional Safety Applications
Dec. 2022



Andes Technology Collaborates with LDRA to Deliver Integrated Tool Suite for Safety-Critical Software on Andes RISC-V CPU Solutions
Jan. 2023



Upgrade to Solid Sands' latest SuperTest version supports Andes to its ambitions for further growth in the automotive sector
May 2023



晶心科技RISC-V IP支援車用電子

Since founded in March 2005,
Andes Technology is working step-by-step on
RISC-V for ISO 26262 Functional Safety

2016

Andes Joined RISC-V Foundation as one of the Founding Members

- Promoted as Founding Premier Member of RISC-V International in 2019

2017

The First RISC-V Architecture AndesCore™ NX25 and N25 Released

- 25-Series became one of world's most licensed RISC-V CPUs

2020

Andes Development Process Certified for ISO 26262

- Andes became the first ISO 26262 certified RISC-V CPU IP supplier in the world

2022

AndesCore™ N25F-SE Certified for ISO 26262

- N25F-SE became the first full compliant ISO 26262 certified RISC-V CPU in the world



2024

AndesCore™ D25F-SE to be Released

- A series of Andes Functional Safety CPU cores will soon follow



AndesCore™ for Automotive Electronics

■ Supporting a Wide Variety of Functional Safety Applications:

- Dashboard display, in-car monitoring, keyless entry, lighting control, tire pressure monitoring, vision ADAS, microcontroller and many more

■ Developers using AndesCore™ Functional Safety Processors to:

- Introduce new electronic systems on automobiles
- Upgrade existing systems that needs to be ISO 26262 compliant

In-car Monitoring



Head Lights



Keyless Control



Blind Spot Monitor



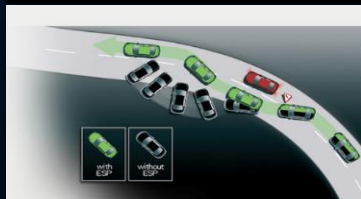
Touch & Display



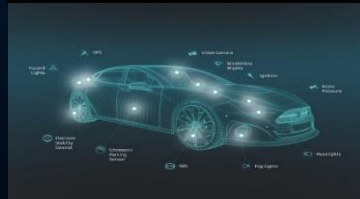
EPS



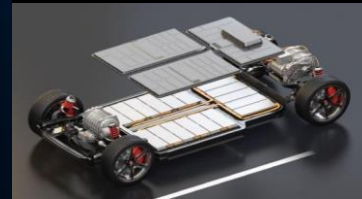
ESC



Sensors & Actuators

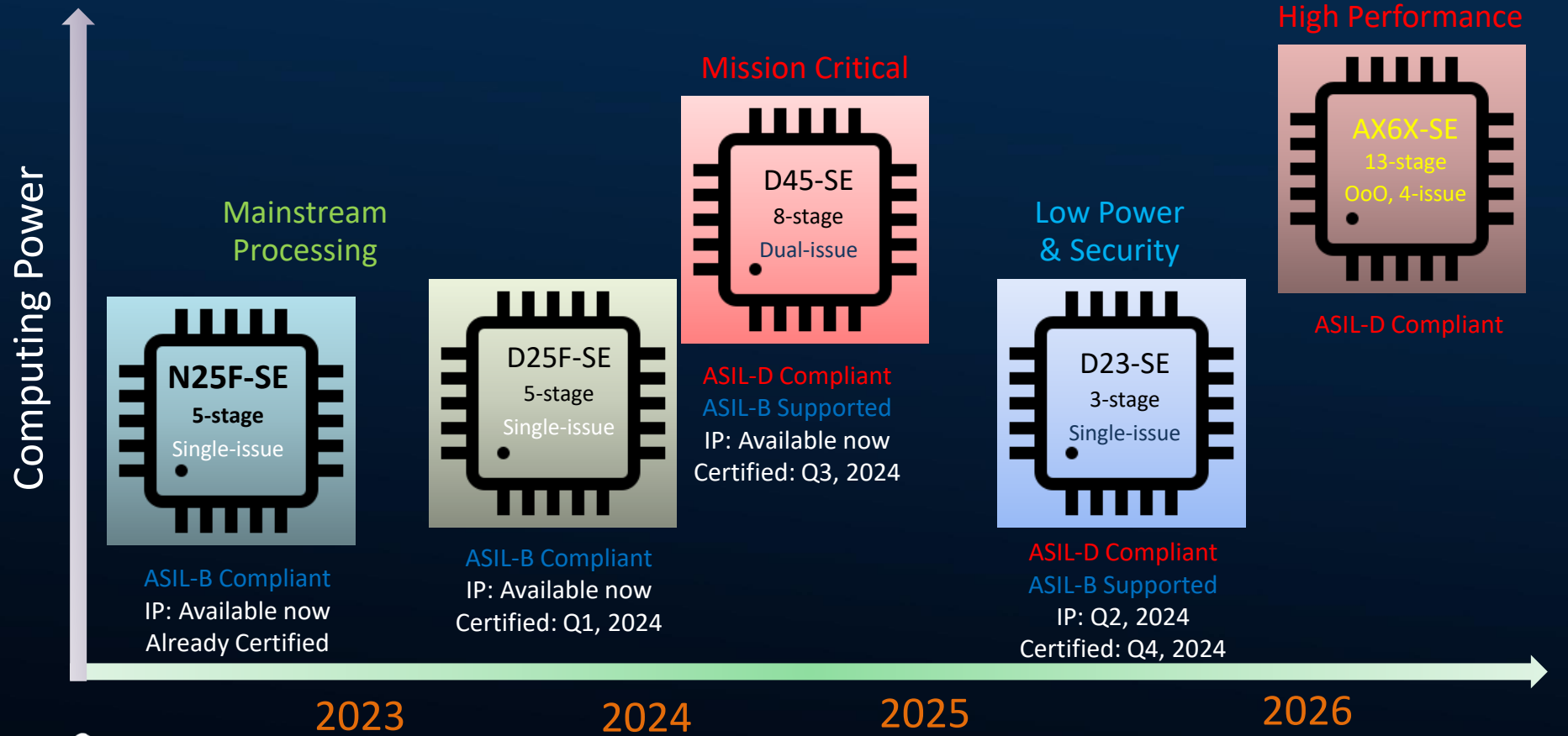


BMS





Andes FUSA Roadmap



晶心科技車用電子生態系統

- Co-working with global leading suppliers in the automotive industry
- Andes and ecosystem partners jointly deliver the trusted RISC-V automotive solutions to designers complying with the standard of functional safety ISO 26262
- Partner Ecosystem Catalogs

Security

Rambus

HSM / RoT

SECURE-IC
THE SECURITY SCIENCE COMPANY

Securizr™ SE

Virtual Open Systems

VOSySmonitoRV

豆荚 BeanPod

TrustKernel

TEE

Safety RTOS



WITTENSTEIN

SAFERTOS

Microsoft

Microsoft Azure RTOS

WINDRV

VxWorks

AUTOSAR

VECTOR

AUTOSAR

SIEMENS

Capital VSTAR
Nucleus SafetyCert

FPG

Fpt Software

MaaZ AUTOSAR

Compiler / Debugger

iar

EWRISCV

Green Hills
SOFTWARE

MULTI IDE / Compiler
RTOS

TASKING

RiscFree IDE/Compiler

ASHLING

Compiler

LAUTERBACH
DEVELOPMENT TOOLS

TRACE32 Debugger

LDRA Tool
ASSURED

LDRA Tool Suite

PARASOFT

Parasoft C/C++ Test

RISC-V for Datacenter & Cloud



RISC-V offers unique
Opportunity for
accelerators



Custom computing for
AI and
other emerging
workloads

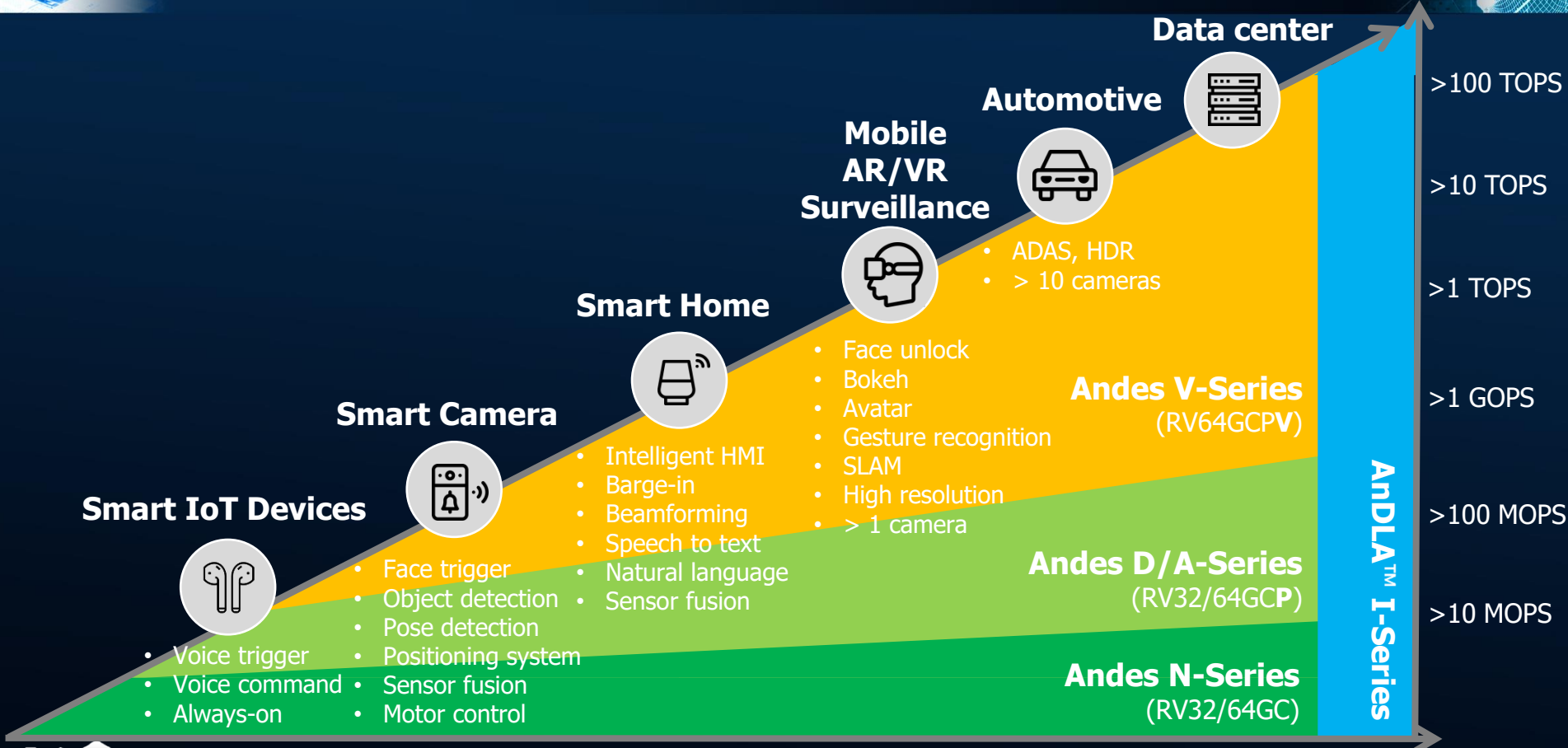


Achieve your
performance and
power targets

RISC-V CPU core market will grow 115% CAGR, capturing > 14% of all CPU cores by 2025



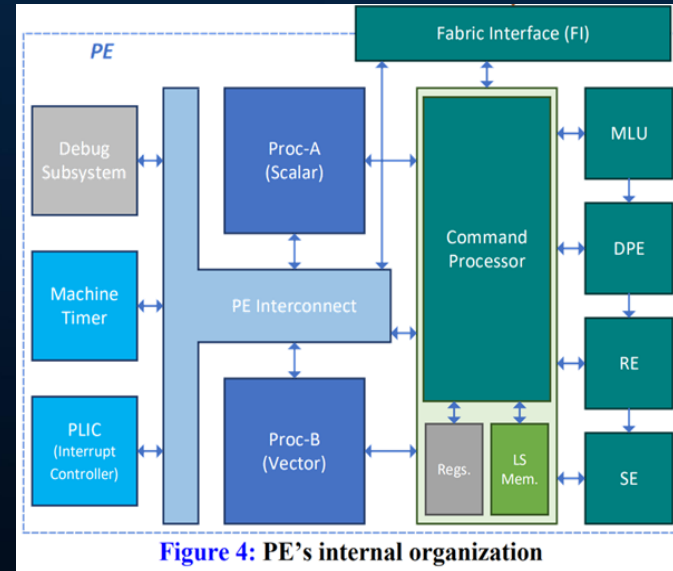
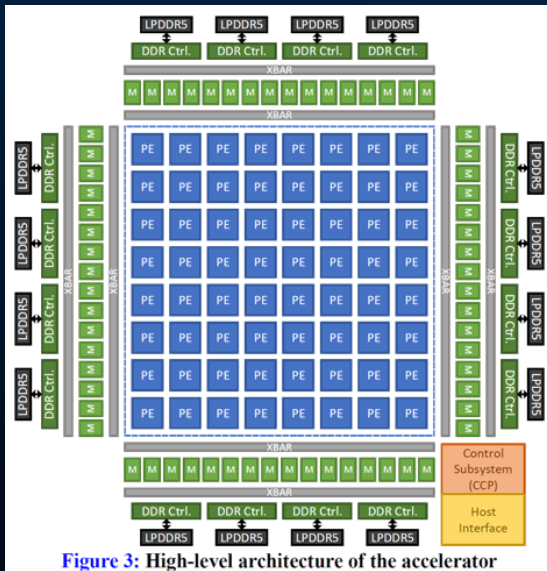
Andes RISC-V Processors to Fit Your AI





MTIA: Meta Training/Inference Accelerator

- ISCA 2023 paper, "MTIA: First Generation Silicon Targeting Meta's Recommendation Systems"
- Proc-A/B: AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models

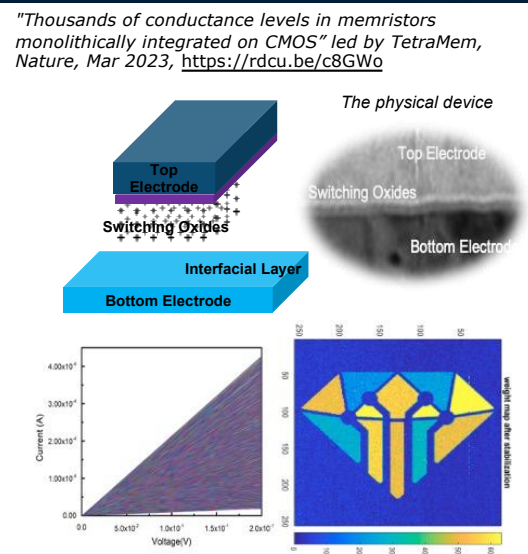


All photos: courtesy of ACM

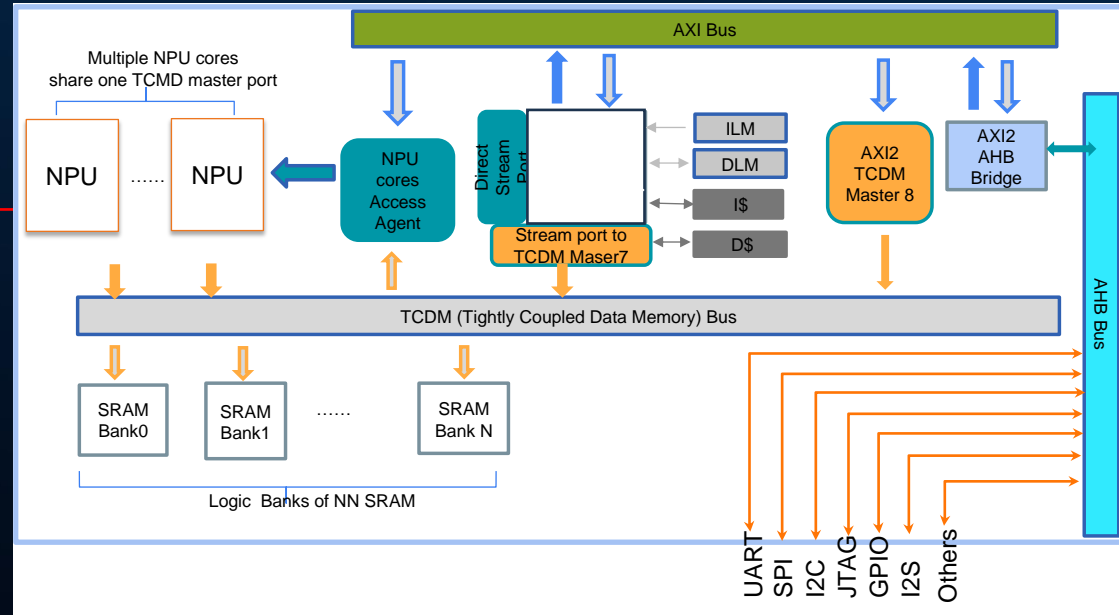


Edge AI With Analog In-Memory Computing

- **TetraMem** Analog In-Memory-Computing MX200 (**RRAM-based**)
- 8-bit 256x256 (**64K**) MAC Engines, **>30 TOPS/W** performance
- ML core operators (conv, gemm) processed in NPU
- Remaining operations processed in RISC-V Vector processors and control CPU



Powered by 8 bits multi-level RRAM device





Endpoint AI

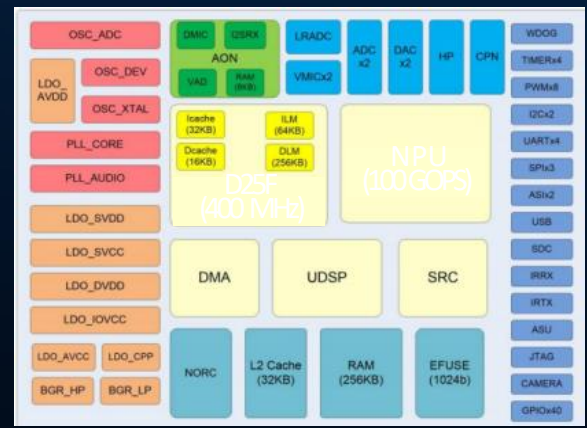
- Renesas R9A06G150 Voice-Control ASSP
 - With **100MHz DSP-capable D25F processor**
 - ML-based voice recognition gets >50% speedup by using P-extension



Voice HMI ASSP 100MHz 32-bit RISC-V with DSP, FP ext.
 V9E32L483V
 10u-10-68F6

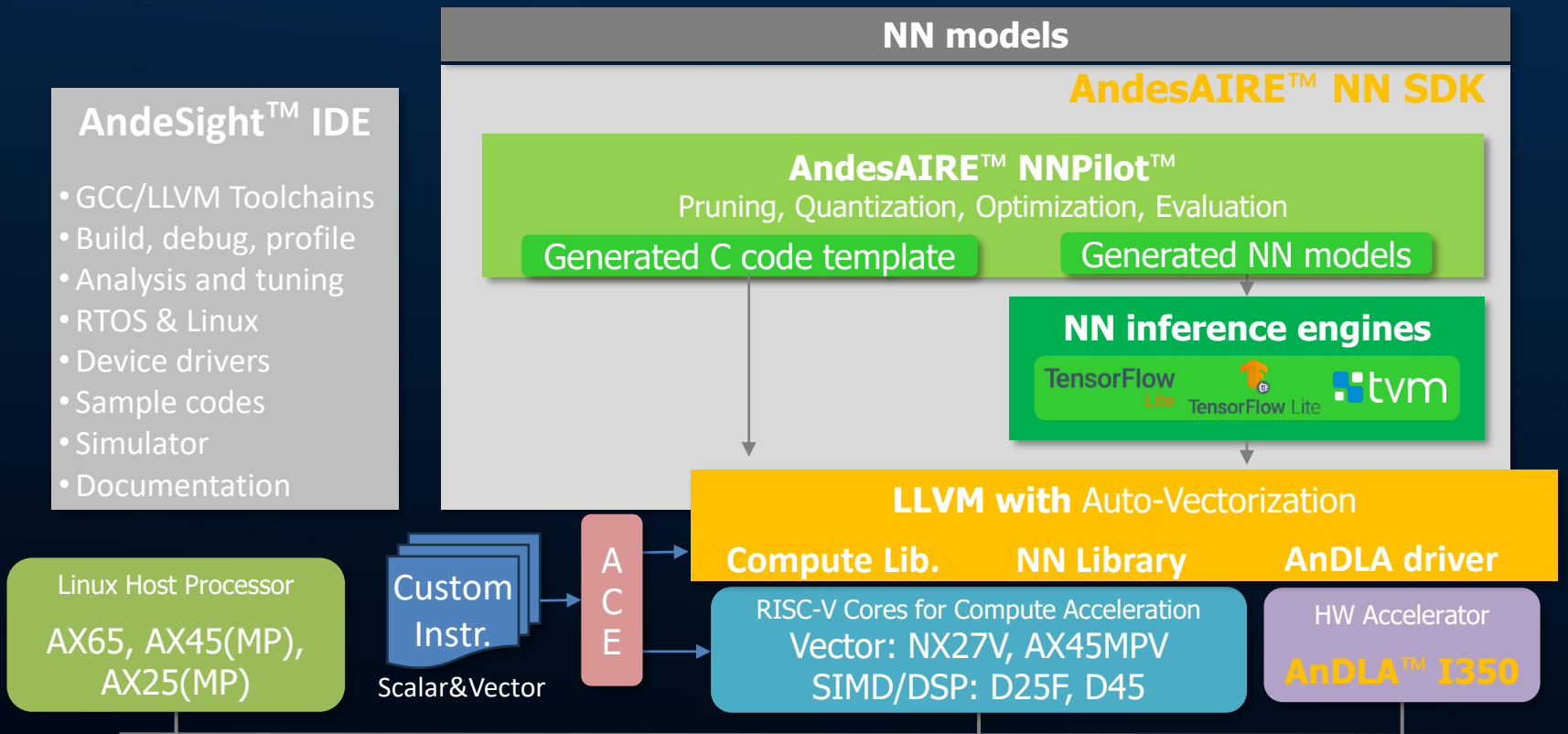
CPU Andes-D25F RV32CMPAF [Extensions] Andes StackSafe, PowerBrake, Recoverable NMI, Branch prediction PMP 16 regions	Memory Code Flash (256 KB) SRAM (128 KB) [w/ 4x32KB power-off] Data Flash (16 KB) Standby SRAM (1 KB) QSPI (1ch)	Analog 12-bit ADC (6ch) w/ 2 SH 12-bit DAC (2ch)	Timers 16-bit GPT (4ch) 32-bit Low Power Timer (4ch) WDT
Communication SCI (2ch) w/ FIFO, Manchester I2C (1ch) SPI (1ch) w/ FIFO PDM (2ch) SSIE (2ch) IRDA (SCID)	System Machine Timer DTC DMA (8ch) On-chip Oscillators (HOCO, MOCO, LOCO) Ext. Oscillator/Clock (MOSC) 32-bit DOC	Safety Bus Master MPU SRAM Parity Check Clock Accuracy Check CRC Calculator IWDG Oscillation Stop Detection	Package QFN 48 QFN 32 QFN 24

- Spacetouch SPV60 Intelligent audio processor
 - High performance for customer development
 - ◆ 100 GOPS NPU for noise reduction, echo cancellation, howling suppression
 - ◆ uDSP for FFT/IFFT, atan, log, etc.
 - ◆ **400MHz D25F with ID caches/Local Memory**
 - Rich audio interfaces and other peripherals
 - Applications:
 - ◆ Intelligent voice, smart earphone, professional audio



AndesAIRE™: Andes AI Runs Everywhere

■ HW/SW Solutions for AI from the Edge to the Cloud



AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera



Smart Sensor



Smart Home Appliance



AIoT / tinyML



Robotics



Wearable





研發暨技術能量



晶心科技 RISC-V CPU Cores



AX60 Series 13-stage OOO Linux MP		AX65	AX66	AX6X-SE	A72~A78; N1/V1/X1
<i>Categories</i>	<i>Power-efficient</i>	<i>Mid-range</i>	<i>Extended</i>	<i>FUSA</i>	
45 Series 8-stage Superscalar	N45, NX45	D45	AX45MPV A45(MP), AX45(MP)	D45-SE	A53/55, R52/ R82, M7
27 Series 5-stage MemBoost		NX27V	A27(L2), AX27(L2)		A5/7/35
25 Series 5-stage Fast&Compact	N25F, NX25F	D25F	A25(MP), AX25(MP)	D25F-SE N25F-SE	A5/7/35, R4/5, M4/33
Compact Series	N22, N225	D23		D23-SE	M0/0+/3/33/4
<i>Categories</i>	<i>Embedded Control</i>	<i>Compute Acc.</i>	<i>Linux AP</i>	<i>FUSA</i>	<i>References</i>

■ **To be released in 2024:** D25F-SE, D45-SE, AX66

■ **Under Planning :** D23-SE, AX6X-SE

Note: roadmap subject to change without notice

RISC-V Continues to Rapidly

- **RISE: RISC-V Software Ecosystem, a project under LF Europe**
- **To accelerate the development of RISC-V open source SW**
- **Led by industry leaders**
- **Areas to focus over time:**

- Compilers & Toolchains
- Language Runtimes
- System Libraries
- Debug & Profiling Tools
- Simulator/Emulators
- Kernel and Virtualization
- Linux Distro Integration
- System Firmware



- **More at <https://riseproject.dev>**

晶心科技合作夥伴暨生態系統

AI tools, SW
and IP



Security



DSP, Audio and Vision

Development tools

RTOS





感謝聆聽