



# 晶心科技

## 投資者說明會

林志明

董事長暨執行長

113年3月22日



# 投資安全聲明

除本文包含的歷史資訊外，本演示文稿中涉及的事項均為前瞻性陳述，涉及某些可能導致實際結果出現重大差異的風險和不確定性，包括但不限於天氣、競爭產品和定價的影響、半導體產品供需的全行業變化、快速的技術變革、半導體行業週期、和一般經濟狀況。

除法律要求外，晶心不承擔因新資訊、未來事件或其他原因而更新任何前瞻性陳述的義務。



# 報告標題



- 晶心公司簡介
- 財務與經營狀況
- 關鍵應用與趨勢
- 研發暨技術能量



# 晶心科技公司簡介

## 晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數超過500人；80%為工程師。
- 獲得TSMC 2015年新的 IP OIP Award 。
- 晉升為RISC-V國際聯盟(前身為RISC-V基金會) 首席會員。(2020)
- 獲得AI Global Media頒發「2020年最傑出嵌入式處理器IP供應商」。
- EE Awards亞洲金選獎 - 「Taiwan 產品獎」, 「Asia 企業獎」(2021)
- 2023亞太區 前五百大高成長企業

## 晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

## 晶心利基

- 智能及環保之電子設備
- 雲端應用,人工智慧及物聯網

# 晶心科技公司現況

## 晶心科技指標性資訊

**19** Years

Pureplay CPU vendor

**500+**

Employee , > 80% R&D

**400+** Customers

Licensing AndesCore™

**14Bn+** SoC

Total Customer Shipment

## 2023年營運數字

Revenue \$ Growth

1.05 Bn, NT\$

13.5% YoY

License \$ Growth

18.3% YoY

Royalty \$ Growth

-1.2% YoY

SoC Shipping Q'ty

2.1Bn

## 晶心科技參與RISC-V International (RVI) 組織的工作



Founding & Premier Member from 2016



Board of Directors



Chairs/Co-Chairs of Task Groups



Technical Steering Committee



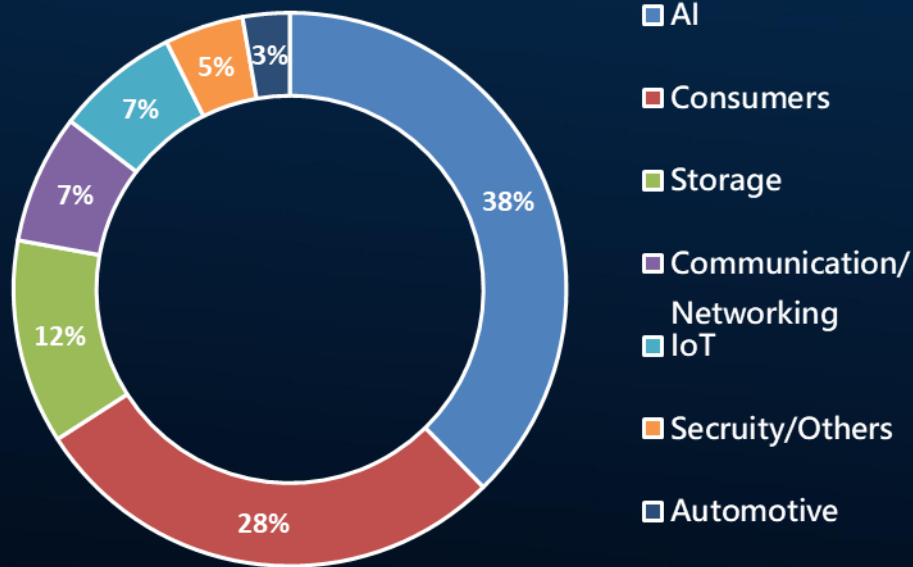
Ambassador



# 財務與經營狀況

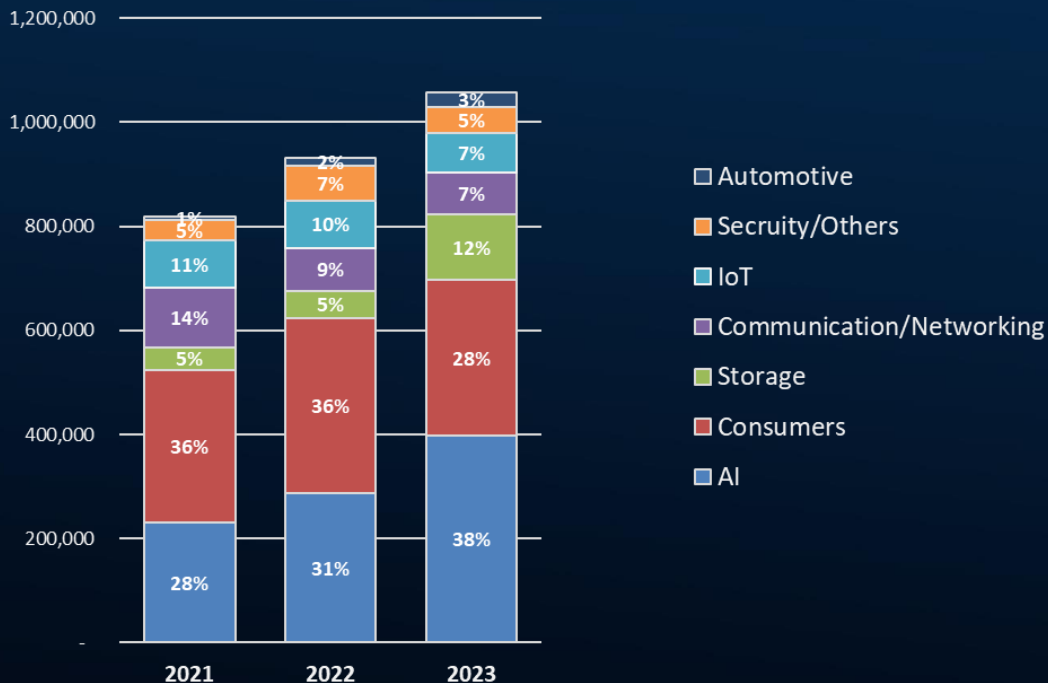
# 2023年度 營收應用類別分析

## Revenue



# 2021 to 2023年度 營收應用類別分析

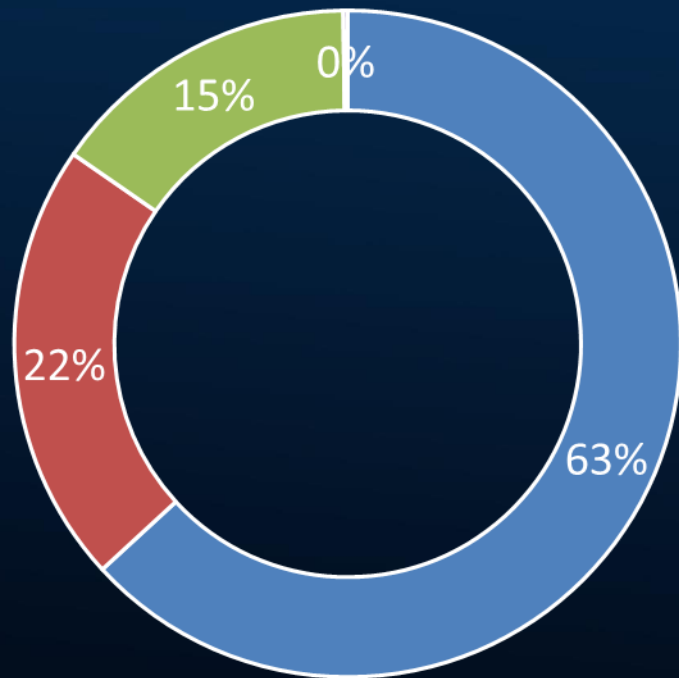
(NTD ' 000)







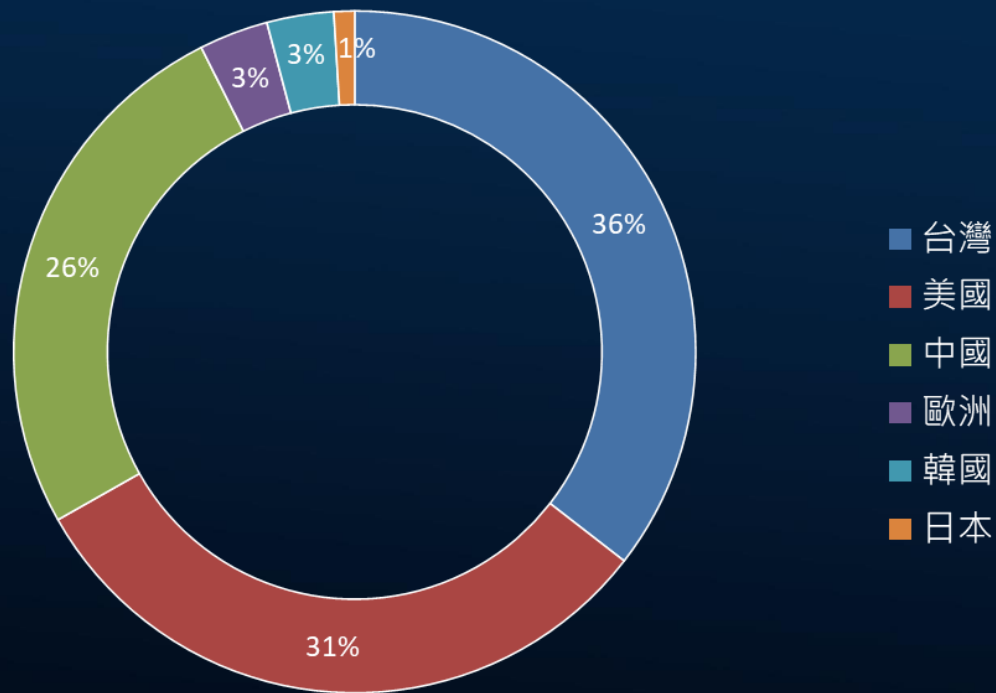
# 2023年度 營收商業模式分析



- 矽智財授權收入
- 權利金收入
- 維護服務收入
- 其他收入

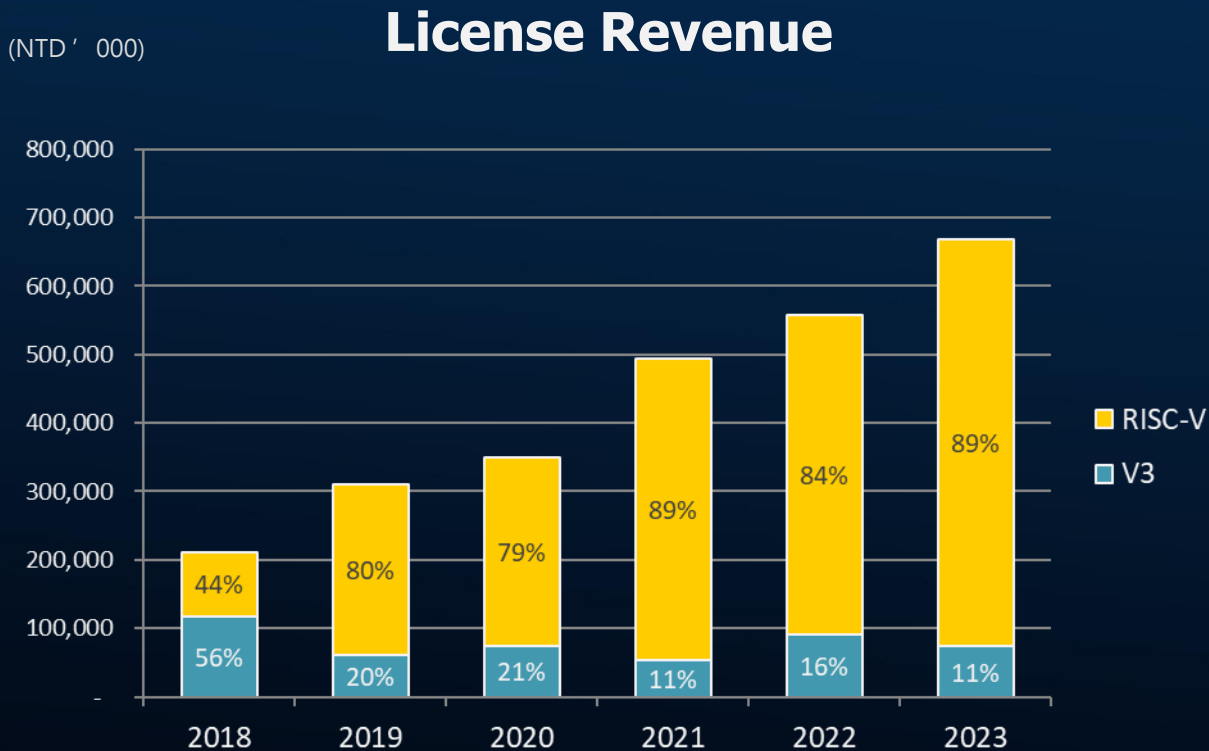


# 2023年度 地區別營收分析





# 歷年授權金收入分析

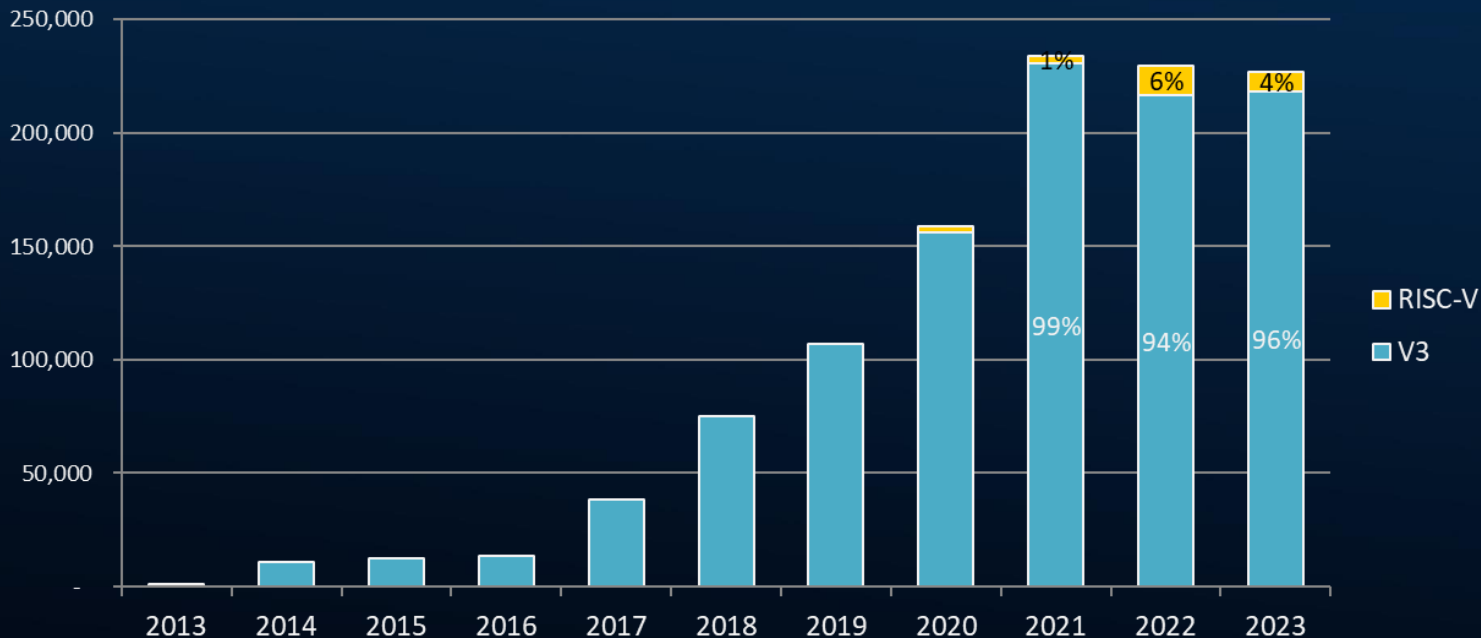




# 歷年權利金收入分析

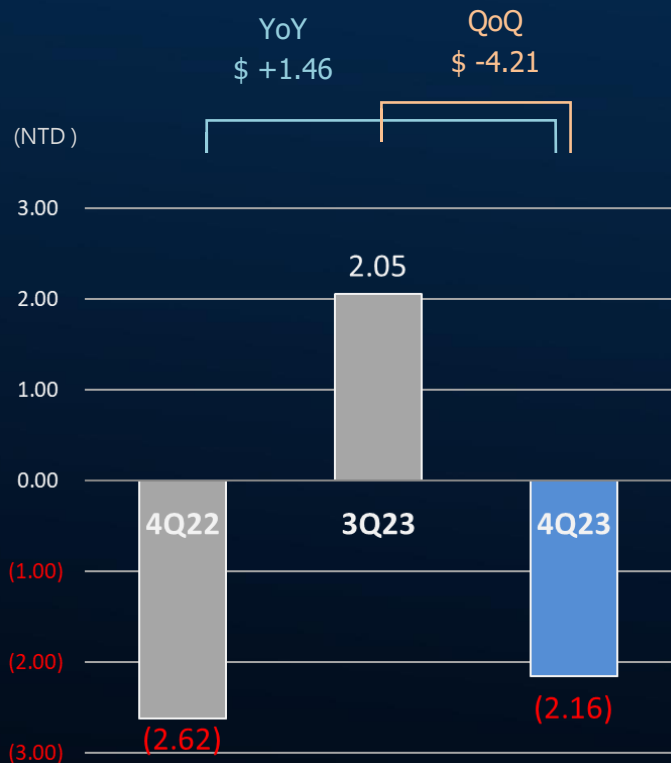
## Royalty Revenue

(NTD ' 000)





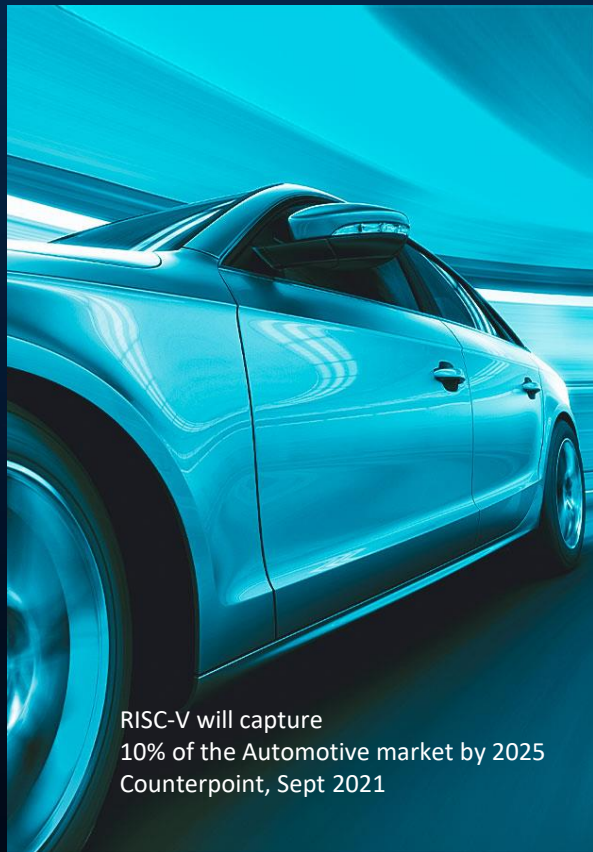
# 每股盈餘分析





# 關鍵應用vs.市場趨勢

# The Key Applications & The Trend



RISC-V will capture  
10% of the Automotive market by 2025  
Counterpoint, Sept 2021



RISC-V will command 28% of the  
IoT market by 2025  
Counterpoint, Sept 2021



RISC-V-based AI SoCs will grow 73.6%  
CAGR to 25B units and \$291B in revenue  
by 2027  
Semico Research, Dec 2021

# RISC-V for Datacenter & Cloud



RISC-V offers unique  
Opportunity for  
accelerators



Custom computing for  
AI and  
other emerging  
workloads



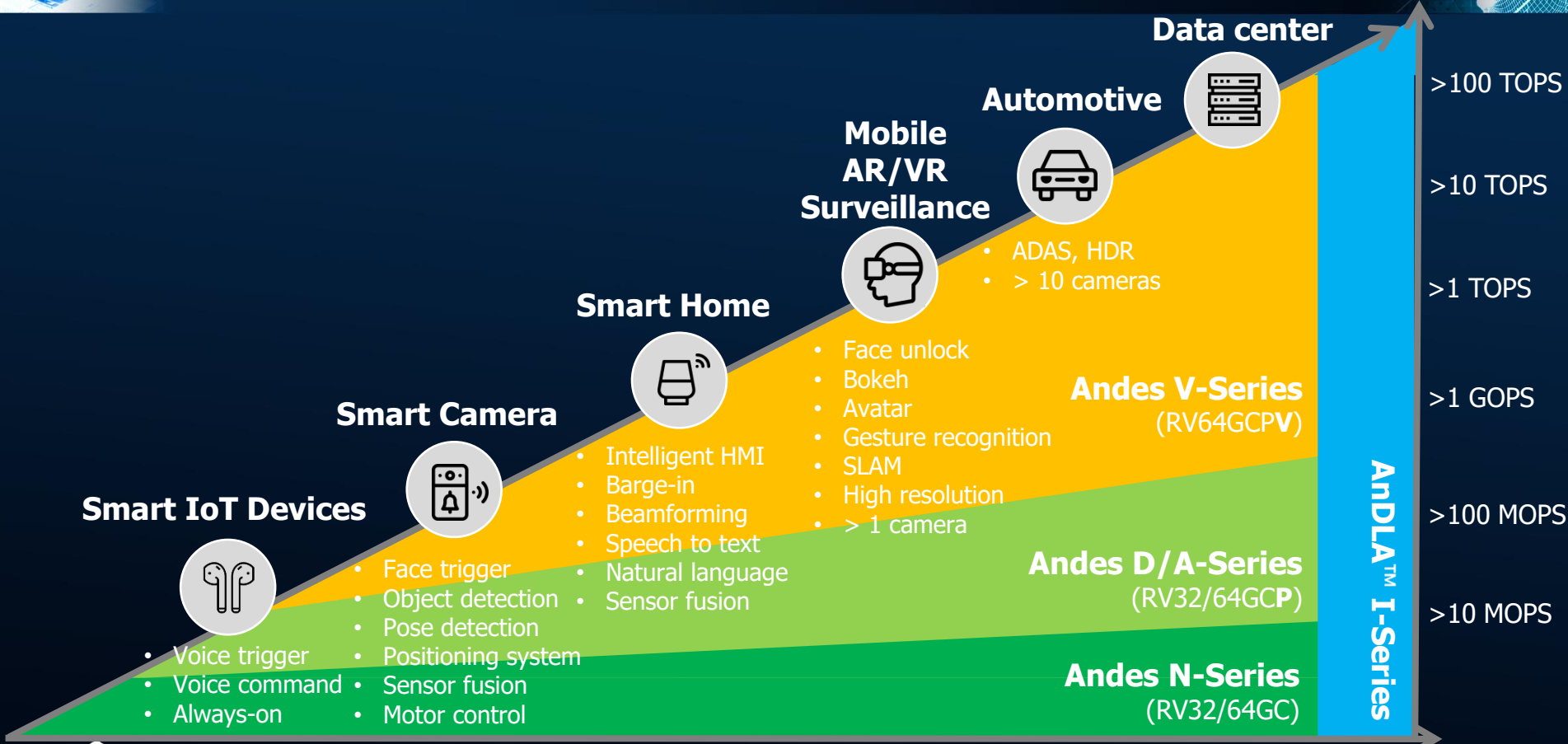
Achieve your  
performance and  
power targets

RISC-V CPU core market will grow 115% CAGR, capturing > 14% of all CPU cores by 2025



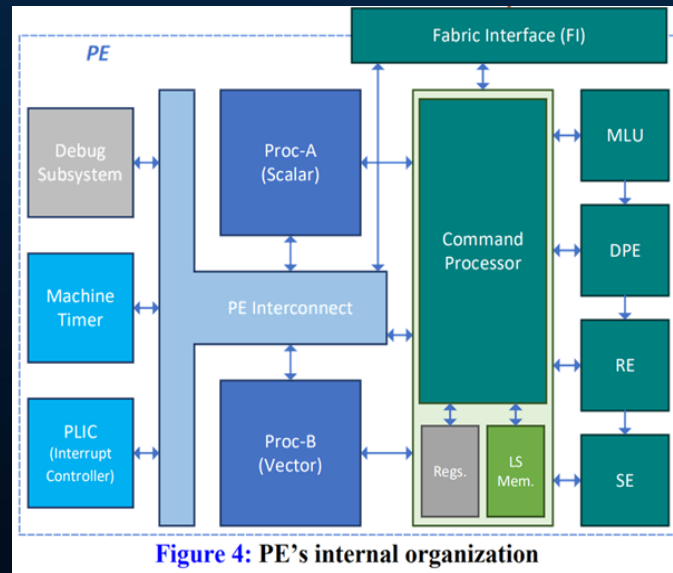


# Andes RISC-V Processors to Fit Your AI



# MTIA: Meta Training/Inference Accelerator

- ISCA 2023 paper, "MTIA: First Generation Silicon Targeting Meta's Recommendation Systems"
- Proc-A/B: AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models

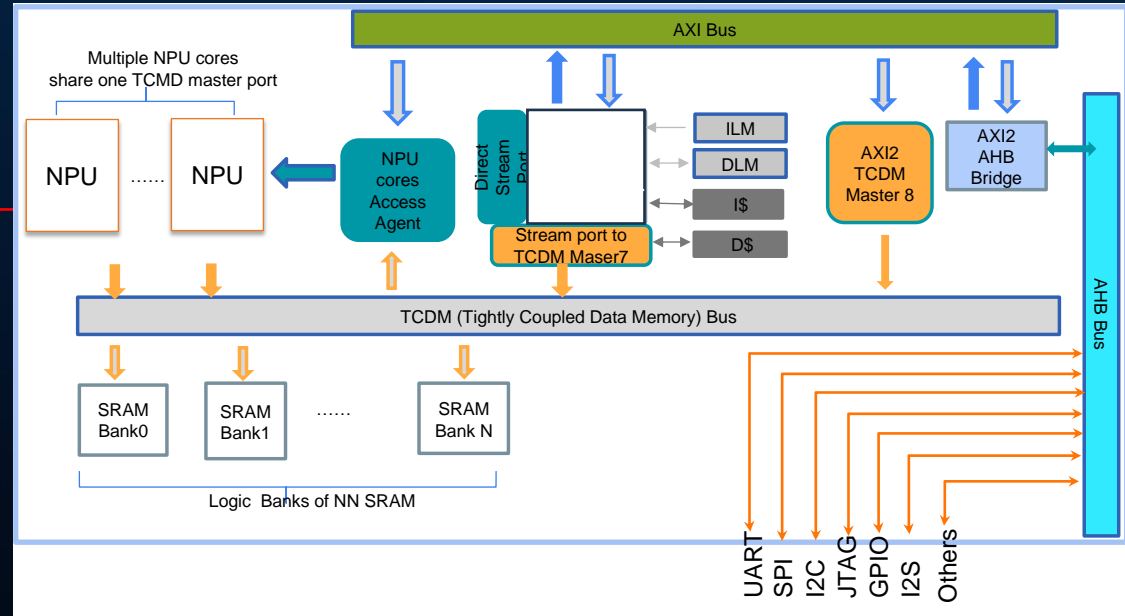
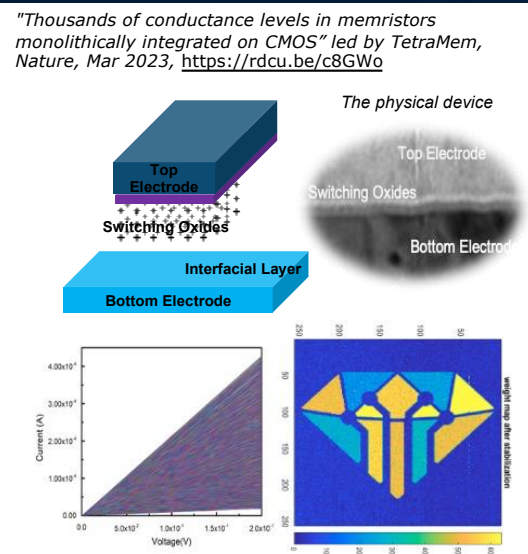


All photos: courtesy of ACM



# Edge AI With Analog In-Memory Computing

- **TetraMem** Analog In-Memory-Computing MX200 (**RRAM-based**)
- 8-bit 256x256 (**64K**) MAC Engines, **>30 TOPS/W** performance
- ML core operators (conv, gemm) processed in NPU
- Remaining operations processed in RISC-V Vector processors and control CPU





# Endpoint AI

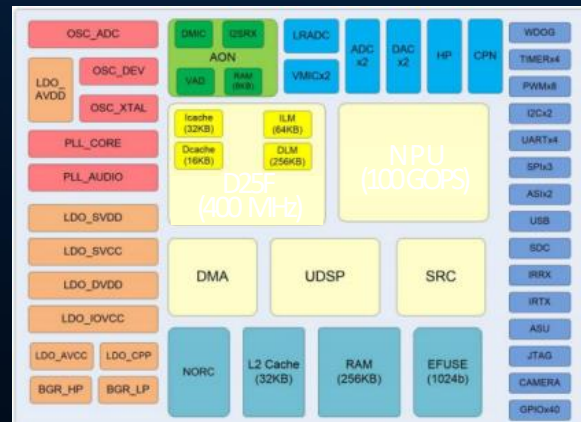
- Renesas R9A06G150 Voice-Control ASSP
  - With **100MHz DSP-capable D25F processor**
  - ML-based voice recognition gets >50% speedup by using P-extension



Voice HMI ASSP		100MHz 32-bit RISC-V with DSP, FP ext.		V6E32L483V 10u-10-68F6	
<b>CPU</b>	Andes-D25F RV32C/MAPP [Extensions] Andes StackSafe, PowerBrake, Recoverable NMI, Branch prediction PMP 16 regions	<b>Memory</b>	Code Flash (256 KB) SRAM (128 KB) [ w/ 4x32KB power-off ] Data Flash (16 KB) Standby SRAM (1 KB) QSPI (1ch)	<b>Analog</b>	12-bit ADC (6ch) w/ 2 SH 12-bit DAC (2ch)
<b>Communication</b>	SCI (2ch) w/ FIFO, Manchester I2C (1ch) SPI (1ch) w/ FIFO PDM (2ch) SSIE (2ch) IRDA (SCIO)	<b>System</b>	Machine Timer DTC DMA (8ch) On-chip Oscillators (HOCO, MOCO, LOCO) Ext. Oscillator/Clock (MOSC) 32-bit DOC	<b>Timers</b>	16-bit GPT (4ch) 32-bit Low Power Timer (4ch) WDT
<b>Package</b>		<b>Safety</b>	Bus Master MPU SRAM Parity Check Clock Accuracy Check CRC Calculator IWDG Oscillation Stop Detection	<b>Package</b>	QFN 48 QFN 32 QFN 24

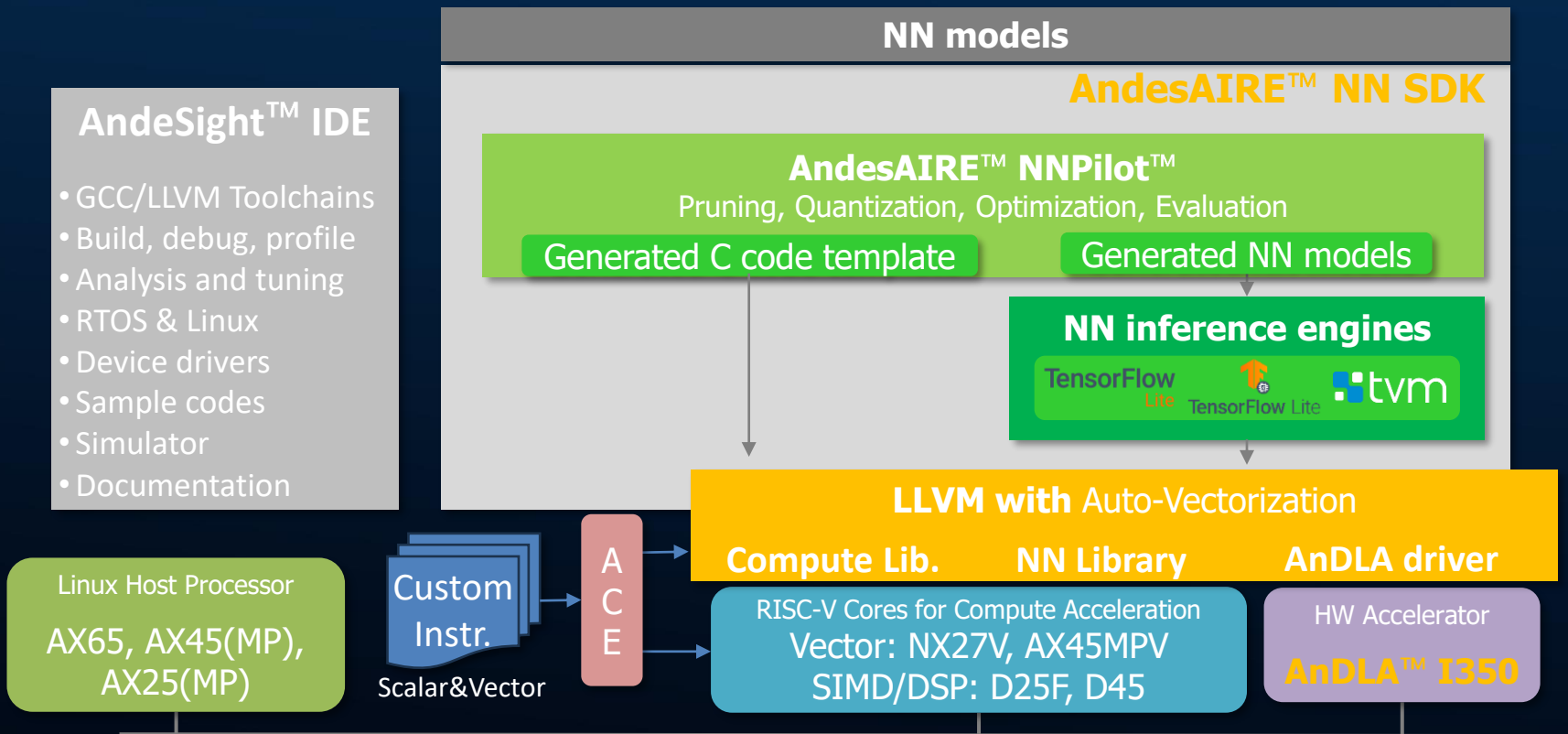
- Spacetouch SPV60 Intelligent audio processor

- High performance for customer development
  - ◆ 100 GOPS NPU for noise reduction, echo cancellation, howling suppression
  - ◆ uDSP for FFT/IFFT, atan, log, etc.
  - ◆ **400MHz D25F with ID caches/Local Memory**
- Rich audio interfaces and other peripherals
- Applications:
  - ◆ Intelligent voice, smart earphone, professional audio



# AndesAIRE™: Andes AI Runs Everywhere

## ■ HW/SW Solutions for AI from the Edge to the Cloud



# AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera



Smart Sensor



Smart Home Appliance



AIoT / tinyML



Robotics



Wearable



# RISC-V growth momentum Led by Industrial Leader



Leading Semiconductor Industry Players Join Forces to Accelerate RISC-V

Aug. 2023



Renesas Extends Leading RISC-V Embedded Processing Portfolio with New Motor Control ASSP Solution

Sep. 2022



Intel Mobileye EyeQ Ultra RISC-V processor targets Level 4 autonomous driving

Jan. 2022



European processor project shows shift to RISC-V

Dec. 2021



NSITEXE achieves world's first RISC-V processor with vector extension certified for ISO 26262 ASIL D ready product

Aug. 2021



RISC-V crypto core is qualified to ASIL-D for automotive designs

Jan. 2020



Kneron Unveils Its First RISC-V SoC Built for Autonomous, Assisted Driving

Nov. 2021



Andes and IAR Together Enable Leading Vendor ILITEK to Accelerate the Development of its ISO 26262 Ready TDDI SoC ILI6600A

Feb. 2023



Andes and IAR Systems enable leading automotive-focused IC design companies to accelerate time to market

Mar. 2022



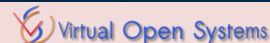
Andes Technology and Green Hills Software Team Up to Deliver Advanced Automotive Safety Platform for RISC-V

Aug. 2022



NSITEXE Selects ImperasDV for Automotive Quality RISC-V Processor Functional Design Verification

May 2022



VOSySmonitoRV, a Secure Monitor Layer for RISC-V Architecture Mixed-Critical Systems



Andes Technology and Parasoft Collaborate to Provide Seamless Software Testing Tools for Automotive Functional Safety Applications

Dec. 2022



Andes Technology Collaborates with LDRA to Deliver Integrated Tool Suite for Safety-Critical Software on Andes RISC-V CPU Solutions

Jan. 2023



Upgrade to Solid Sands' latest SuperTest version supports Andes to its ambitions for further growth in the automotive sector

May 2023

# Andes is Supporting RISC-V for Automobiles

Since founded in March 2005,  
Andes Technology is working step-by-step on  
RISC-V for ISO 26262 Functional Safety

2016

**Andes Joined RISC-V Foundation as one of the Founding Members**

- Promoted as Founding Premier Member of RISC-V International in 2019

2017

**The First RISC-V Architecture AndesCore™ NX25 and N25 Released**

- 25-Series became one of world's most licensed RISC-V CPUs

2020

**Andes Development Process Certified for ISO 26262**

- Andes became the first ISO 26262 certified RISC-V CPU IP supplier in the world

2022

**AndesCore™ N25F-SE Certified for ISO 26262**

- N25F-SE became the first full compliant ISO 26262 certified RISC-V CPU in the world



2024

**AndesCore™ D25F-SE to be Released**

- A series of Andes Functional Safety CPU cores will soon follow







# AndesCore™ for Automotive Electronics

## ■ Supporting a Wide Variety of Functional Safety Applications:

- Dashboard display, in-car monitoring, keyless entry, lighting control, tire pressure monitoring, vision ADAS, microcontroller and many more

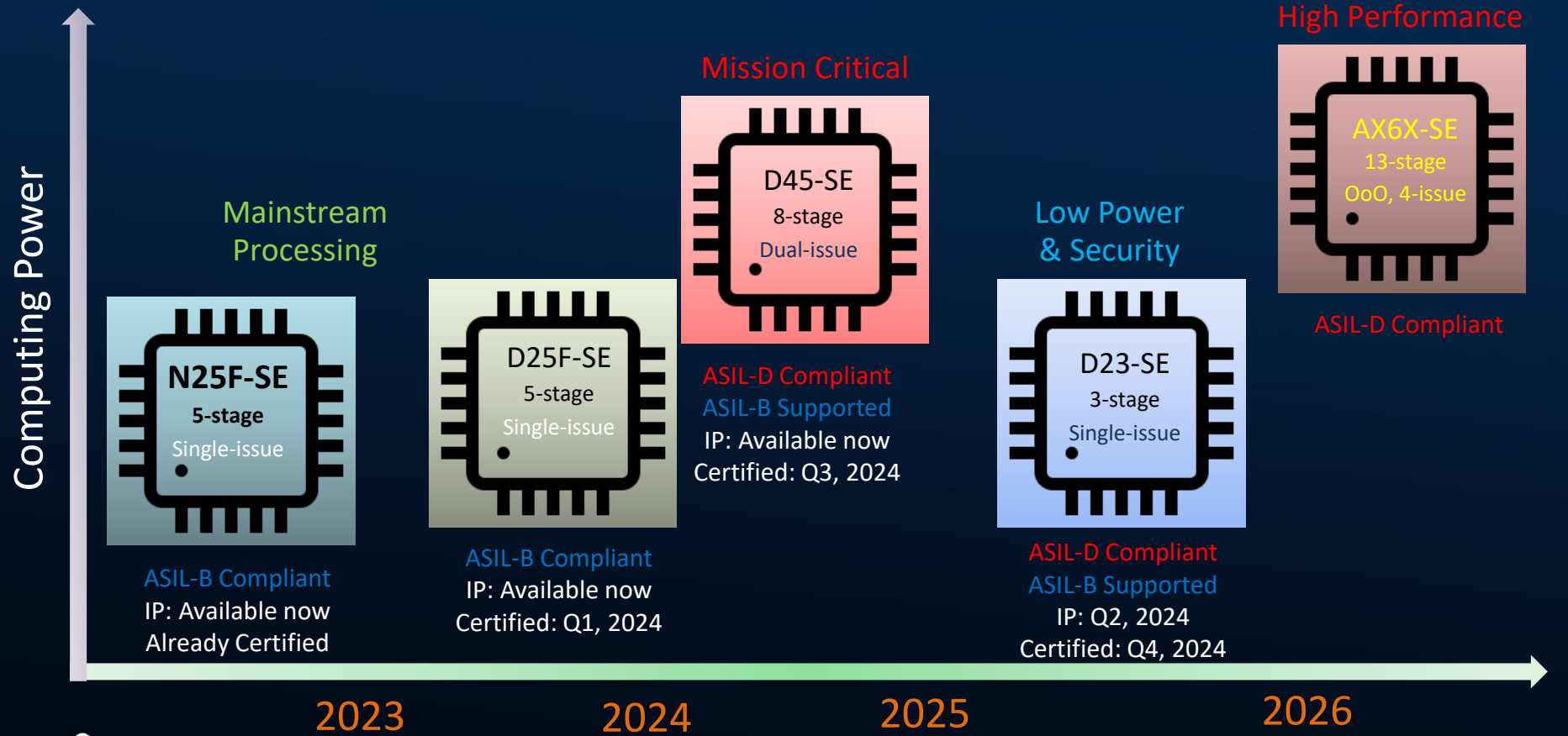
## ■ Developers using AndesCore™ Functional Safety Processors to:

- Introduce new electronic systems on automobiles
- Upgrade existing systems that needs to be ISO 26262 compliant





# Andes FUSA Roadmap



# Andes Automotive Ecosystem

- Co-working with global leading suppliers in the automotive industry
- Andes and ecosystem partners jointly deliver the trusted RISC-V automotive solutions to designers complying with the standard of functional safety ISO 26262
- Partner Ecosystem Catalogs

## Security

**Rambus**

HSM / RoT

**SECURE-IC**  
THE SECURITY SCIENCE COMPANY

Securizr™ SE

**Virtual Open Systems**

VOSySmonitoRV

**豆荚 BeanPod**

**TrustKernel**

TEE

## Safety RTOS



WITTENSTEIN

SAFERTOS

**Microsoft**

Microsoft Azure RTOS

**WINDRV**

VxWorks

## AUTOSAR

**VECTOR**

AUTOSAR

**SIEMENS**

Capital VSTAR  
Nucleus SafetyCert

**FPG**

Fpt Software

MaaZ AUTOSAR

## Compiler / Debugger

**iar**

EWRISCV

**Green Hills**  
SOFTWARE

MULTI IDE / Compiler  
RTOS

**TASKING**

RiscFree IDE/Compiler

**ASHLING**

Compiler

**LAUTERBACH**  
DEVELOPMENT TOOLS

TRACE32 Debugger

**LDRA**  
ASSURED

Tool

LDRA Tool Suite

**PARASOFT**

Parasoft C/C++ Test



# 研發暨技術能量

# 晶心科技的 CPU Core IP

<b>AX60 Series</b> 13-stage OOO Linux MP		AX65	AX66	AX6X-SE	A72~A78; N1/V1/X1
<i>Categories</i>	<i>Power-efficient</i>	<i>Mid-range</i>	<i>Extended</i>	<i>FUSA</i>	
<b>45 Series</b> 8-stage Superscalar	N45, NX45	D45	AX45MPV A45(MP), AX45(MP)	D45-SE	A53/55, R52/ R82, M7
<b>27 Series</b> 5-stage MemBoost		NX27V	A27(L2), AX27(L2)		A5/7/35
<b>25 Series</b> 5-stage Fast&Compact	N25F, NX25F	D25F	A25(MP), AX25(MP)	D25F-SE N25F-SE	A5/7/35, R4/5, M4/33
<b>Compact Series</b>	N22, N225	D23		D23-SE	M0/0+/3/33/4
<i>Categories</i>	<i>Embedded Control</i>	<i>Compute Acc.</i>	<i>Linux AP</i>	<i>FUSA</i>	<i>References</i>

■ **To be released in 2024:** D25F-SE, D45-SE, AX66

■ **Under Planning :** D23-SE, AX6X-SE

Note: roadmap subject to change without notice

# RISC-V Continues to Rapidly

- **RISE: RISC-V Software Ecosystem, a project under LF Europe**
- **To accelerate the development of RISC-V open source SW**
- **Led by industry leaders**
- **Areas to focus over time:**

- Compilers & Toolchains
- Language Runtimes
- System Libraries
- Debug & Profiling Tools
- Simulator/Emulators
- Kernel and Virtualization
- Linux Distro Integration
- System Firmware



- **More at <https://riseproject.dev>**

# 晶心科技合作夥伴暨生態系統

AI tools, SW  
and IP



Security



DSP, Audio and Vision

Development tools

RTOS





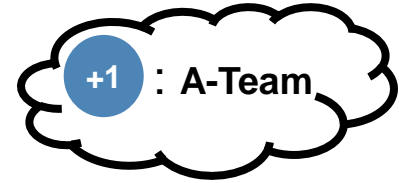
# 擴充技術能量 進而成長與分享成果



# Review 2021 GDR and Achievement

- **2021 Q3 \$127M GDR was raised**
- **All projects planed in GDR roadshow all kicked off, with one more project kicked-off: Andes new office**
  - Design centers expansion (200 worldwide experts) were smooth, and getting stabilized now, R&D results with such expansion started to show up
- **In 2023 Q4 AX65 IP was released, it started with counting ROI of GDR**
- **Estimate 2024 to 2026 will be peak of products development output with 2021 GDR raised, which in turn will bring in new stream of revenue growth**

# Andes Future project pipeline – Beyond Current Roadmap



**Project I**  
**Qilai**

*Platform Chip with AX45MP + NX27V+ high-speed interfaces*

- **Potential applications:** Office productivity tools, Image processing tools, Web browsers, Scientific computation libraries, AI infrastructure



**Project II**  
**Makadou**

*Next Generation High-end RISC-V Core for Edge AI/Tablet/Automotive*

- **Potential applications:** Edge AI, Tablet, Automotive electronics, Advanced Driver Assistance Systems



**Project III**  
**Cuzco**

*Server-grade RISC-V core for Datacenter AI/Desktop/HPC*

- **Potential applications:** Datacenter AI, Desktop PC/Server, High-Performance Computing

新聞稿 2021-10-29

## 晶心科技發行GDR 於盧森堡證券交易所上市 拓展業務

[Facebook](#) [推特](#) [領英](#)

加州聖荷西 – 2021年10月29日 – RISC-V CPU IP 領先供應商晶心科技 (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099) 今天宣布成功發行海外存託憑證 (GDR)。日盧森堡證券交易所上市。每份新發行的海外存託憑證單位將代表2股普通股，其初始市值定價為31.78美元，約合每股新台幣440元。總共發行400萬股，相當於800萬股普通股。海外募資總額約1.27億美元（新台幣35.17億元）。晶心科技是目前唯一上市的RISC-V CPU IP供應商，GDR股東主要是尋求長期投資的境外機構投資者。

晶心科技主席兼行政總裁林富豪表示：“此次融資讓晶心科技實現了推動中長期研發資本投入、擴大產品線，特別是高端產品的主要目標。”「此外，全球投資者能夠分享快速成長的 RISC-V 市場。為滿足RISC-V高階運算解決方案的迫切需求，這筆資金將主要用於加速產品設計中心的擴建，以強化我們現有領先的RISC-V產品組合，並加快開發高價值和高價值的產品。高階RISC-V CPU IP和SoC軟硬體整合解決方案。為了搶佔高利潤的高階多核心CPU IP市場並提升銷售勢頭，晶心科技位於台灣、美國和加拿大的設計中心計劃招募200名研發人才，開發下一代RISC-V產品，應用於5G等應用、人工智慧/機器學習、HPC、ADAS、汽車電子、AR/VR、區塊鏈、雲端運算、資料中心、伺服器、物聯網、MCU、儲存設備、安防、無線設備等大量高效能運算市場」。

晶心科技報告，2021年上半年營收年增72.6%，其中63%的營收來自RISC-V產品，包括標準IP授權和客製化運算業務。此外，2020年的收入較2018年晶心開始交付最初的RISC-V核心時幾乎翻了一番。根據 Counterpoint Research 的最新報告，隨著半導體解決方案需要越來越多的多功能IP，純半導體IP 市場規模將以11%的複合年增長率增長，到2025年達到每年86億美元。RISC-V由於其開源性，正在快速成長。優點在於，功耗優化更容易、安全功能可靠、政治風險影響更低。RISC-V處理器將繼續在包括物聯網、工業和汽車在內的多個類別中快速採用，到2025年，這些領域的採用率將分別達到28%、12%和10%。這些市場擴張的有利因素將有利於晶心科技及其子公司顧客。

# Andes Technology USA Corp. Announces Major Expansion of Its U.S. Operation



## *Company Announces Job Openings for San Jose Headquarters and Portland R&D Office*

**San Jose, California October 8, 2021** – Andes Technology USA Corp., the headquarters of North America operations of Hsinchu, Taiwan-based Andes Technology Corporation, a leading supplier of high efficiency, low-power 32/64-bit RISC-V processor cores and founding premier member of RISC-V International, today announced a major expansion of Its U.S. operation. Andes Technology USA is greatly increasing engineering headcount in both the San Jose, California headquarters and its Portland, Oregon research and development facility. Andes Technology USA is seeking engineers in the U.S. and Canada to work remotely or in the Portland or San Jose offices. Openings are available for design engineers, verification engineers, and field application engineers.

Andes Technology USA Corp. was established in 2015 as a California corporation coincident with Andes Technology Corp. joining RISC-V International. After Andes took the RISC-V instruction set architecture (ISA) as the base to form its fifth generation architecture, AndeStar™ V5 and started developing V5 processor IP's, the U.S. operation was formed to be nearby early customer adopters of the new ISA. The U.S. subsidiary established an R&D lab shortly thereafter and began developing architectures for the high-end RISC-V processors. In under a year the investment together with the main engineering team in Taiwan yielded the first commercial RISC-V Vector processor IP which won nearly 10 projects including datacenter projects from a large OEM so far.

“Major semiconductor companies worldwide adopting the RISC-V ISA and the RISC-V International work groups rapid development of the RISC-V ISA extensions is driving demand for engineers to keep up with the fast pace of new technology development,” said Emerson Hsiao, Andes Technology USA Corp. Chief Operating Officer. “RISC-V customers like the growing number of extensions coming available as well as their ability to customize the architecture to better fit their processing requirements. Our tool Andes Custom Extensions (ACE) and the customization capabilities with Andes Technology’s RISC-V toolchain help customers

# 2024 Andes RISC-V Con Hsin-Chu

■ 2024, 3, 28

■ 3A1S

晶心RISC-V CON 新竹

2024-03-28 @ 13:00 - 18:00

## 2024 Andes RISC-V CON

深探車用、AI、應用處理器與安全技術趨勢

JOIN NOW

# 支持國內企業、研究機構、大學參與晶創計畫



2024 - 2033  
3,000億元經費  
計畫優先支持採用國內IP

**ANDES**  
TECHNOLOGY

**ANDES**  
TECHNOLOGY

**ANDES**晶心科技



## 支持企業參與 晶創計畫說明會

2024 / 3 / 6 (三)

### 活動議程

13:30-14:00 報到

14:00-14:10 致詞

14:10-14:50 如何運用Andes IP  
申請晶創計畫

14:50-15:10 Q&A

\*活動採實體與線上同時舉辦\*

實體地點: 晶心科技EVEREST會議室  
(新竹市公道五路3段1號10樓)  
現場備有茶點歡迎參加!

歡迎免費報名



加速創新突破

- 授權費用
  - ✓ 專案生產小於並包含 1000 顆之晶片，授權費為訂價的 Y折
  - ✓ 專案生產超過1000顆晶片視為該專案量產，授權費為訂價的X折
- 每年技術維護費與產品更新費用
  - ✓ 一般商用條件：授權費的 Z%
  - ✓ 晶創計畫：授權費的 W%
- 費用待晶創計畫申請獲審核通過才須支付給晶心科技，若最終計畫未通過，則申請單位可撤銷合約
- 雙方應事先討論整體計畫與應支付晶心科技之費用整合之合理性



## 二、推動領域及補助範疇

驅動臺灣業者投入先進技術應用晶片，至2026年等同或超越國際標竿大廠技術指標之晶片設計開發

### 符合晶創計畫集產業趨勢的研發方向

#### ■ 補助範疇(目標)

- 一. 創新技術之先進晶片開發，採用7nm(含)以下製程。
- 二. 先進異質整合封裝技術之創新晶片(如小晶片整合封裝模組、矽光子等其他新興應用晶片開發)。
- 三. 異質整合微機電感測技術之創新晶片開發，採用0.35μm(含)以下之晶圓級製程。
- 四. 優先推動人工智慧、高效能運算、車用電子、下世代通訊等四領域，規格如下：

Data: 經濟部

#### 一、人工智慧：

- ✓伺服器(推論)：算力 > 500 TOPS
- ✓裝置端：算力 > 80 TOPS

#### 二、高效能運算：

- ✓ 算力 > 500 TOPS

#### 三、車用電子：

- ✓輔助駕駛：算力 > 80 TOPS(L2+)
- ✓智慧座艙：算力 > 40 TOPS

#### 四、下世代通訊

- ✓無線傳輸  
B5G/6G >15 Gbps以上；Wifi >20 Gbps以上
- ✓有線傳輸 >800 Gbps以上





感謝聆聽