Andes Technology Corp.

Investor Conference

Frankwell Lin
Chairman & CEO

Mar. 22, 2024

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

Report Topics

- Andes Company Introduction
- The Financial & Operation Status
- The Key Applications & The Trend
- The R&D Power for The Future

Andes Company Introduction

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 500 people; 80% are engineers.
- TSMC OIP Award "Partner of the Year" for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award "Most Outstanding Embedded Processor IP Supplier" (2020)
- EE Awards - "Taiwan-Product Award" & "Asia-Company Award" (2021)
- Top 500 High-Growth Companies Asia-Pacific (2023)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

Andes Technology Corporation

Quick Facts on Andes

19 Years
Pureplay CPU vendor

500+
Employee , > 80% R&D

400+ Customers
Licensing AndesCore™

14Bn+ SoC
Total Customer Shipment

2023 Operation Result

Revenue $ Growth
1.05 Bn, NT$
13.5% YoY

License $ Growth
18.3% YoY

Royalty $ Growth
-1.2% YoY

SoC Shipping Q'ty
2.1Bn

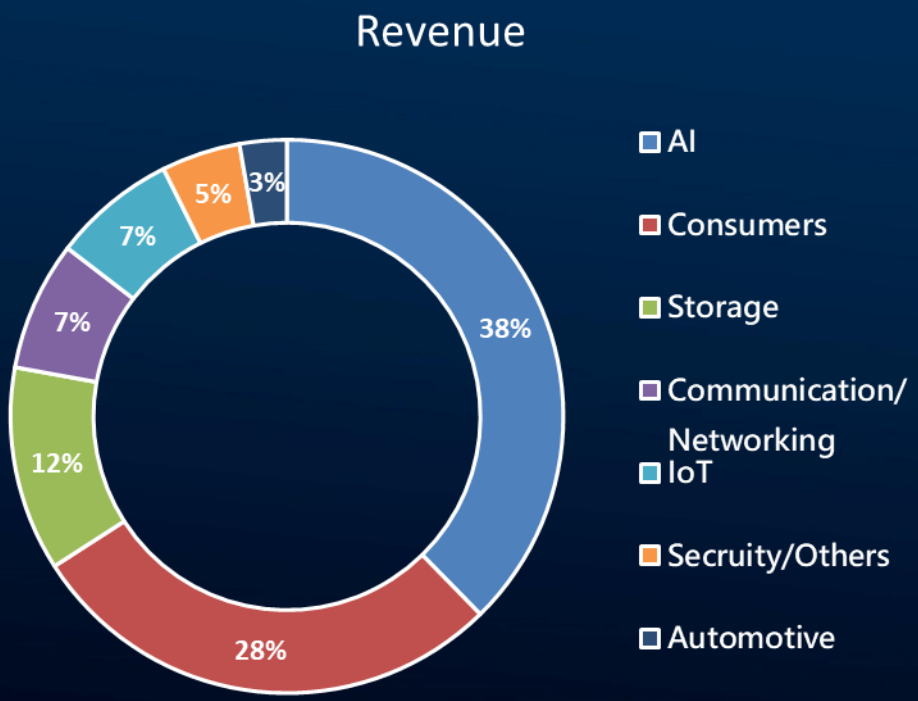
Andes and RISC-V International (RVI)

Founding & Premier Member from 2016

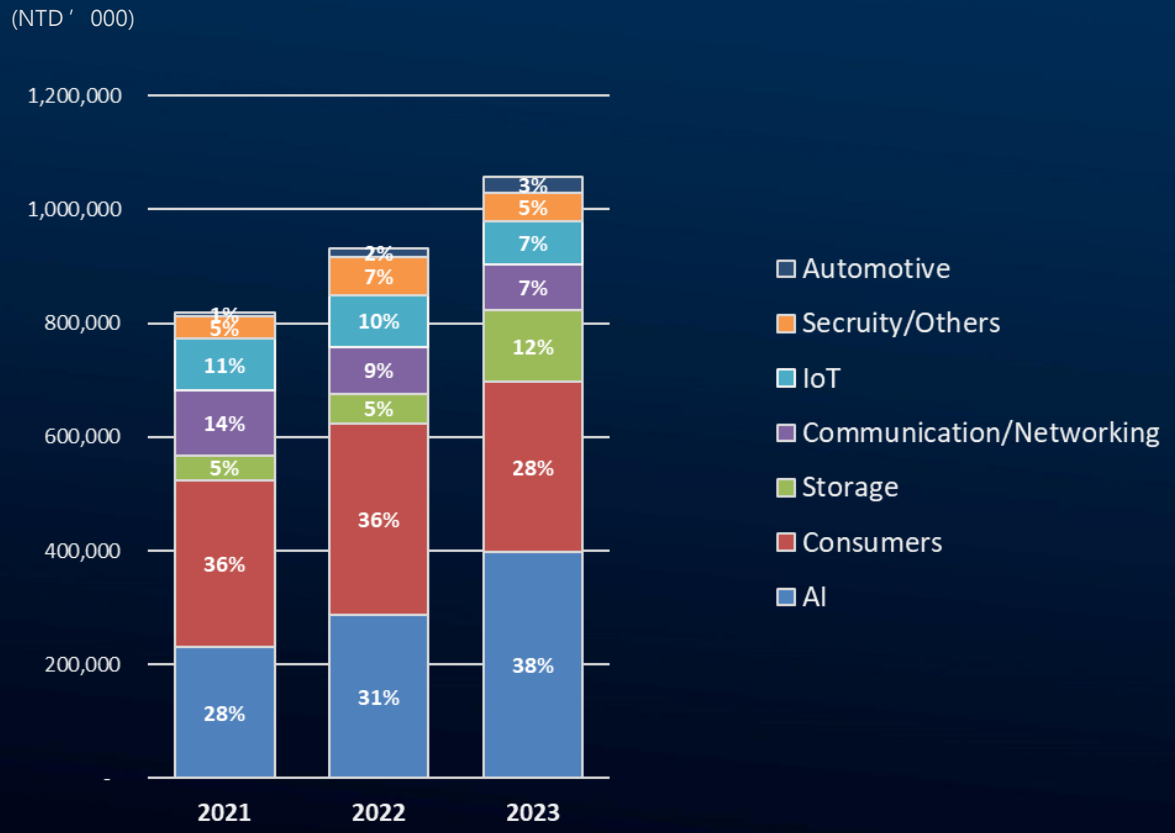
- Board of Directors
- Technical Steering Committee
- Chairs/Co-Chairs of Task Groups
- Ambassador

The Financial & Operation Status

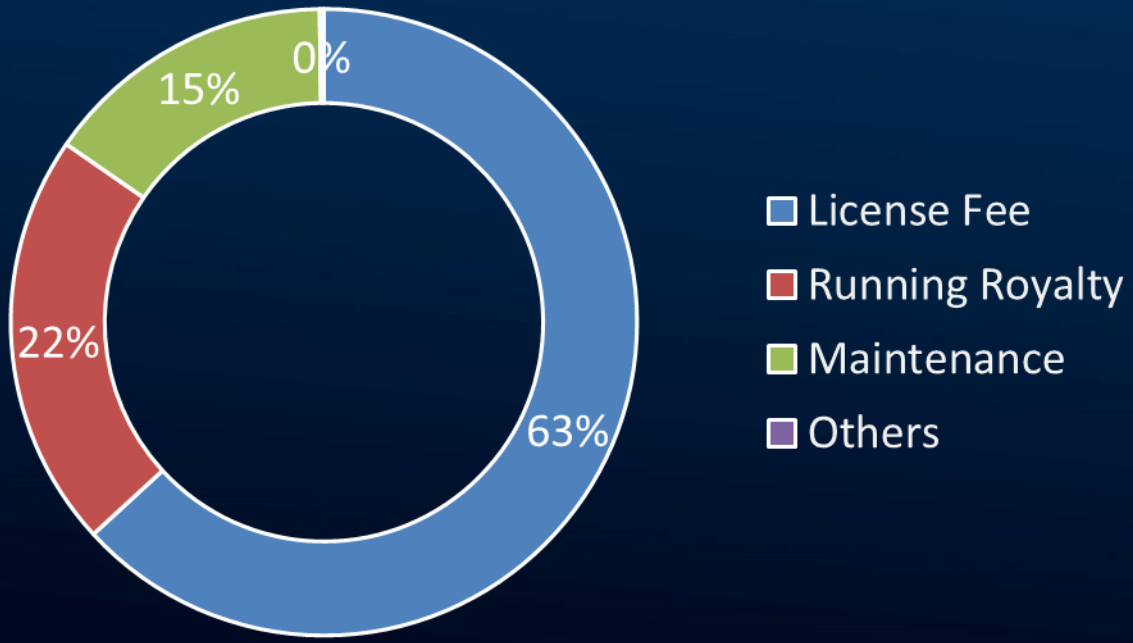
2023 Q1-Q4 Revenue Analysis by Application



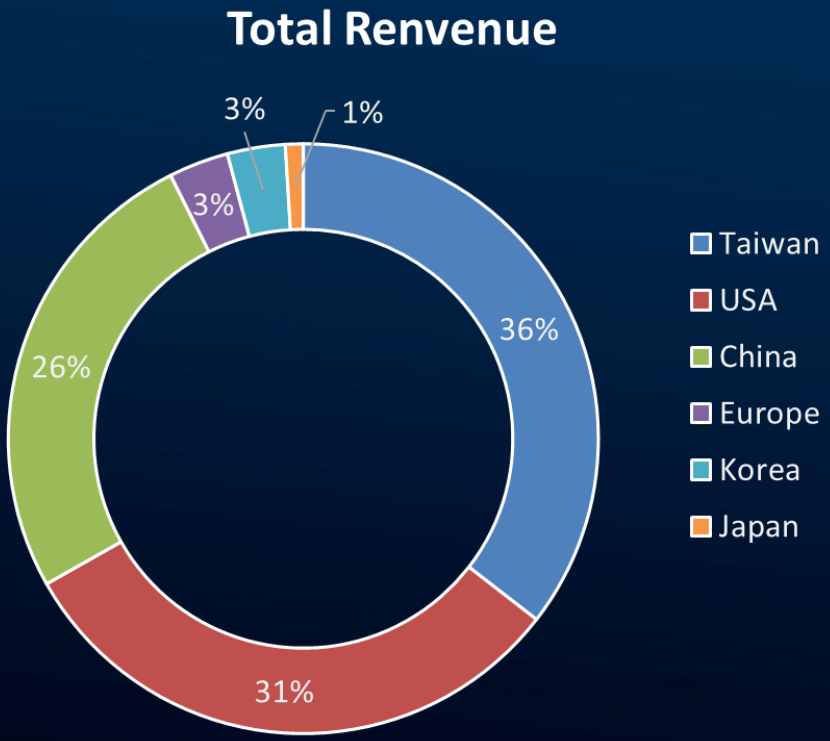
2021 to 2023 Revenue Analysis by Application



2023 Q1-Q4 Revenue Analysis by Business Model

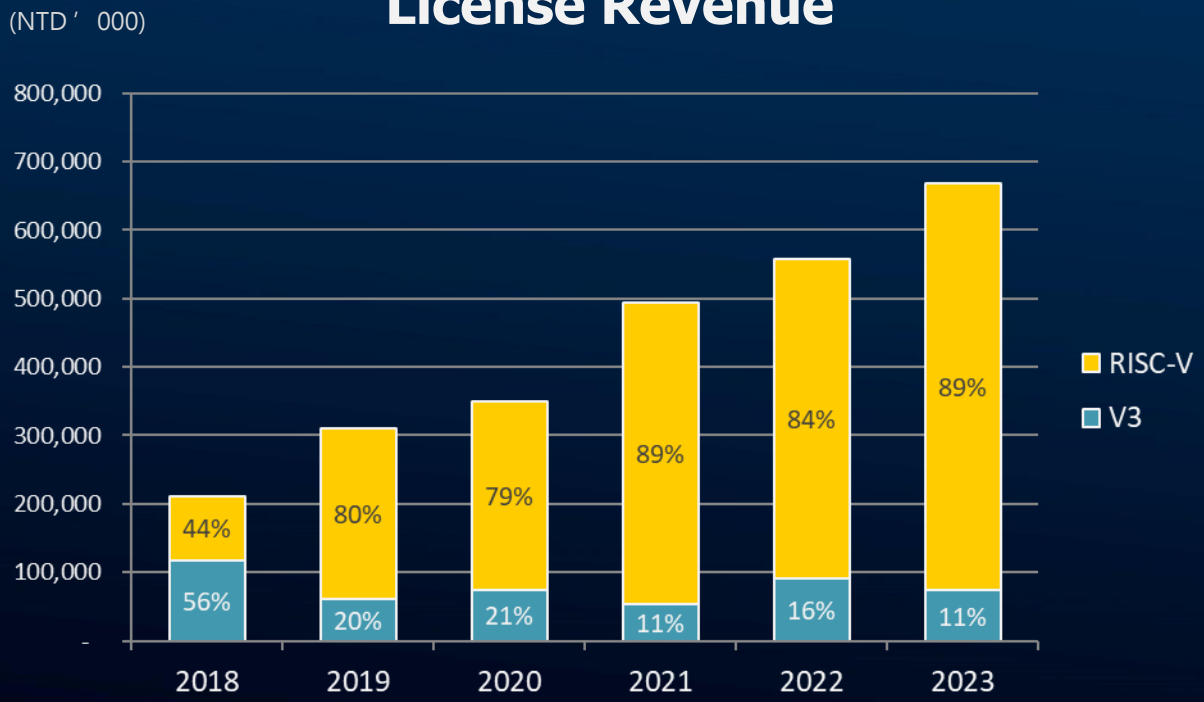


2023 Q1-Q4 Revenue Analysis by Region



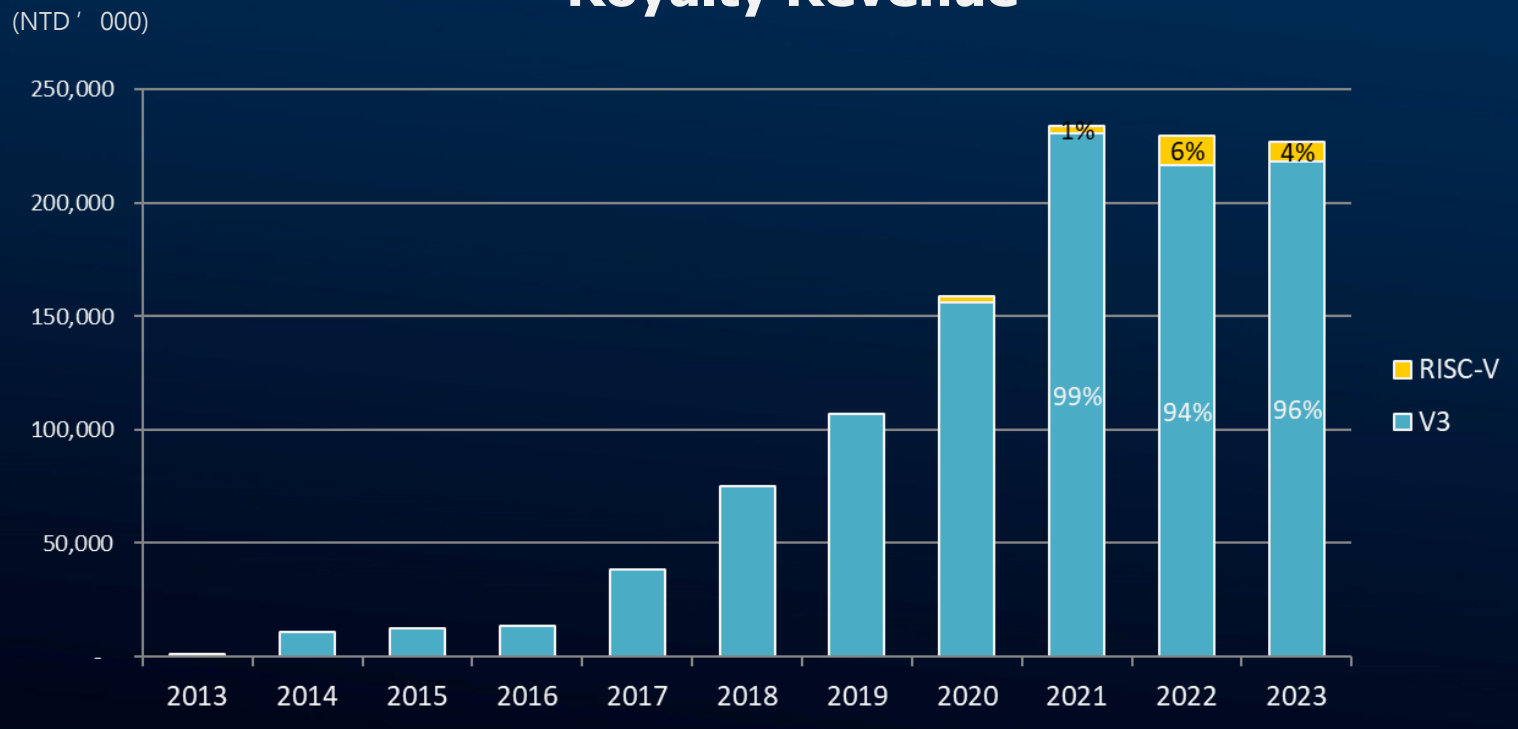
Historical License Revenue Analysis

License Revenue

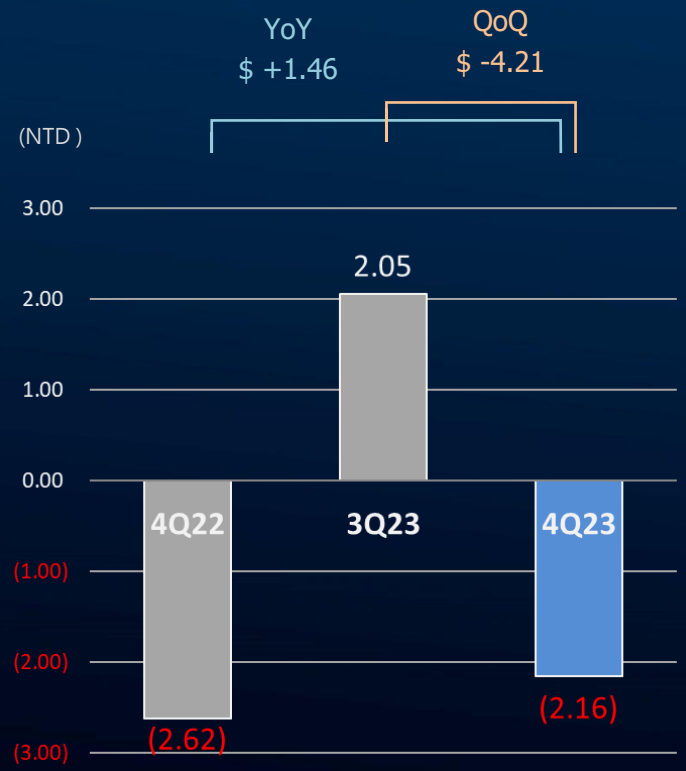


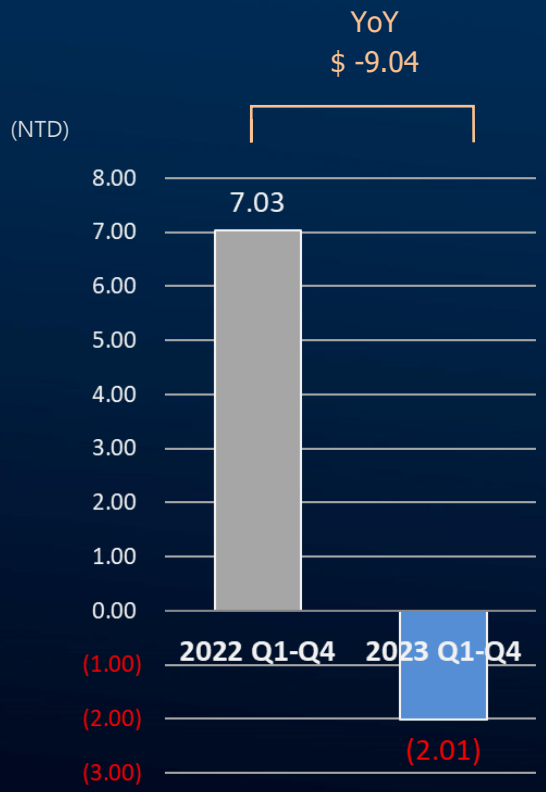
Historical Royalty Revenue Analysis

Royalty Revenue



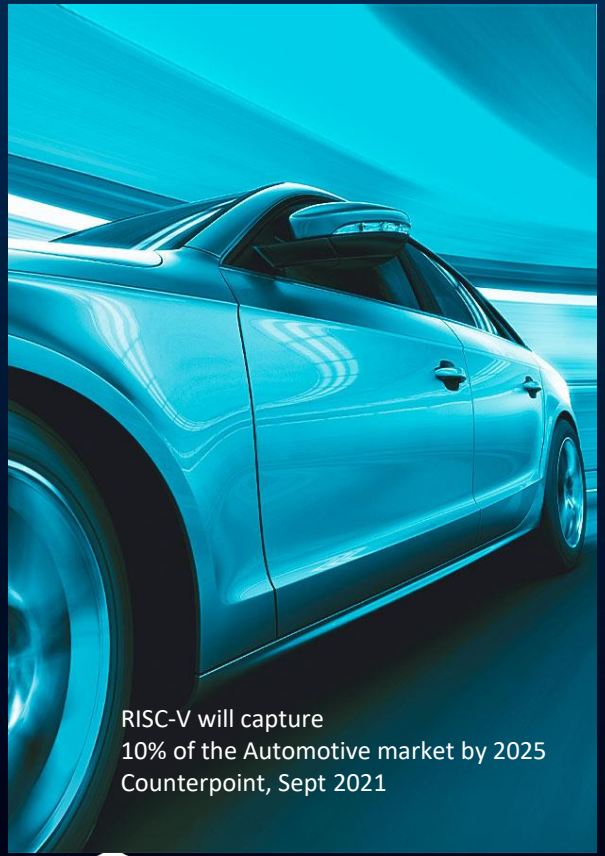
EPS Analysis





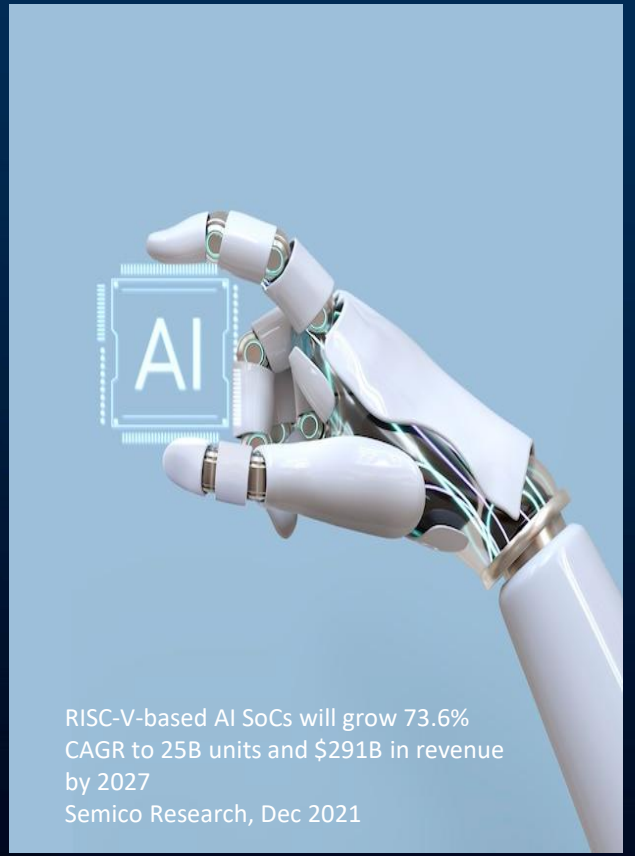
The Key Applications & The Trend

The Key Applications & The Trend



RISC-V will capture
10% of the Automotive market by 2025
Counterpoint, Sept 2021

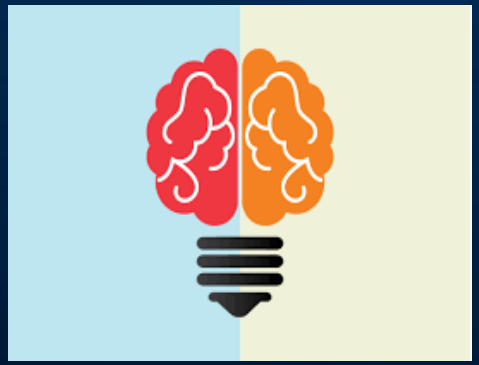
RISC-V will command 28% of the
IoT market by 2025
Counterpoint, Sept 2021



RISC-V-based AI SoCs will grow 73.6%
CAGR to 25B units and $291B in revenue
by 2027
Semico Research, Dec 2021

RISC-V for Datacenter & Cloud

RISC-V offers unique Opportunity for accelerators

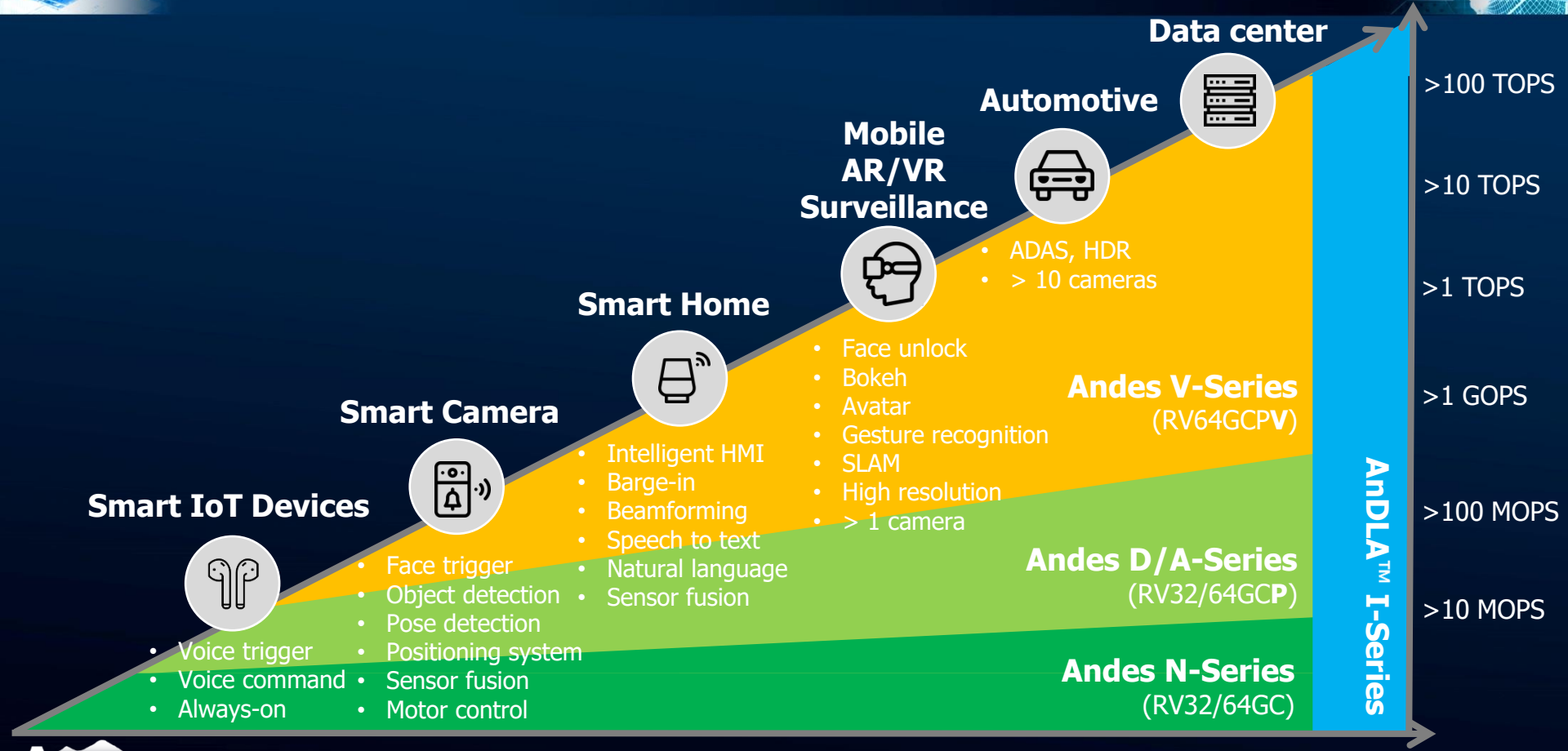


Custom computing for AI and other emerging workloads

Achieve your performance and power targets

RISC-V CPU core market will grow 115% CAGR, capturing > 14% of all CPU cores by 2025

Andes RISC-V Processors to Fit Your AI



MTIA: Meta Training/Inference Accelerator

- ISCA 2023 paper, "MTIA: First Generation Silicon Targeting Meta's Recommendation Systems"
- Proc-A/B: AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models

Figure 3: High-level architecture of the accelerator

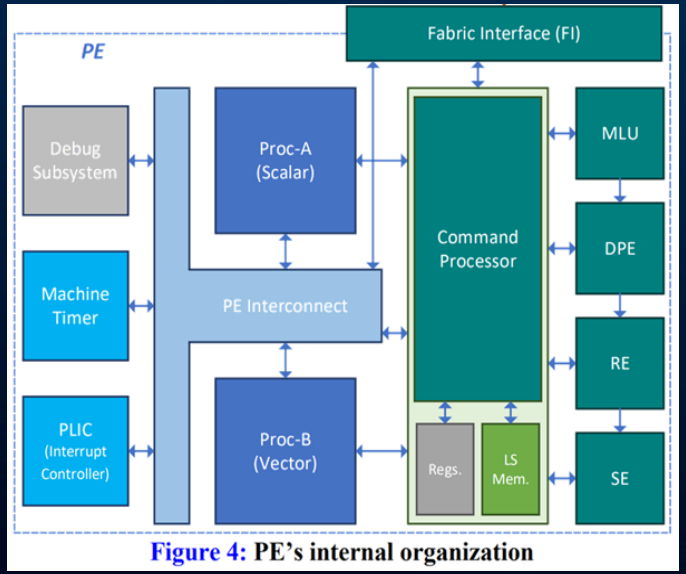
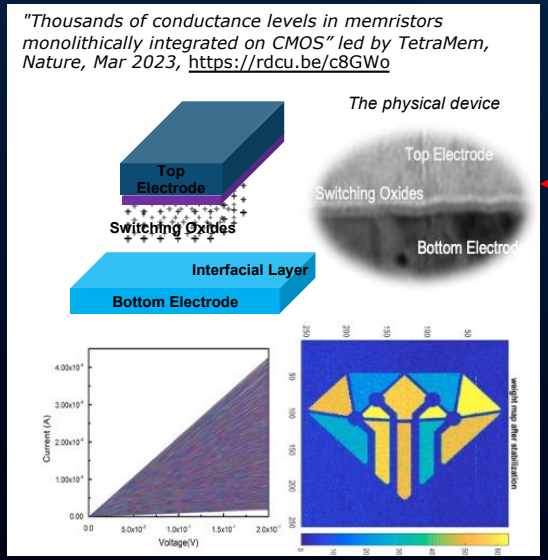


Figure 4: PE's internal organization

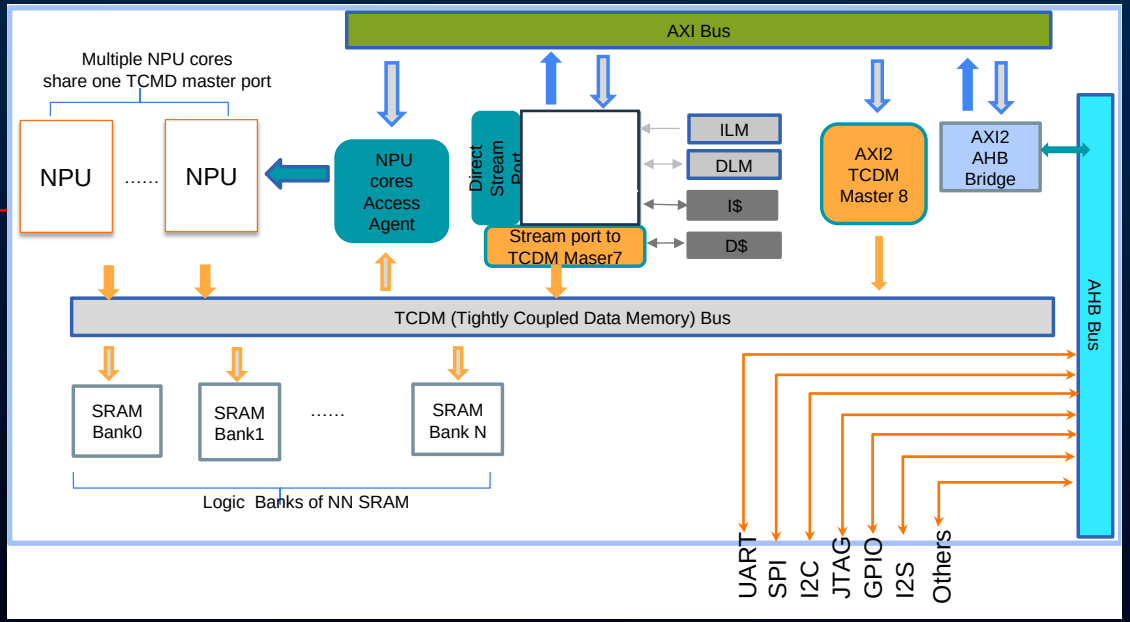
All photos: courtesy of ACM

Edge AI With Analog In-Memory Computing

- TetraMem Analog In-Memory-Computing MX200 (RRAM-based)
- 8-bit 256x256 (64K) MAC Engines, >30 TOPS/W performance
- ML core operators (conv, gemm) processed in NPU
- Remaining operations processed in RISC-V Vector processors and control CPU

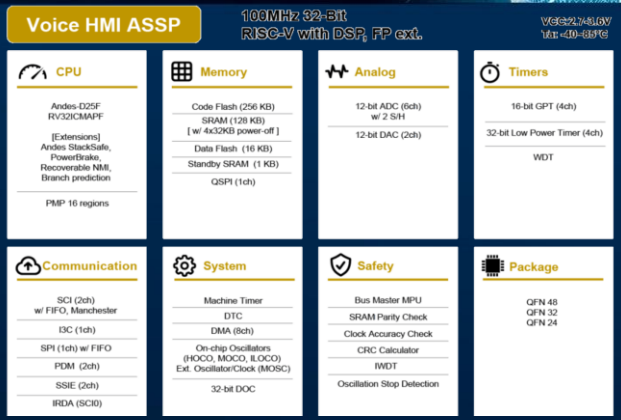


Powered by 8 bits multi-level RRAM device



Endpoint AI

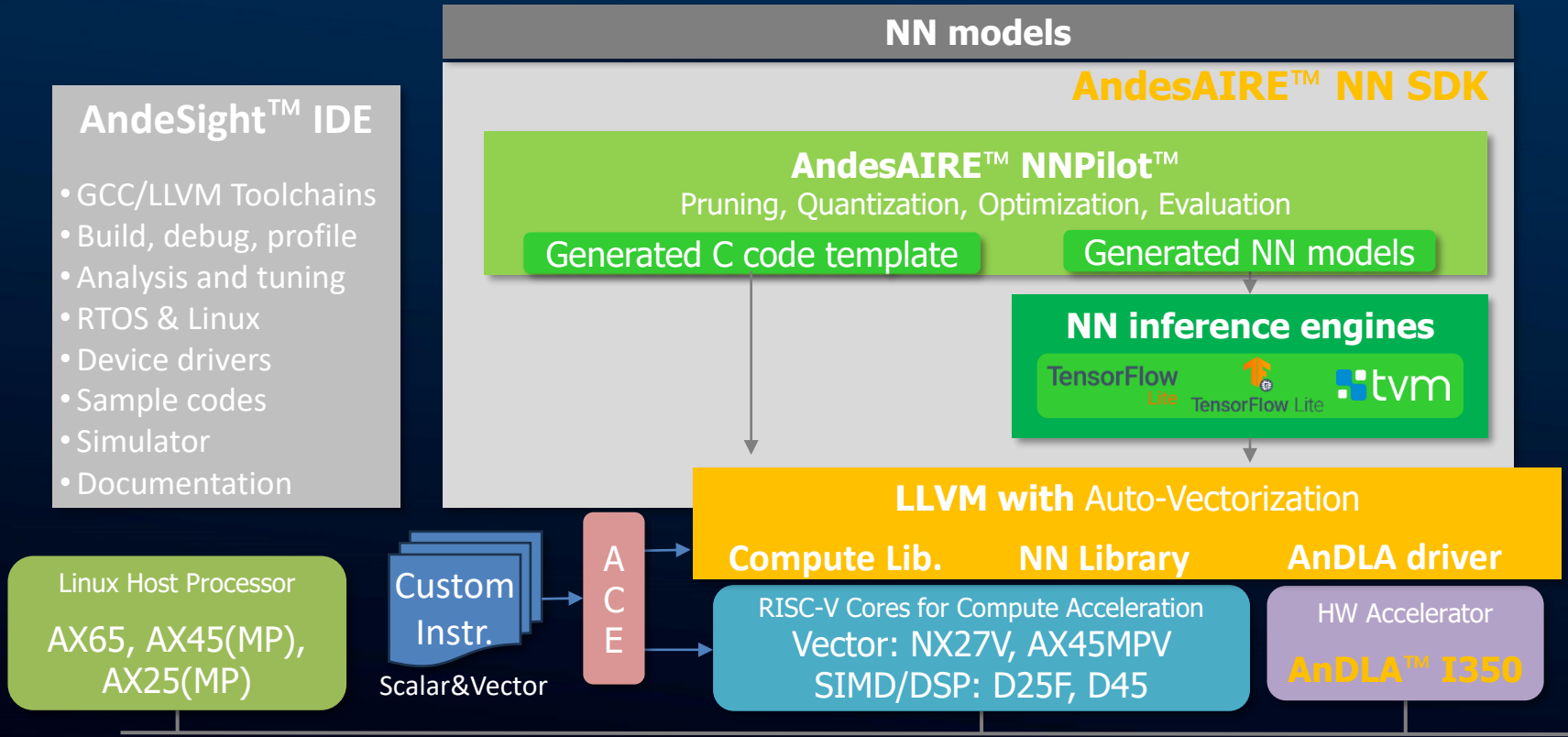
- Renesas R9A06G150 Voice-Control ASSP
  - With 100MHz DSP-capable D25F processor
  - ML-based voice recognition gets >50% speedup by using P-extension



- Spacetouch SPV60 Intelligent audio processor
  - High performance for customer development
    - 100 GOPS NPU for noise reduction, echo cancellation, howling suppression
    - uDSP for FFT/IFFT, atan, log, etc.
    - 400MHz D25F with ID caches/Local Memory
  - Rich audio interfaces and other peripherals
  - Applications:
    - Intelligent voice, smart earphone, professional audio

AndesAIRE™: Andes AI Runs Everywhere

HW/SW Solutions for AI from the Edge to the Cloud



AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera

Smart Sensor

Smart Home Appliance

AIoT / tinyML

Robotics

Wearable

RISC-V growth momentum Led by Industrial Leader

BOSCH Infineon NXP NORDIC SEMICONDUCTOR
Leading Semiconductor Industry Players Join Forces to Accelerate RISC-V
Aug. 2023

RENESAS
Renesas Extends Leading RISC-V Embedded Processing Portfolio with New Motor Control ASSP Solution
Sep. 2022

mobileye An Intel Company
Intel Mobileye EyeQ Ultra RISC-V processor targets Level 4 autonomous driving
Jan. 2022

European Processor Initiative epi
European processor project shows shift to RISC-V
Dec. 2021

NSI-TEXE
NSITEXE achieves world's first RISC-V processor with vector extension certified for ISO 26262 ASIL D ready product
Aug. 2021

Rambus
RISC-V crypto core is qualified to ASIL-D for automotive designs
Jan. 2020

Kneron
Kneron Unveils Its First RISC-V SoC Built for Autonomous, Assisted Driving
Nov. 2021

ILITEK
I Love Innovation
Andes and IAR Together Enable Leading Vendor ILITEK to Accelerate the Development of its ISO 26262 Ready TDDI SoC ILI6600A
Feb. 2023

iar
Andes and IAR Systems enable leading automotive-focused IC design companies to accelerate time to market
Mar. 2022

Green Hills SOFTWARE
Andes Technology and Green Hills Software Team Up to Deliver Advanced Automotive Safety Platform for RISC-V
Aug. 2022

imperas
NSITEXE Selects ImperasDV for Automotive Quality RISC-V Processor Functional Design Verification
May 2022

Virtual Open Systems
VOSySmonitoRV, a Secure Monitor Layer for RISC-V Architecture Mixed-Critical Systems

PARASOFT
Andes Technology and Parasoft Collaborate to Provide Seamless Software Testing Tools for Automotive Functional Safety Applications
Dec. 2022

LDRA
Andes Technology Collaborates with LDRA to Deliver Integrated Tool Suite for Safety-Critical Software on Andes RISC-V CPU Solutions
Jan. 2023

Solid Sands
Upgrade to Solid Sands' latest SuperTest version supports Andes to its ambitions for further growth in the automotive sector
May 2023

Andes is Supporting RISC-V for Automobiles

Since founded in March 2005,
Andes Technology is working step-by-step on
RISC-V for ISO 26262 Functional Safety

2016

Andes Joined RISC-V Foundation as one of the Founding Members

- Promoted as Founding Premier Member of RISC-V International in **2019**

2017

The First RISC-V Architecture AndesCore™ NX25 and N25 Released

- 25-Series became one of world's most licensed RISC-V CPUs

2020

Andes Development Process Certified for ISO 26262

- Andes became the first ISO 26262 certified RISC-V CPU IP supplier in the world

2022

AndesCore™ N25F-SE Certified for ISO 26262

- N25F-SE became the first full compliant ISO 26262 certified RISC-V CPU in the world

2024

AndesCore™ D25F-SE to be Released

- A series of Andes Functional Safety CPU cores will soon follow

AndesCore™ for Automotive Electronics

- **Supporting a Wide Variety of Functional Safety Applications:**
  - Dashboard display, in-car monitoring, keyless entry, lighting control, tire pressure monitoring, vision ADAS, microcontroller and many more
- **Developers using AndesCore™ Functional Safety Processors to:**
  - Introduce new electronic systems on automobiles
  - Upgrade existing systems that needs to be ISO 26262 compliant

In-car Monitoring

Head Lights

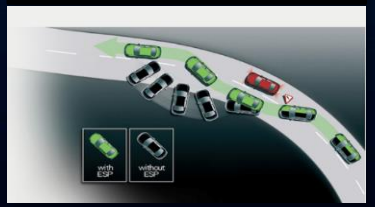
Keyless Control

Blind Spot Monitor

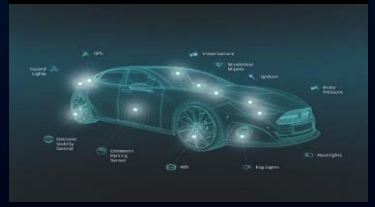
Touch & Display

EPS

ESC



Sensors & Actuators

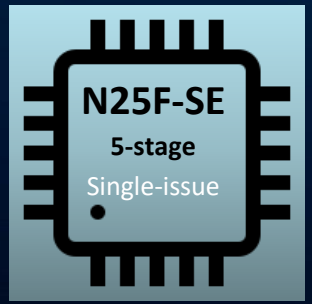


BMS

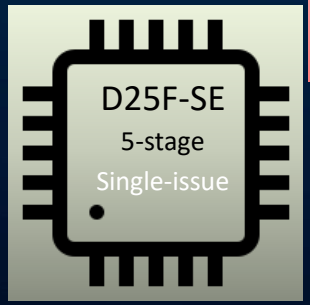
Andes FUSA Roadmap

Computing Power

Mainstream Processing

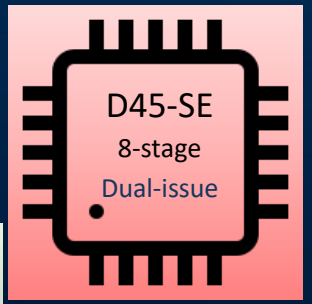


ASIL-B Compliant
IP: Available now
Already Certified



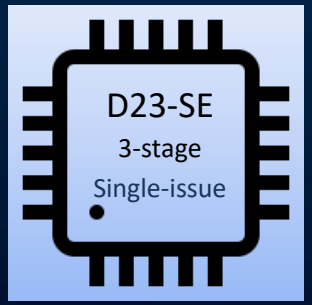
ASIL-B Compliant
IP: Available now
Certified: Q1, 2024

Mission Critical



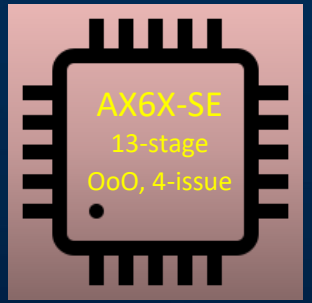
ASIL-D Compliant
ASIL-B Supported
IP: Available now
Certified: Q3, 2024

Low Power & Security



ASIL-D Compliant
ASIL-B Supported
IP: Q2, 2024
Certified: Q4, 2024

High Performance



ASIL-D Compliant

2023 2024 2025 2026

Andes Automotive Ecosystem

- Co-working with global leading suppliers in the automotive industry
- Andes and ecosystem partners jointly deliver the trusted RISC-V automotive solutions to designers complying with the standard of functional safety ISO 26262
- Partner Ecosystem Catalogs

Security

- Rambus — HSM / RoT
- SECURE-IC — Securyzr™ SE
- Virtual Open Systems — VOSySmonitoRV
- 豆荚 Beanpod, KTrustKernel — TEE

Safety RTOS

- WITTENSTEIN — SAFERTOS
- Microsoft — Microsoft Azure RTOS
- WNDRVR — VxWorks

AUTOSAR

- VECTOR — AUTOSAR
- SIEMENS — Capital VSTAR, Nucleus SafetyCert
- FPT Fpt Software — MaaZ AUTOSAR

Compiler / Debugger

- iar — EWRISCV
- Green Hills SOFTWARE — MULTI IDE / Compiler RTOS
- TASKING — RiscFree IDE/Compiler
- ASHLING — Compiler
- LAUTERBACH DEVELOPMENT TOOLS — TRACE32 Debugger

Tool

- LDRA ASSURED — LDRA Tool Suite
- PARASOFT — Parasoft C/C++ Test

The R&D Power for The Future

Andes RISC-V CPU Cores

AX60 Series 13-stage OOO Linux MP		AX65	AX66	AX6X-SE	A72~A78; N1/V1/X1
Categories	*Power-efficient*	*Mid-range*	*Extended*	*FUSA*	
45 Series 8-stage Superscalar	N45, NX45	D45	AX45MPV A45(MP), AX45(MP)	D45-SE	A53/55, R52/ R82, M7
27 Series 5-stage MemBoost		NX27V	A27(L2), AX27(L2)		A5/7/35
25 Series 5-stage Fast&Compact	N25F, NX25F	D25F	A25(MP), AX25(MP)	D25F-SE N25F-SE	A5/7/35, R4/5, M4/33
Compact Series	N22, N225	D23		D23-SE	M0/0+/3/33/4
Categories	*Embedded Control*	*Compute Acc.*	*Linux AP*	*FUSA*	*References*

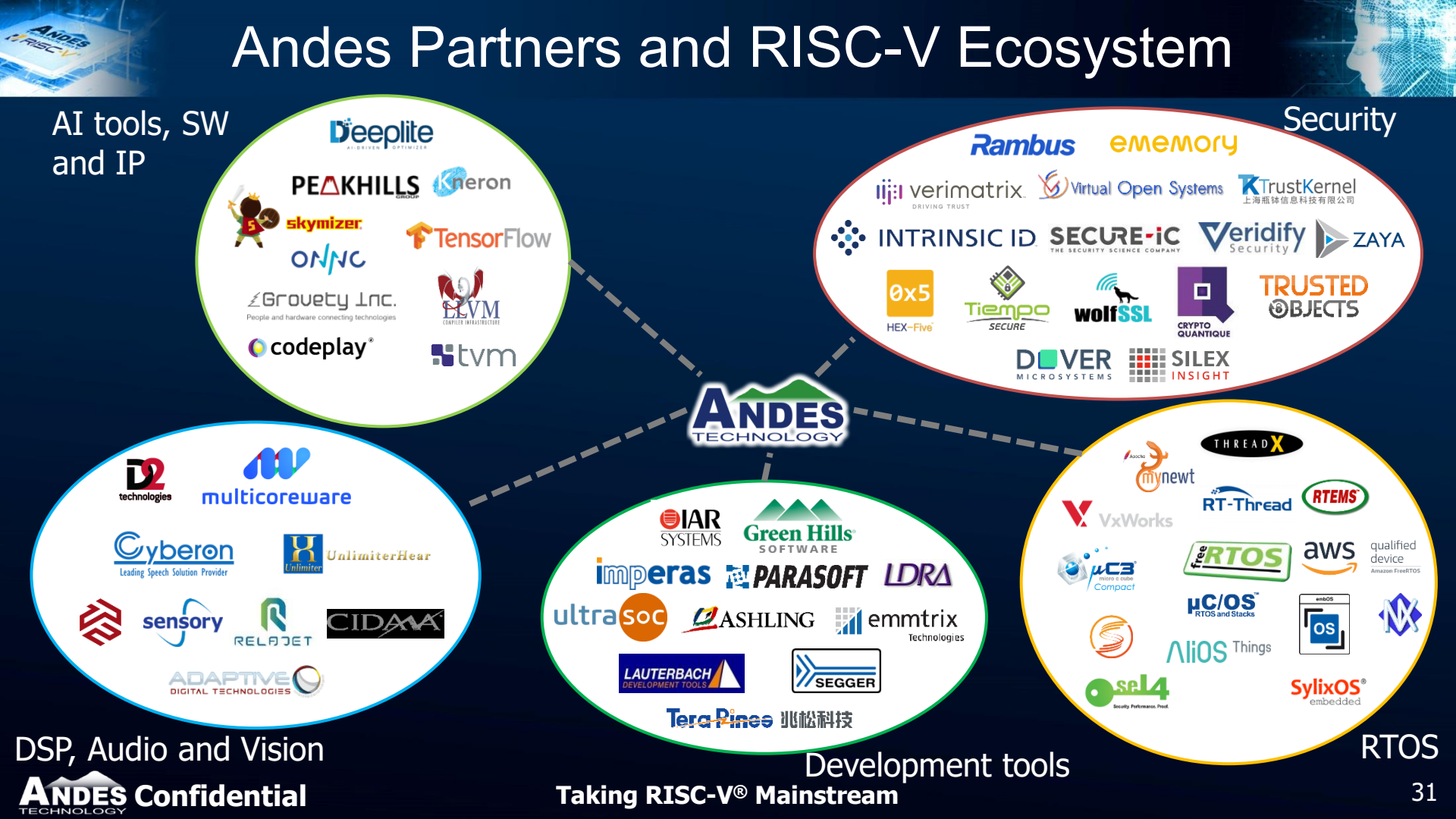
- **To be released in 2024:** D25F-SE, D45-SE, AX66
- **Under Planning :** D23-SE, AX6X-SE

Note: roadmap subject to change without notice

RISC-V Continues to RISE Rapidly

- **RISE: RISC-V Software Ecosystem, a project under LF Europe**
- **To accelerate the development of RISC-V open source SW**
- **Led by industry leaders**
- **Areas to focus over time:**
  - Compilers & Toolchains
  - Language Runtimes
  - System Libraries
  - Debug & Profiling Tools
  - Simulator/Emulators
  - Kernel and Virtualization
  - Linus Distro Integration
  - System Firmware
- **More at *https://riseproject.dev***

Andes Partners and RISC-V Ecosystem



Extend technical capabilities to grow and share results

回顧2021年GDR募資及成果

- **2021 Q3 $127M GDR was raised**
- **All projects planed in GDR roadshow all kicked off, with one more project kicked-off: Andes new office**
  - Design centers expansion (200 worldwide experts) were smooth, and getting stabilized now, R&D results with such expansion started to show up
- **In 2023 Q4 AX65 IP was released, it started with counting ROI of GDR**
- **Estimate 2024 to 2026 will be peak of products development output with 2021 GDR raised, which in turn will bring in new stream of revenue growth**

Andes Future project pipeline – Beyond Current Roadmap

Project I
Qilai

Platform Chip with AX45MP + NX27V+ high-speed interfaces

- **Potential applications:** Office productivity tools, Image processing tools, Web browsers, Scientific computation libraries, AI infrastructure

Project II
Makadou

Next Generation High-end RISC-V Core for Edge AI/Tablet/Automotive

- **Potential applications:** Edge AI, Tablet, Automotive electronics, Advanced Driver Assistance Systems

Project III
Cuzco

Server-grade RISC-V core for Datacenter AI/Desktop/HPC

- **Potential applications:** Datacenter AI, Desktop PC/Server, High-Performance Computing

新聞稿 2021-10-29

晶心科技發行GDR 於盧森堡證券交易所上市 拓展業務

加州聖荷西 – 2021 年 10 月 29 日 – RISC-V CPU IP 領先供應商晶心科技 (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099) 今天宣布成功發行海外存託憑證 (GDR)。日盧森堡證券交易所上市。每份新發行的海外存託憑證單位將代表2股普通股，其初始市值定價為31.78美元，約合每股新台幣440元。總共發行400萬股，相當於800萬股普通股。海外募資總額約1.27億美元（新台幣35.17億元）。晶心科技是目前唯一上市的RISC-V CPU IP供應商，GDR股東主要是尋求長期投資的境外機構投資者。

晶心科技主席兼行政總裁林富豪表示：“此次融資讓晶心科技實現了推動中長期研發資本投入、擴大產品線，特別是高端產品的主要目標。”「此外，全球投資者能夠分享快速成長的 RISC-V 市場。為滿足RISC-V高階運算解決方案的迫切需求，這筆資金將主要用於加速產品設計中心的擴建，以強化我們現有領先的RISC-V產品組合，並加快開發高價值和高價值的產品。高階RISC-V CPU IP和SoC軟硬體整合解決方案。為了搶佔高利潤的高階多核心CPU IP市場並提升銷售勢頭，晶心科技位於台灣、美國和加拿大的設計中心計劃招募200名研發人才，開發下一代RISC-V產品，應用於5G等應用、人工智慧/機器學習、HPC、ADAS、汽車電子、AR/VR、區塊鏈、雲端運算、資料中心、伺服器、物聯網、MCU、儲存設備、安防、無線設備等大量高效能運算市場」。

晶心科技報告，2021年上半年營收年增72.6%，其中63%的營收來自RISC-V產品，包括標準IP授權和客製化運算業務。此外，2020年的收入較2018年晶心開始交付最初的RISC-V核心時幾乎翻了一番。根據 Counterpoint Research 的最新報告，隨著半導體解決方案需要越來越多的多功能IP，純半導體IP 市場規模將以11% 的複合年增長率增長，到2025 年達到每年86 億美元。RISC-V由於其開源性，正在快速成長。優點在於，功耗優化更容易、安全功能可靠、政治風險影響更低。RISC-V處理器將繼續在包括物聯網、工業和汽車在內的多個類別中快速採用，到2025年，這些領域的採用率將分別達到28%、12%和10%。這些市場擴張的有利因素將有利於晶心科技及其子公司顧客。

Andes Technology USA Corp. Announces Major Expansion of Its U.S. Operation

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Company Announces Job Openings for San Jose Headquarters and Portland R&D Office

San Jose, California October 8, 2021 – Andes Technology USA Corp., the headquarters of North America operations of Hsinchu, Taiwan-based Andes Technology Corporation, a leading supplier of high efficiency, low-power 32/64-bit RISC-V processor cores and founding premier member of RISC-V International, today announced a major expansion of Its U.S. operation. Andes Technology USA is greatly increasing engineering headcount in both the San Jose, California headquarters and its Portland, Oregon research and development facility. Andes Technology USA is seeking engineers in the U.S. and Canada to work remotely or in the Portland or San Jose offices. Openings are available for design engineers, verification engineers, and field application engineers.

Andes Technology USA Corp. was established in 2015 as a California corporation coincident with Andes Technology Corp. joining RISC-V International. After Andes took the RISC-V instruction set architecture (ISA) as the base to form its fifth generation architecture, AndeStar™ V5 and started developing V5 processor IP's, the U.S. operation was formed to be nearby early customer adopters of the new ISA. The U.S. subsidiary established an R&D lab shortly thereafter and began developing architectures for the high-end RISC-V processors. In under a year the investment together with the main engineering team in Taiwan yielded the first commercial RISC-V Vector processor IP which won nearly 10 projects including datacenter projects from a large OEM so far.

"Major semiconductor companies worldwide adopting the RISC-V ISA and the RISC-V International work groups rapid development of the RISC-V ISA extensions is driving demand for engineers to keep up with the fast pace of new technology development," said Emerson Hsiao, Andes Technology USA Corp. Chief Operating Officer. "RISC-V customers like the growing number of extensions coming available as well as their ability to customize the architecture to better fit their processing requirements. Our tool Andes

2024 Andes RISC-V Con Hsin-Chu

- 2024, 3, 28
- 3A1S

晶心RISC-V CON 新竹

2024-03-28 @ 13:00 - 18:00

Support domestic enterprises, research institutions, and universities to participate in the Chip-driven industrial innovation plan

License Fees

- ✓ For projects producing fewer than or equal to 1000 chips, the authorization fee is Y% off the list price.
- ✓ For projects producing more than 1000 chips, it is considered mass production, and the authorization fee is X% off the list price.

Annual technical maintenance and product update fees:

- ✓ Under standard commercial conditions: Z% of the authorization fee.
- ✓ Under the Crystal Innovation Project: W% of the authorization fee.
- Fees are payable to Andes Technology only upon approval of the Crystal Innovation Project application. If the final project is not approved, the contracting party may revoke the contract.
- Both parties should discuss the reasonableness of integrating the overall project plan and fees payable to Andes Technology in advance.

二、推動領域及補助範疇

驅動臺灣業[illegible]標之晶片設計開發

R&D direction in line with chip innovation plan and industry trends

■ 補助

一. 創新技術之先進晶片開發，採用7nm (含)以下製程。

二. 先進異質整合封裝技術之創新晶片(如小晶片整合封裝模組、矽光子等其他新興應用晶片開發)。

三. 異質整合微機電感測技術之創新晶片開發，採用0.35μm(含)以下之晶圓級製程。

四. 優先推動人工智慧、高效能運算、車用電子、下世代通訊等四領域，規格如下：

Data: Ministry of Economic Affairs

一、人工智慧：

✓伺服器(推論)：算力 > 500 TOPS
✓裝置端：算力 > 80 TOPS

二、高效能運算：

✓ 算力 > 500 TOPS

三、車用電子：

✓輔助駕駛：算力 > 80 TOPS(L2+)
✓智慧座艙：算力 > 40 TOPS

四、下世代通訊

✓無線傳輸
B5G/6G >15 Gbps以上；Wifi >20 Gbps以上
✓有線傳輸 >800 Gbps以上

註：TOPS(Tera Operations Per Second for INT8; 每秒一兆次操作)

Thank you