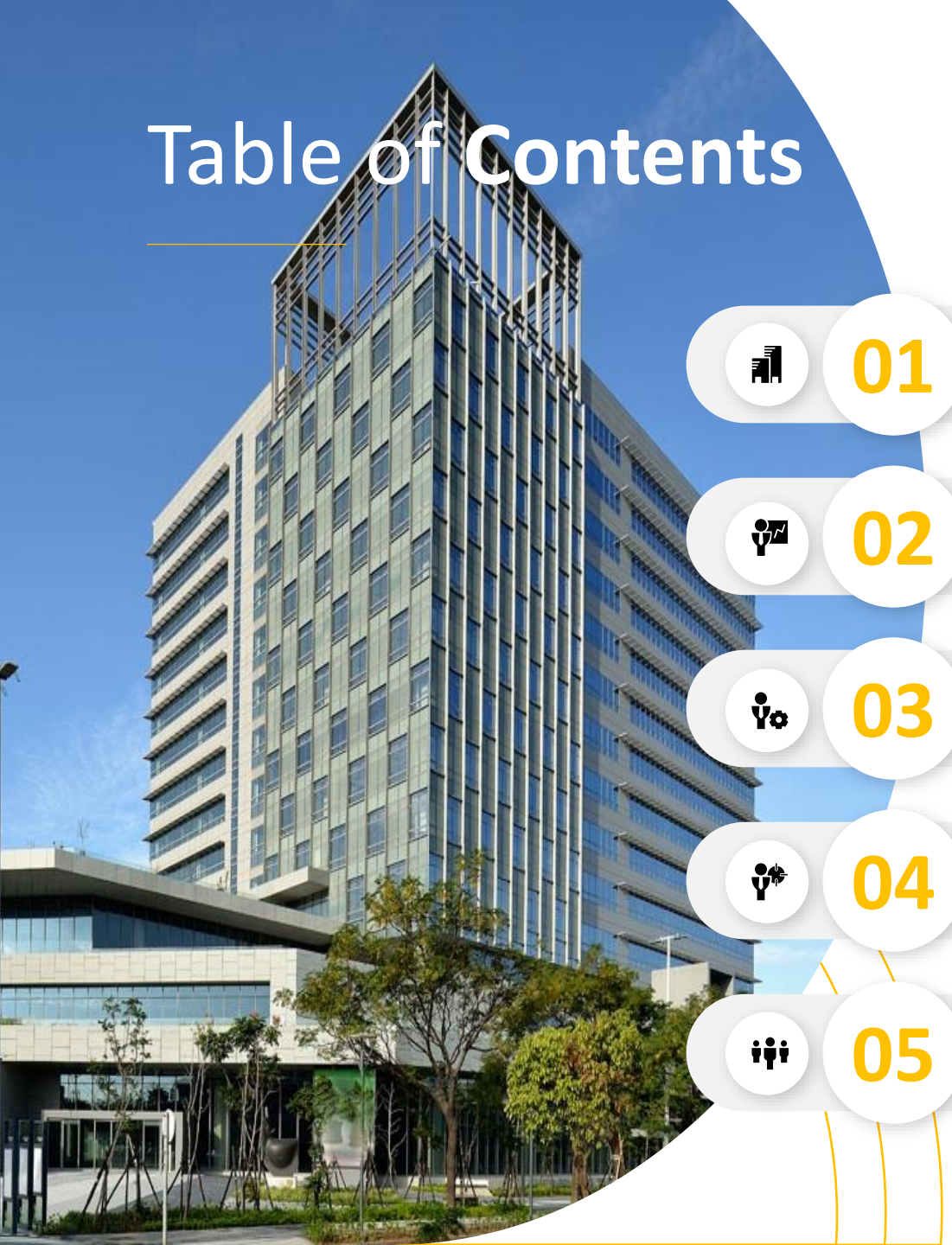
Andes Technology Corp.
Investor Conference Report

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.



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Company Overview

http://www.andestech.com

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 450 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- Al Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- EE Awards - “Taiwan-Product Award” & ”Asia-Company Award” (2021)
- Top 500 High-Growth Companies Asia-Pacific (2023)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

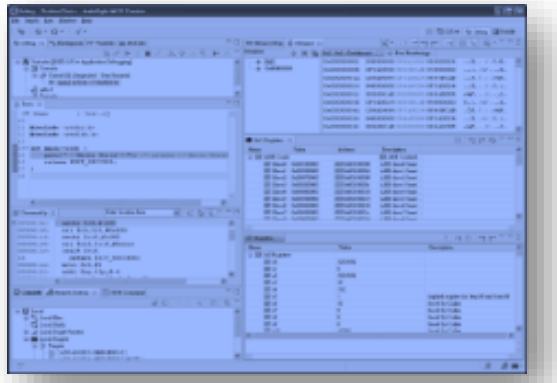
Emerging Opportunities

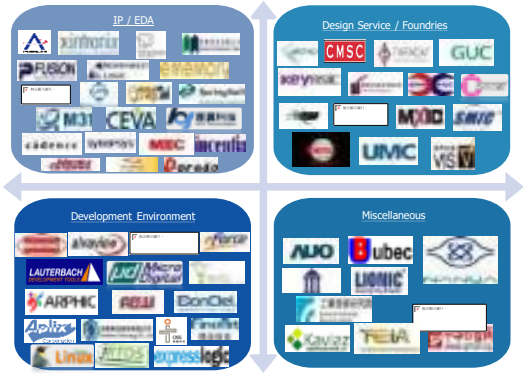
- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

ANDES TECHNOLOGY

Business Status Overview

- **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed
- AndeSight™ IDE:
  - **25,000+** installations
- Eco-system:
  - **500+** partners
- **>13B** Accumulative SoC Shipped



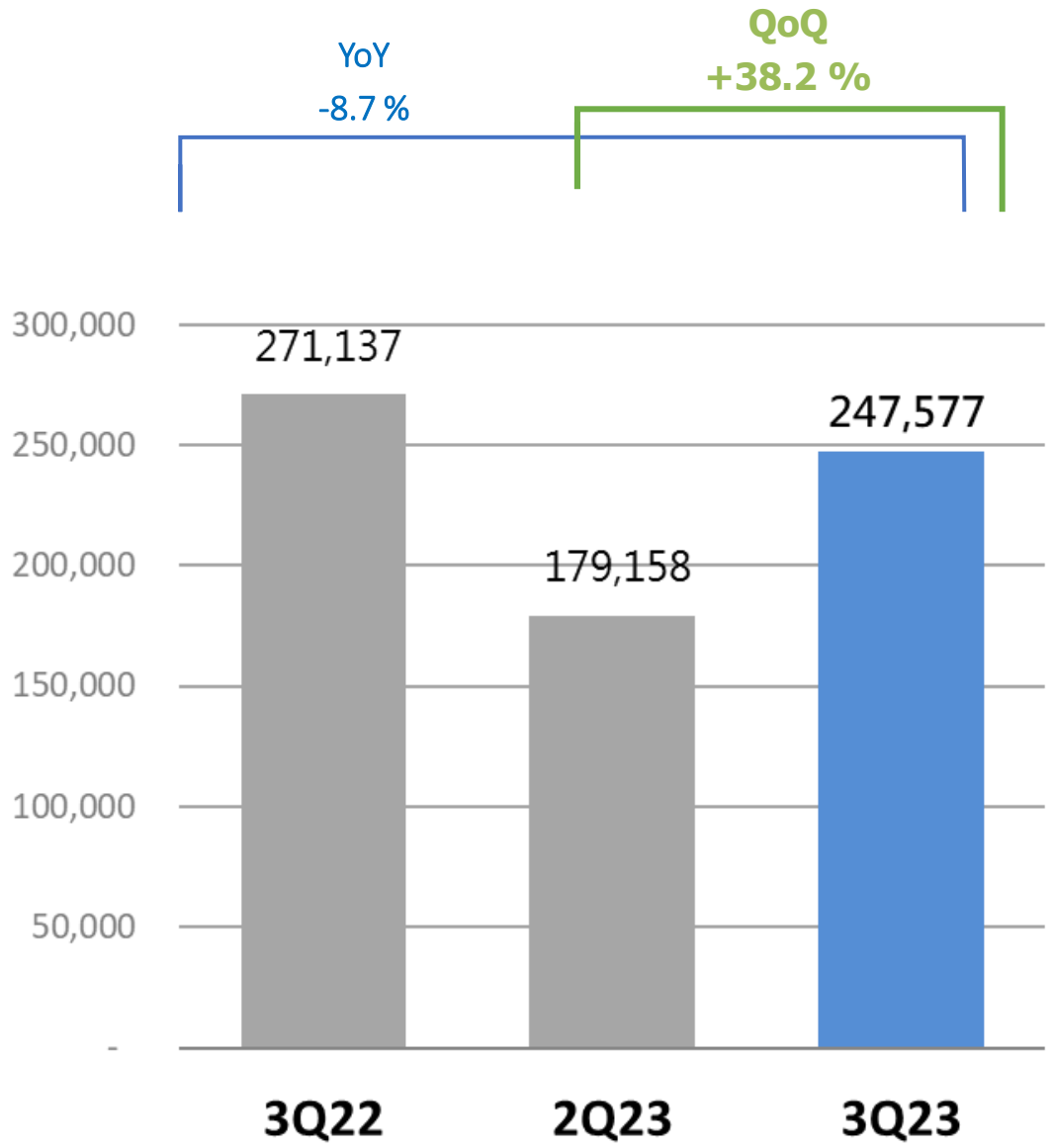


Operation Results

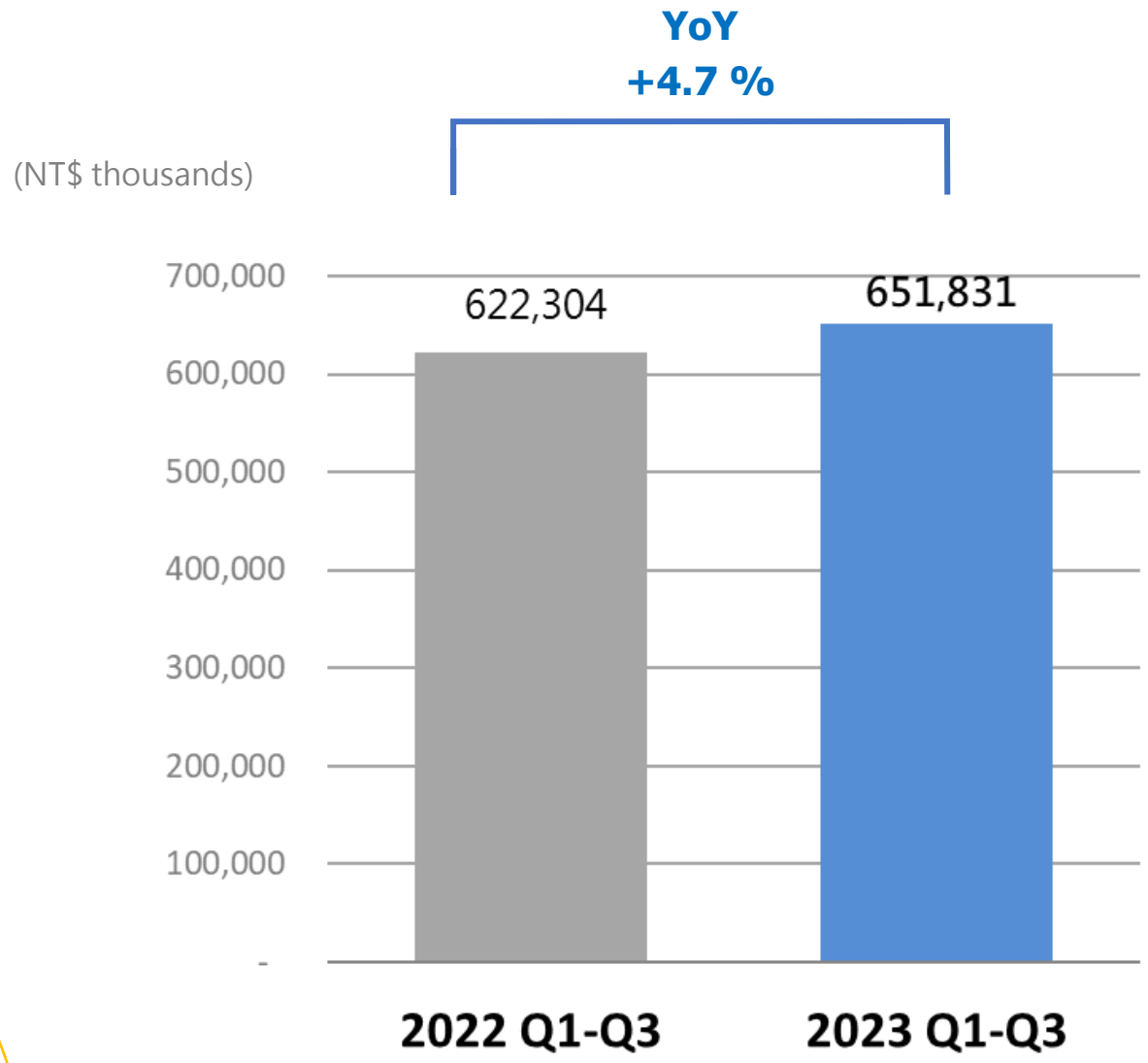
http://www.andestech.com

3Q23 Revenue Analysis

(NT$ thousands)

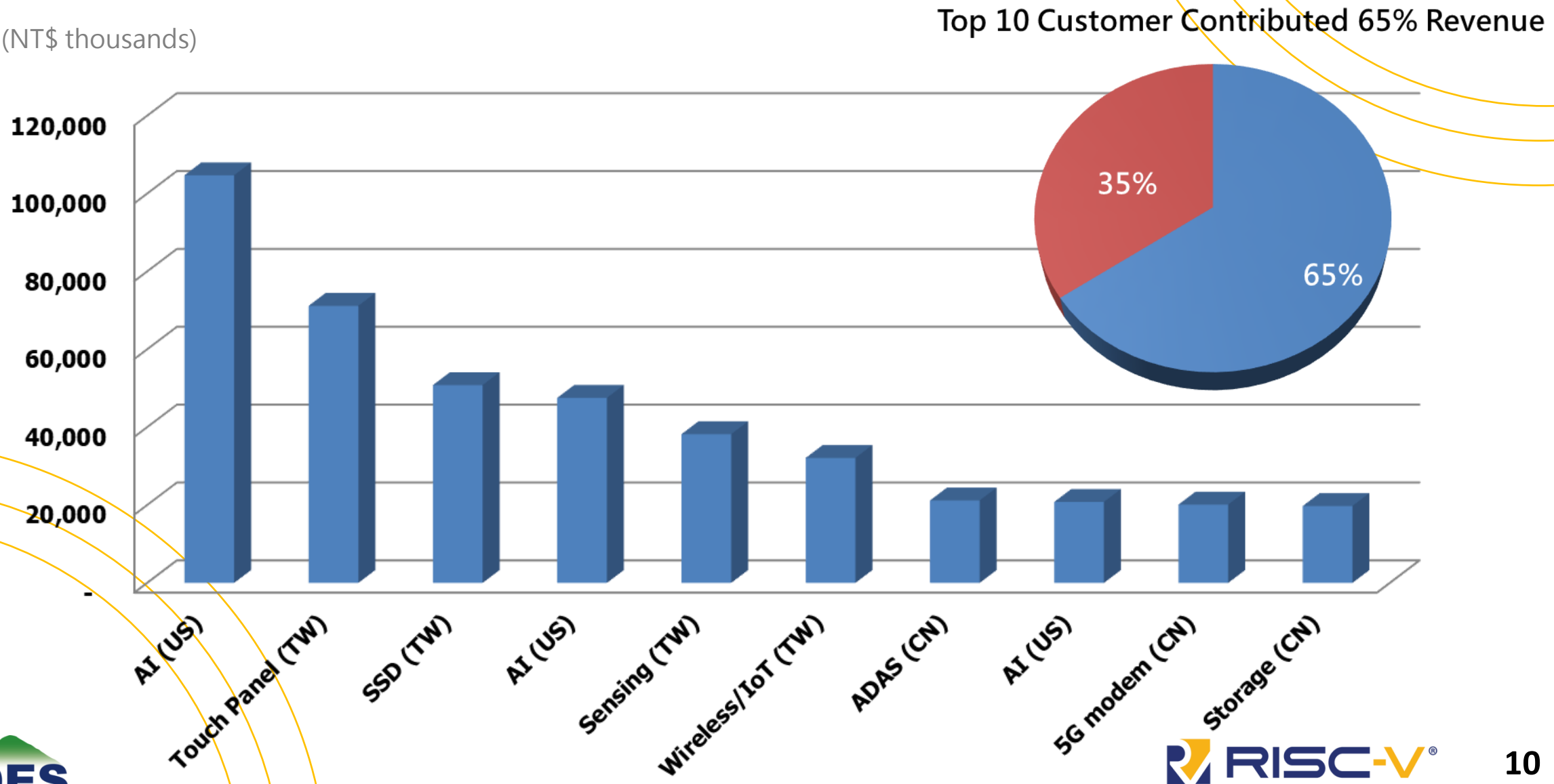


23Q1-Q3 Revenue Analysis

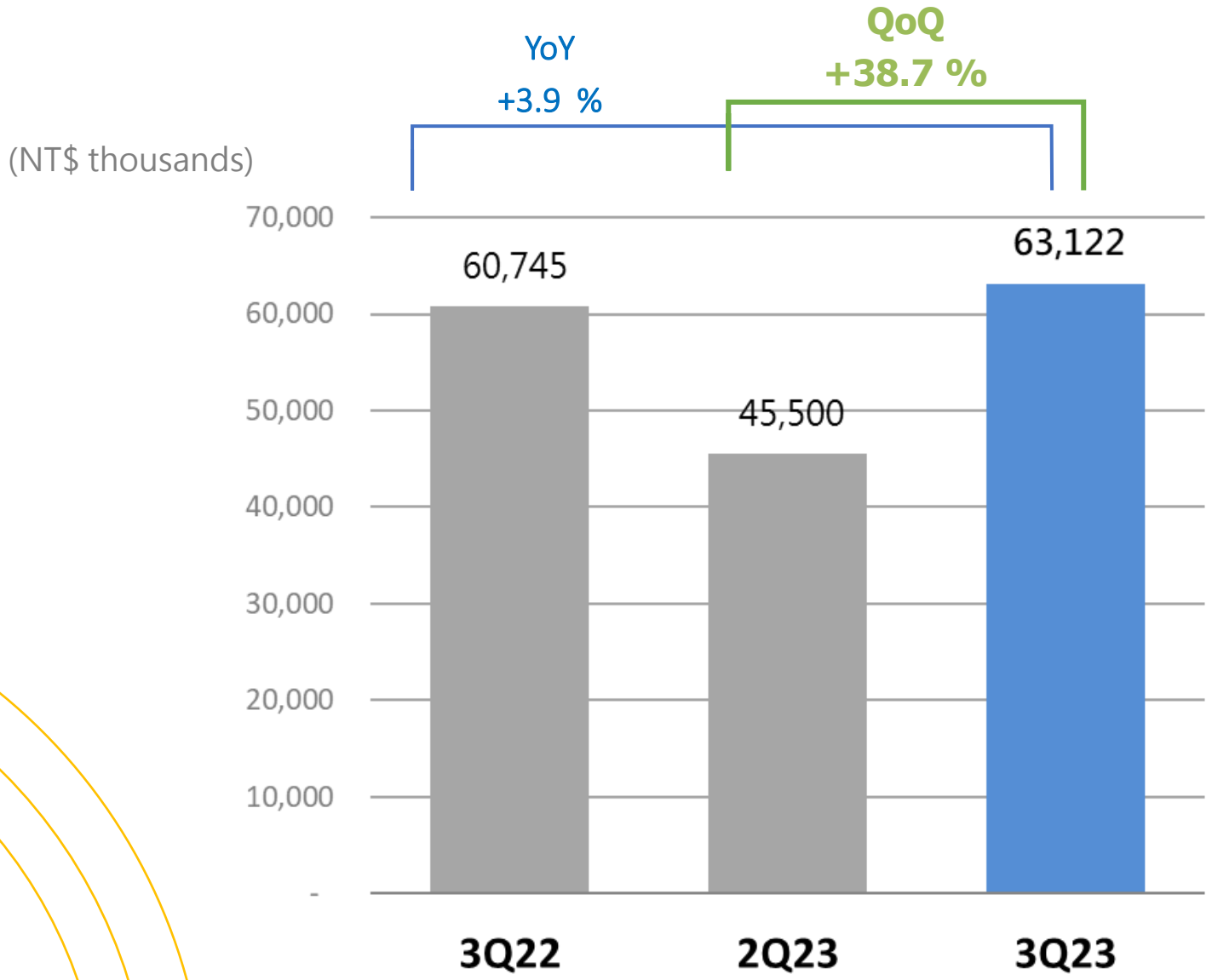


23Q1-Q3 Top 10 Customers Analysis by Revenue

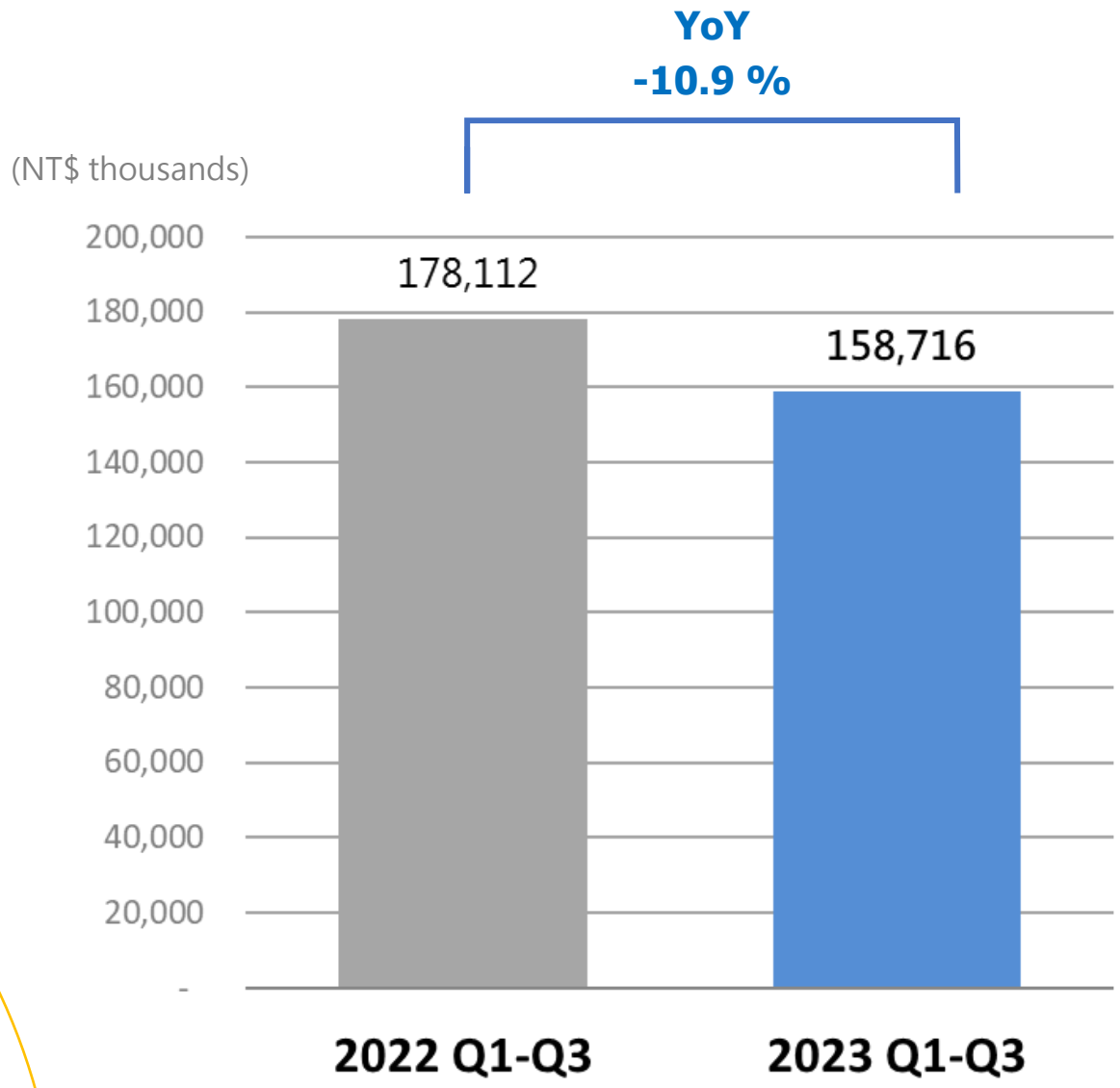
(NT$ thousands)



3Q23 Royalty Analysis

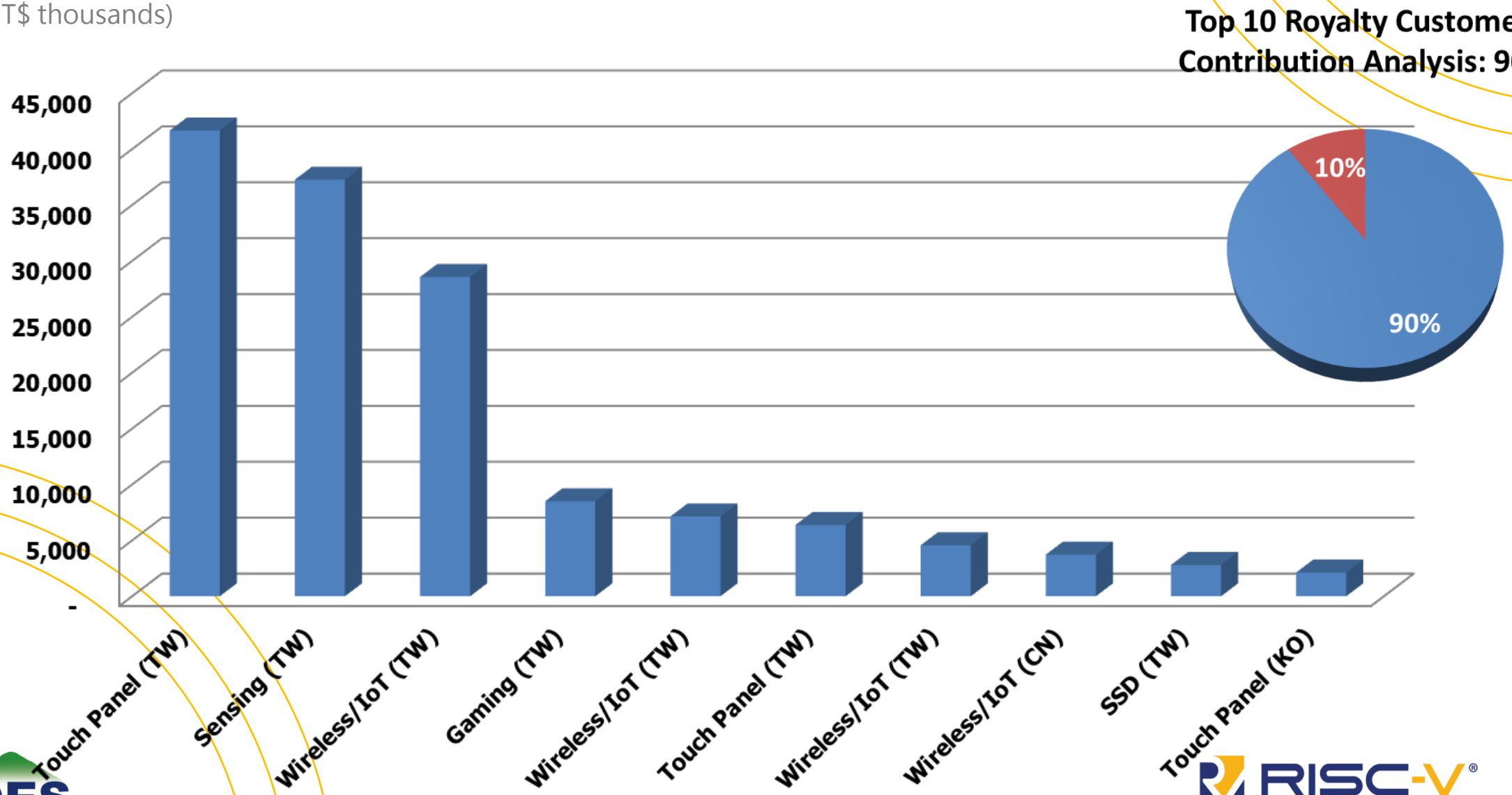


23Q1-Q3 Royalty Analysis

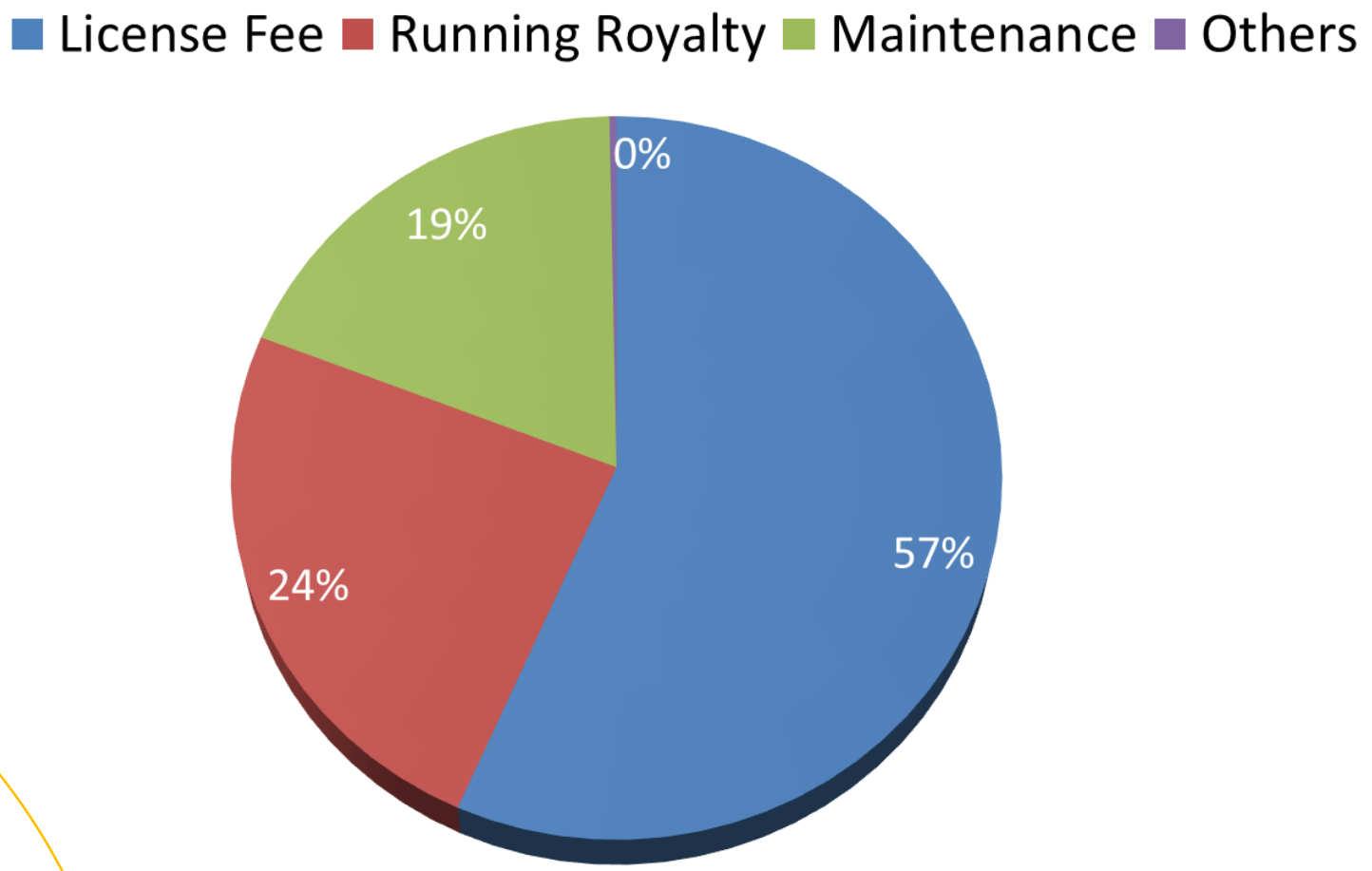


23Q1-Q3 Top 10 Royalty Contributors Analysis by Applicat

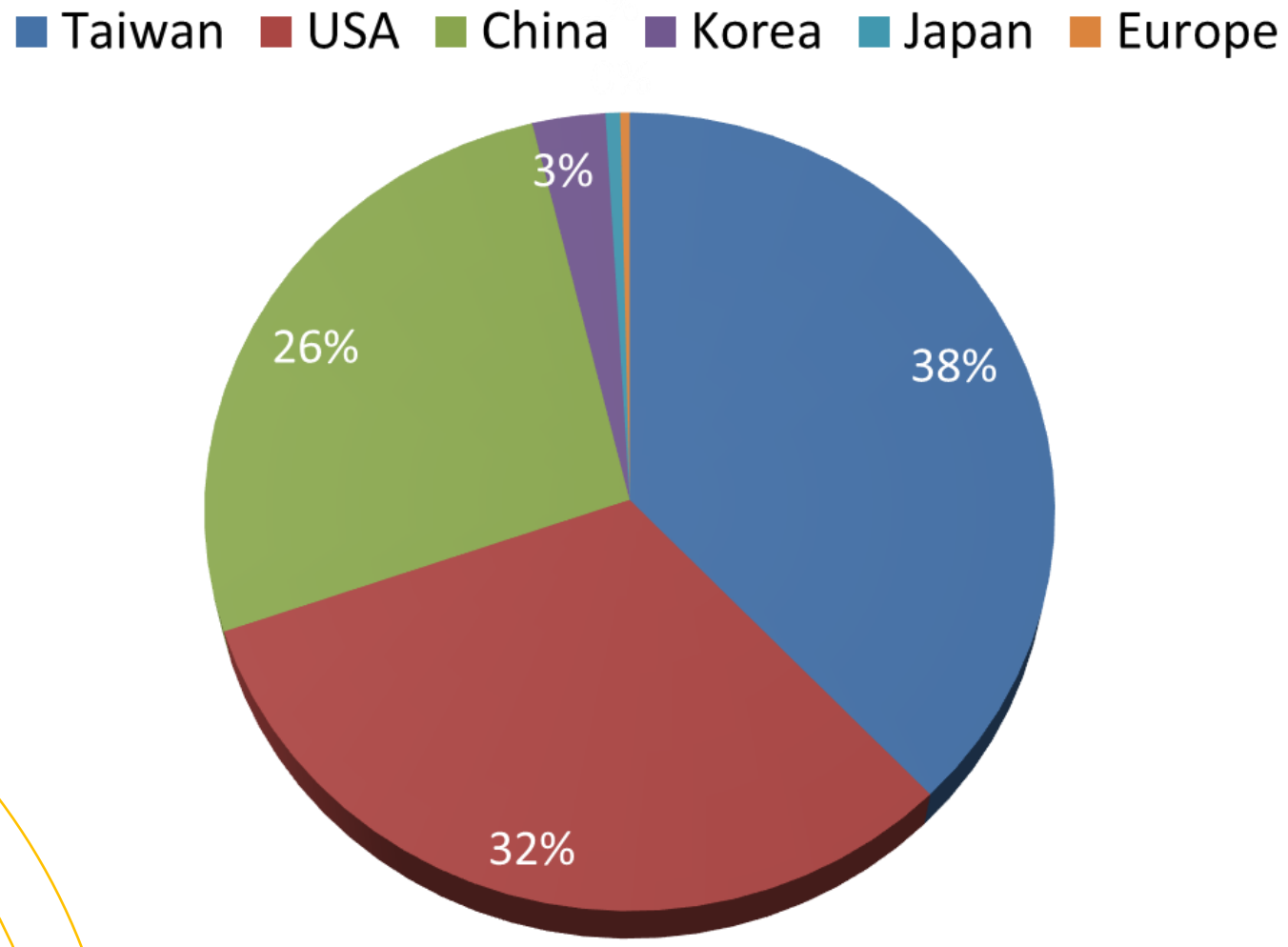
(NT$ thousands)



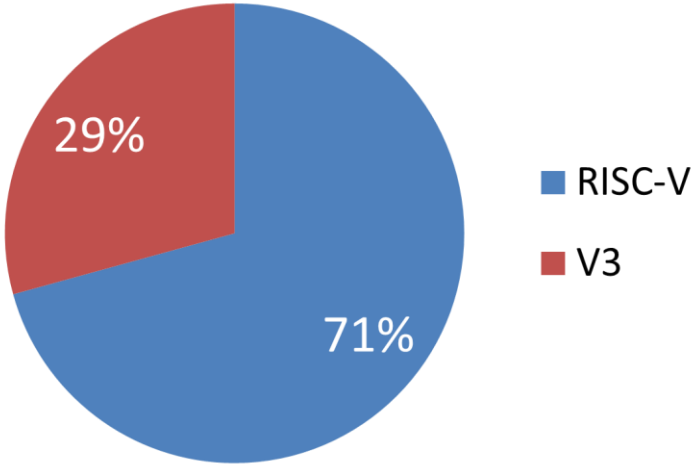
23Q1-Q3 Revenue Analysis by Payment Model

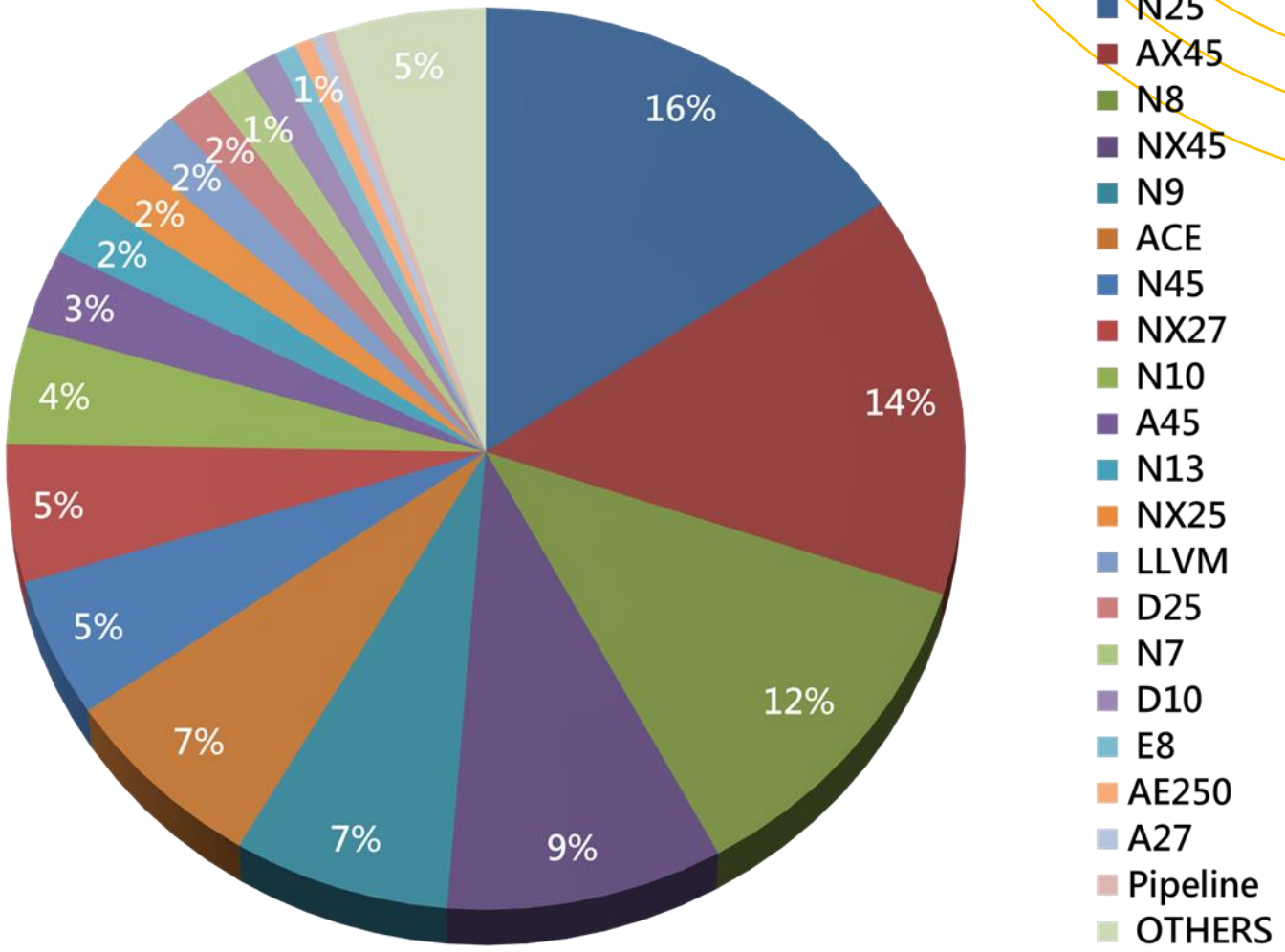


23Q1-Q3 Revenue Analysis by Region



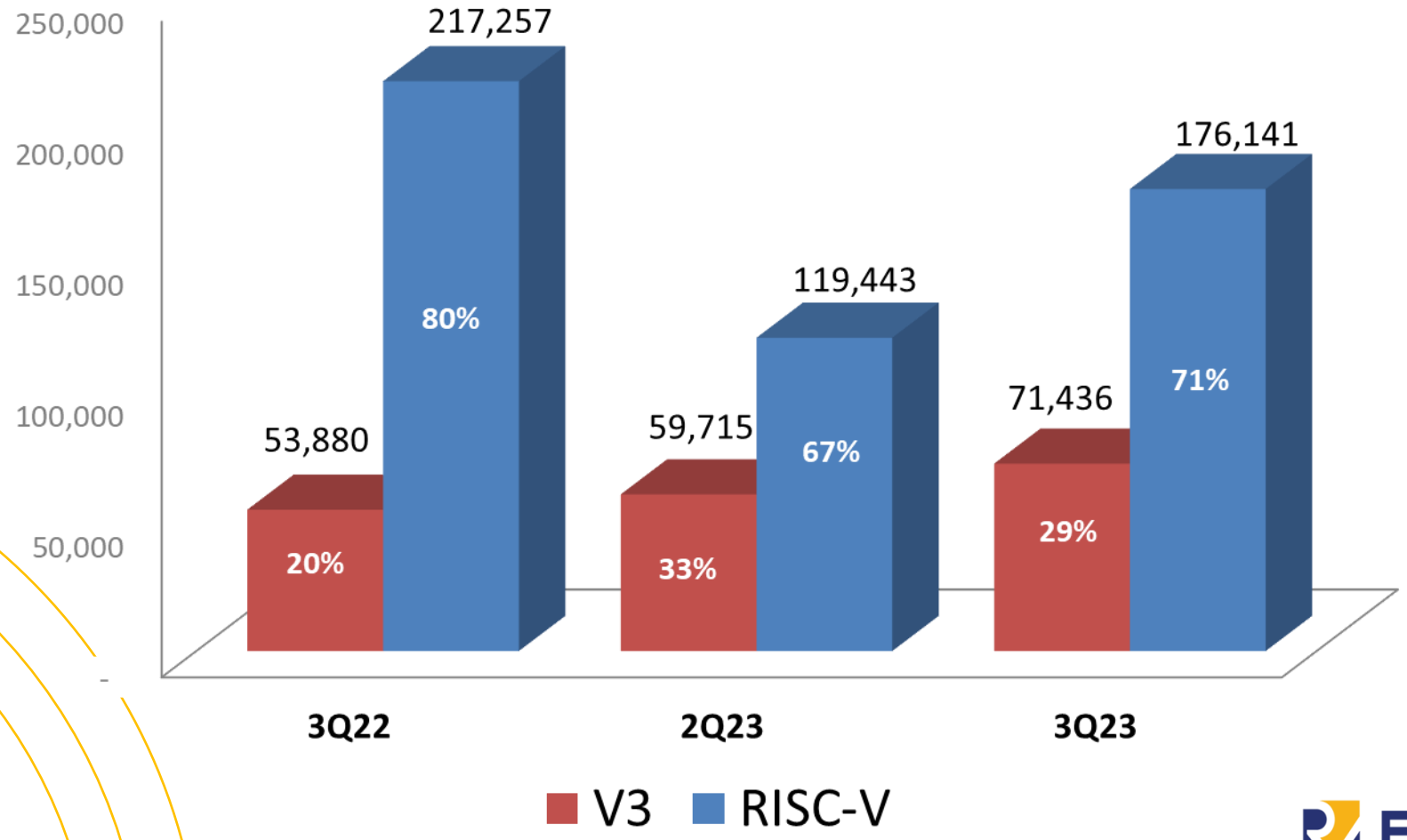
23Q1-Q3 Revenue Analysis by Product





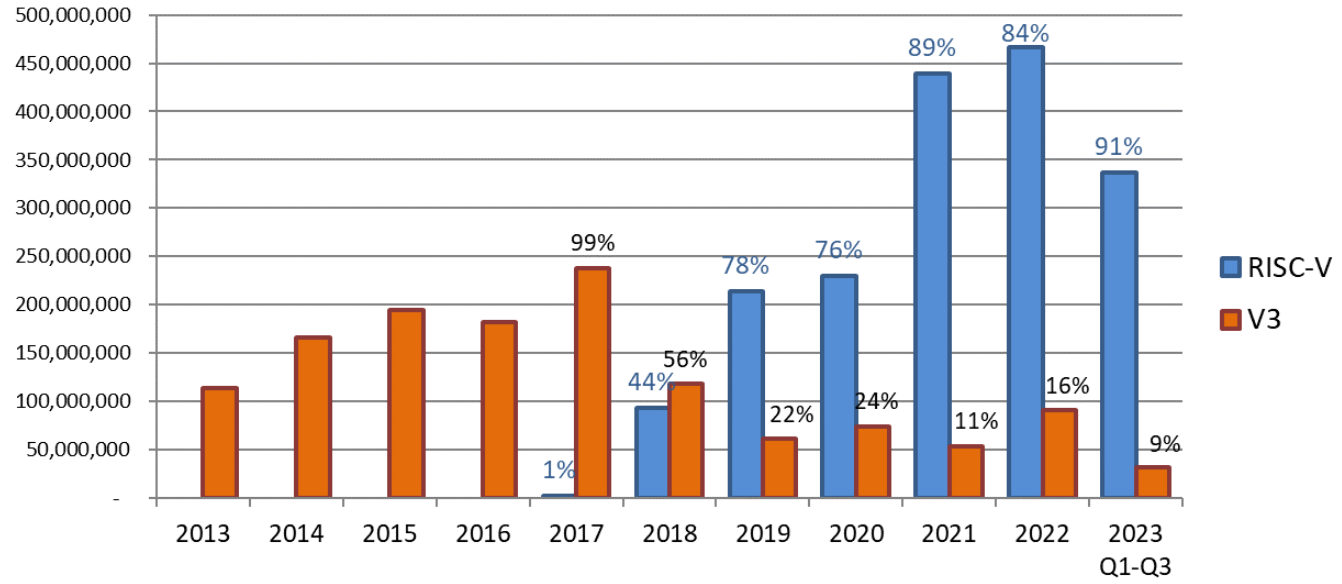
3Q23 Revenue Analysis - RISC-V

(NT$ thousands)



Historical Revenue Analysis

(NT$)



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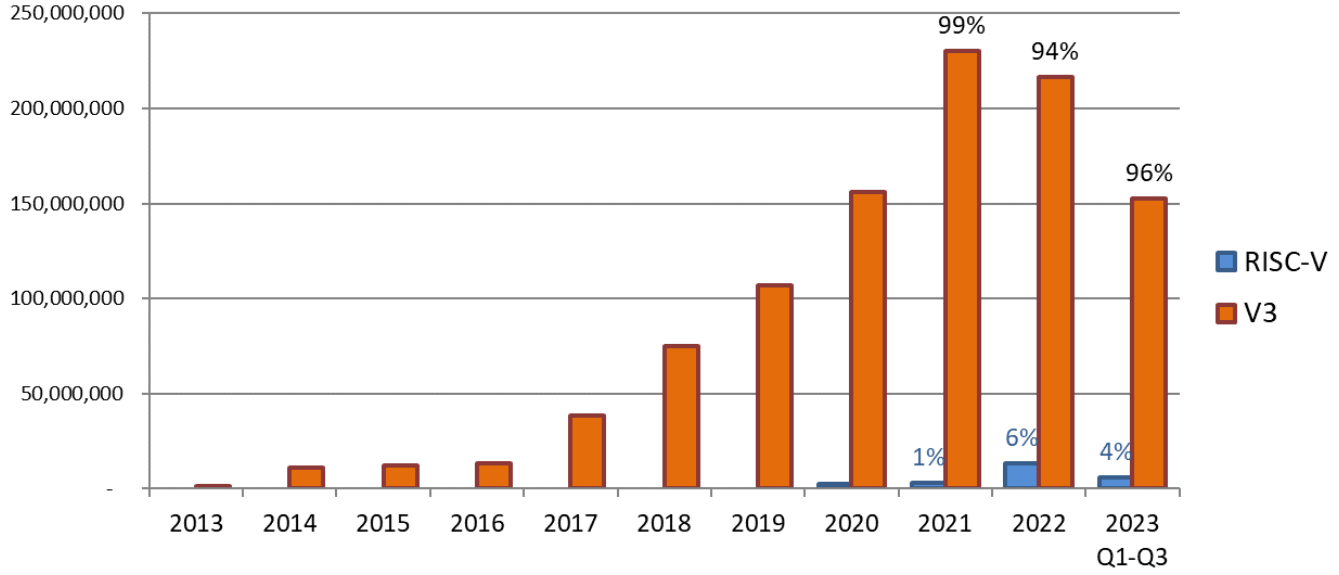
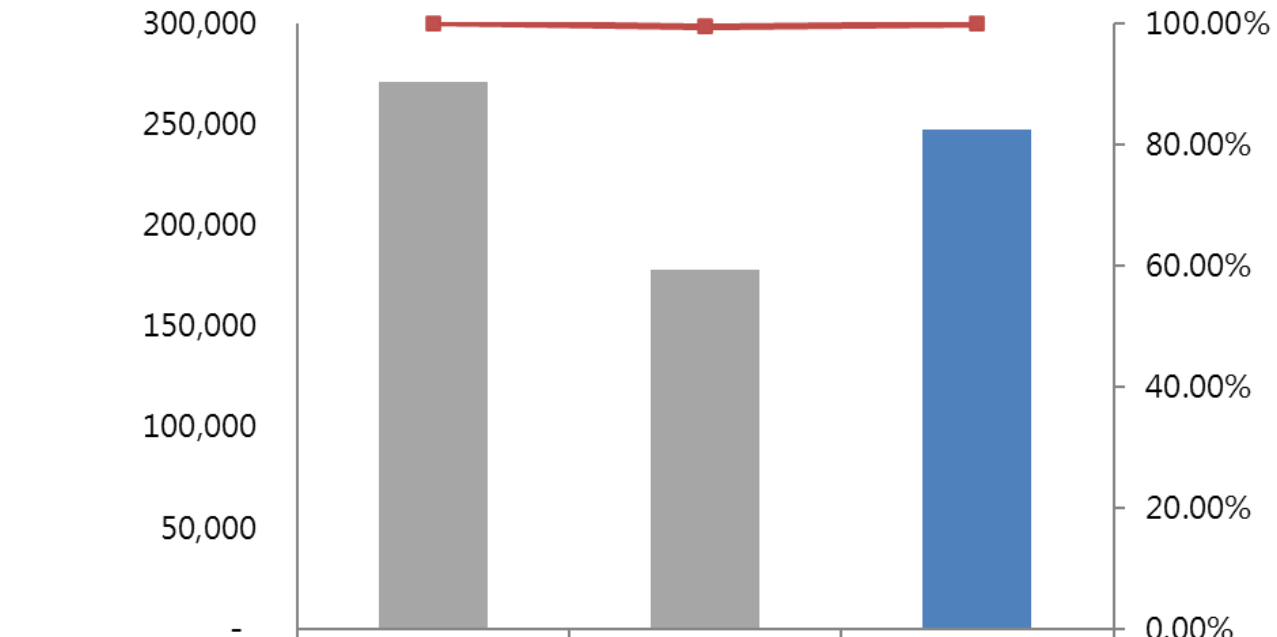


Royalty

3Q23 Consolidated Gross Margin

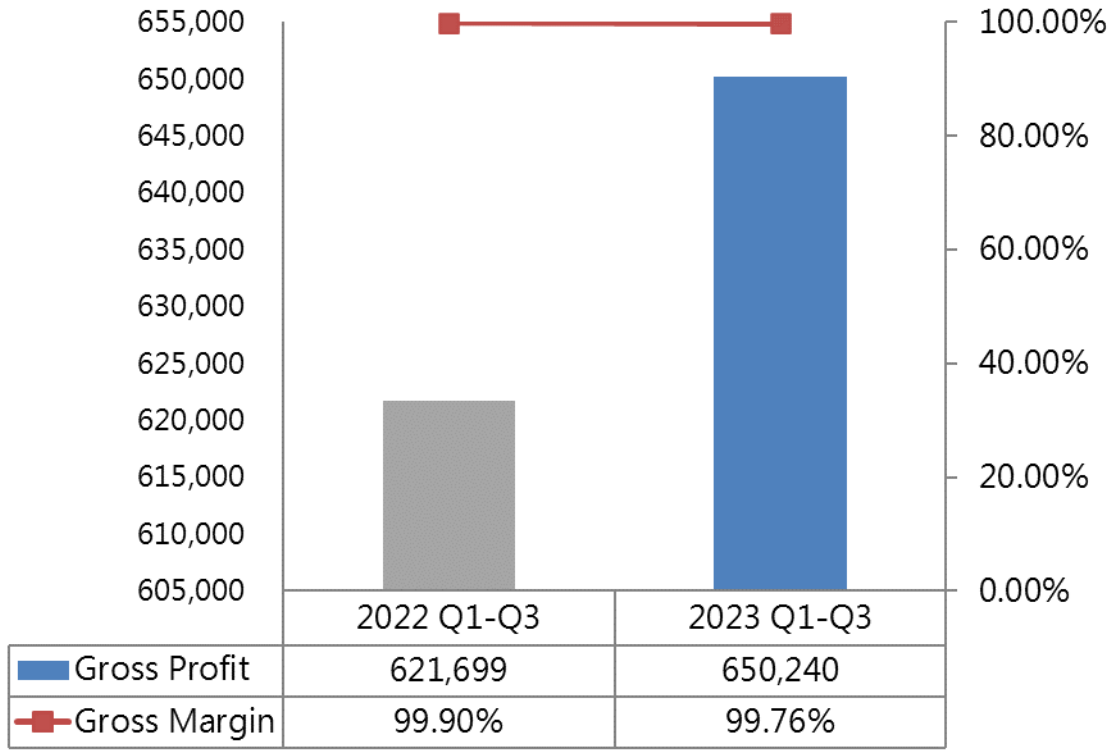
(NT$ thousands)



	3Q22	2Q23	3Q23
Gross Profit	270,957	178,118	247,183
Gross Margin	99.93%	99.42%	99.84%

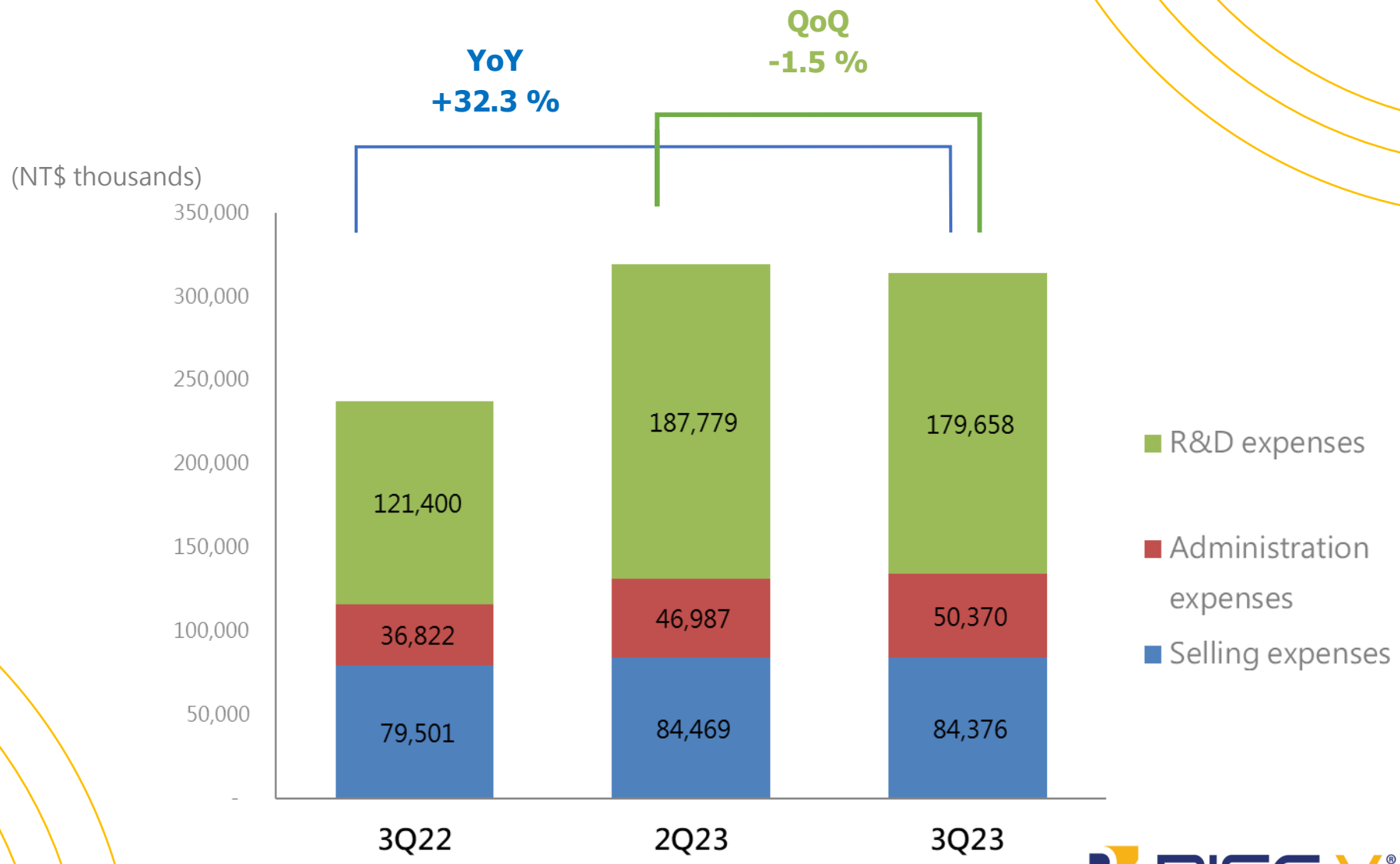
2023 Q1-Q3 Consolidated Gross Margin

(NT$ thousands)

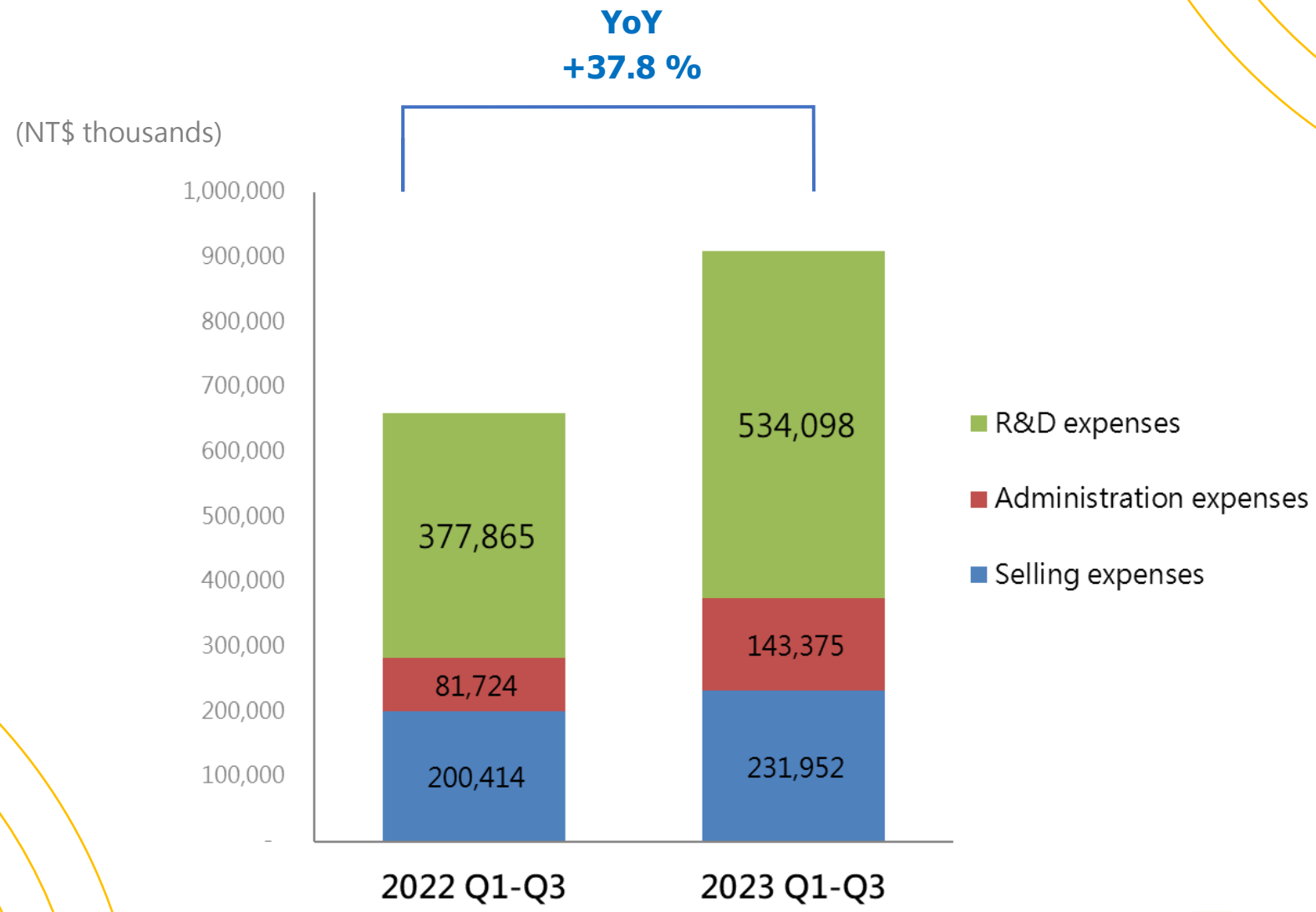


	2022 Q1-Q3	2023 Q1-Q3
Gross Profit	621,699	650,240
Gross Margin	99.90%	99.76%

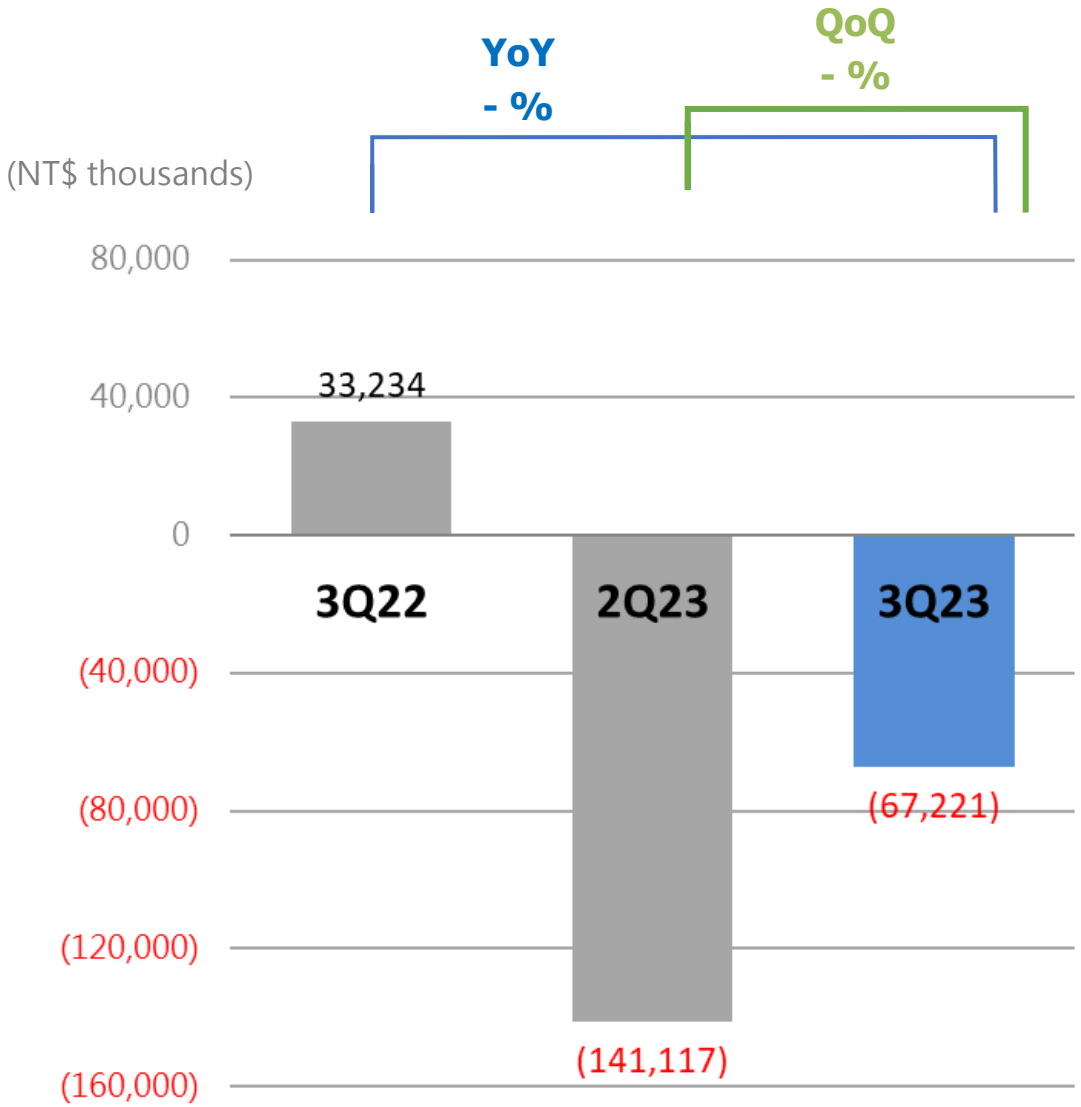
3Q23 Consolidated Operating Expenses



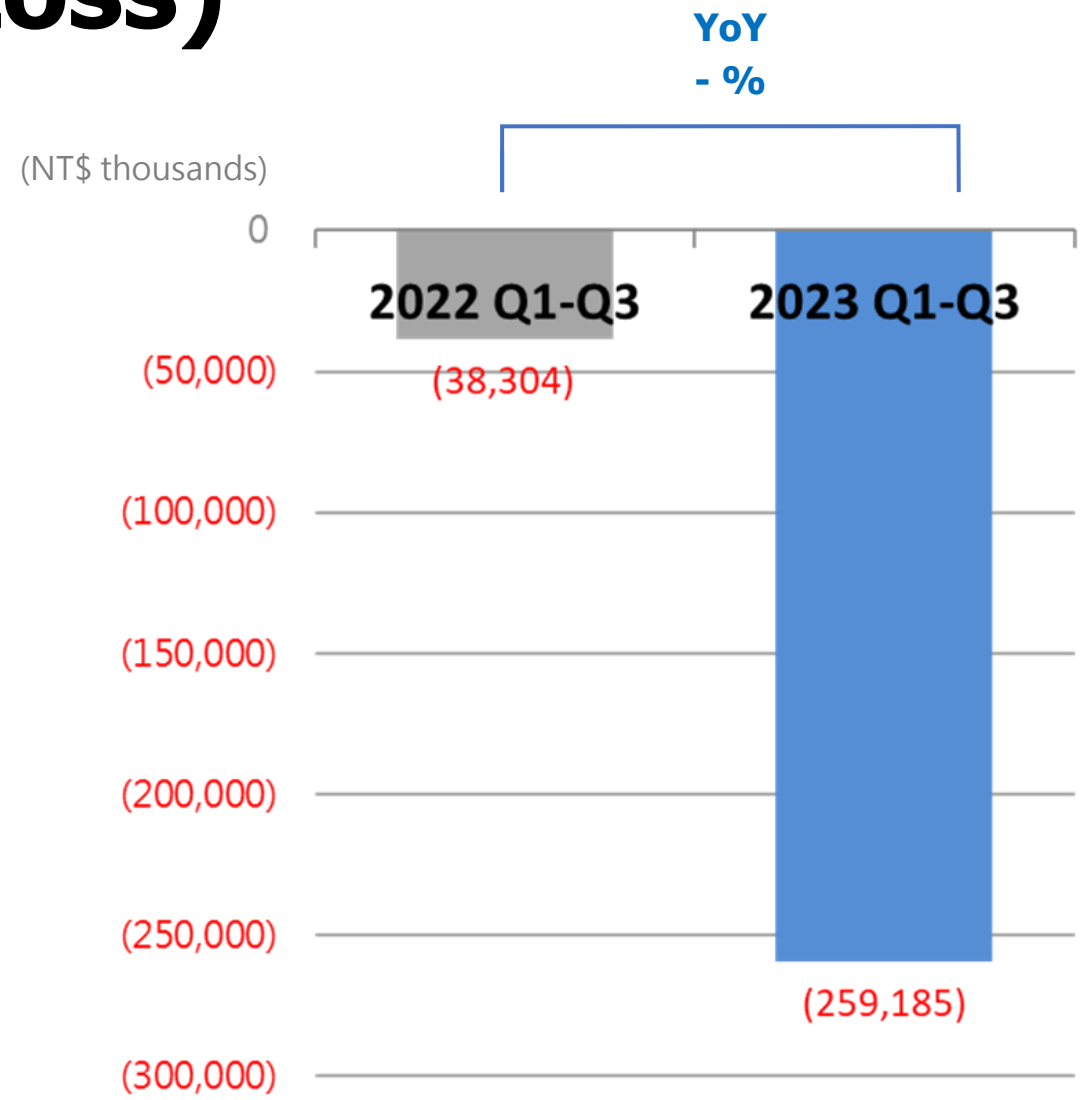
2023 Q1-Q3 Consolidated Operating Expenses



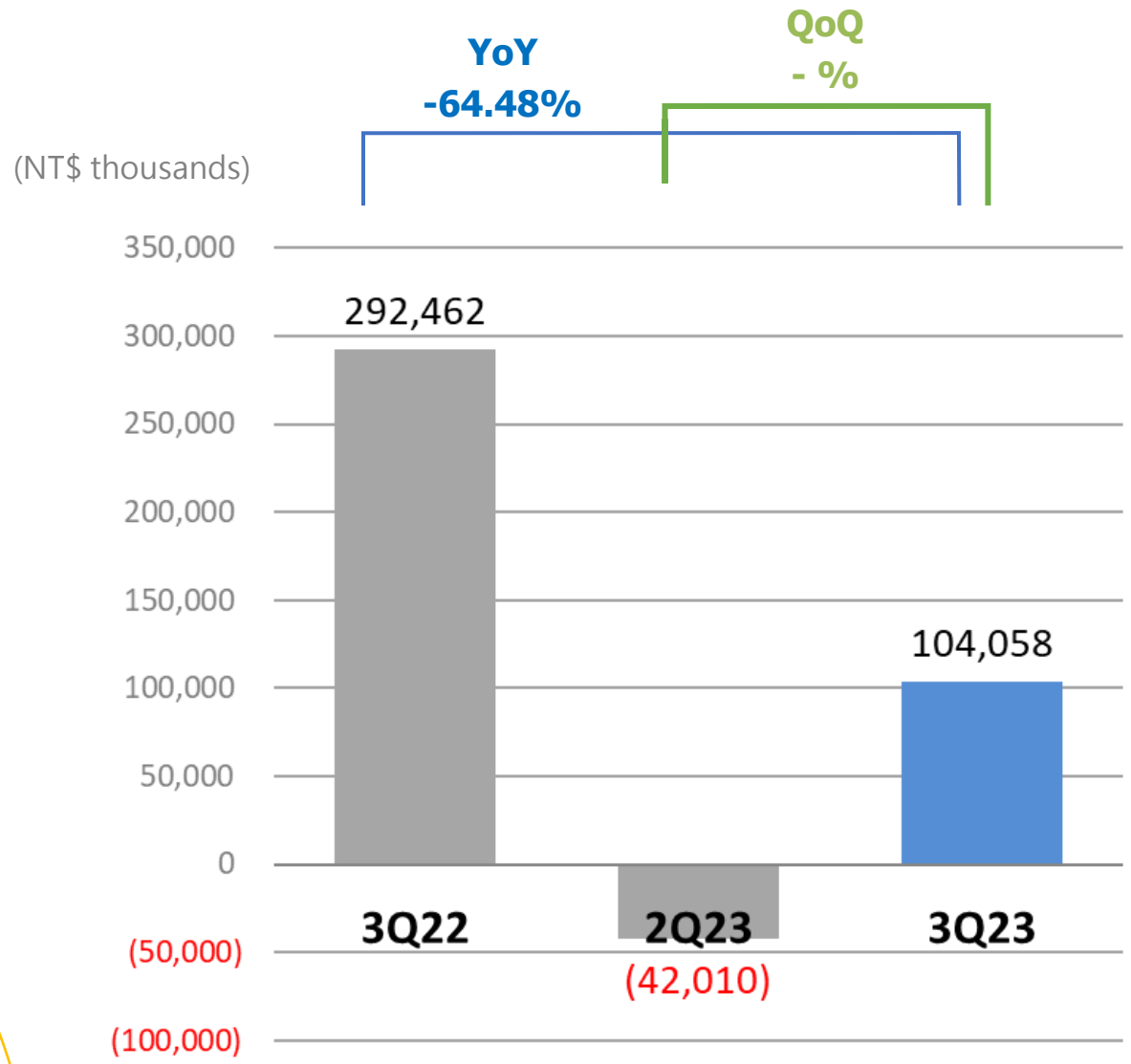
3Q23 Consolidated Operating Income



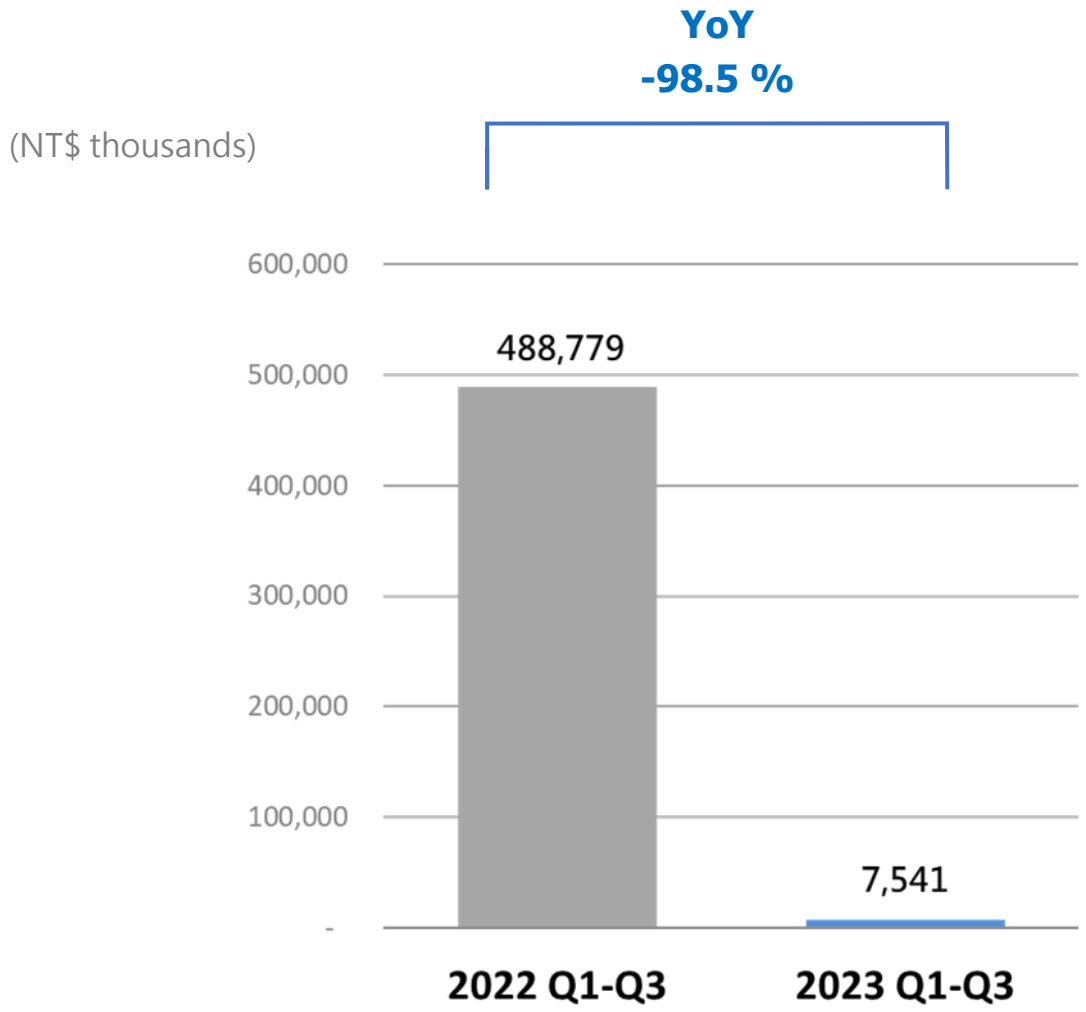
2023 Q1-Q3 Consolidated Operating Income (Loss)



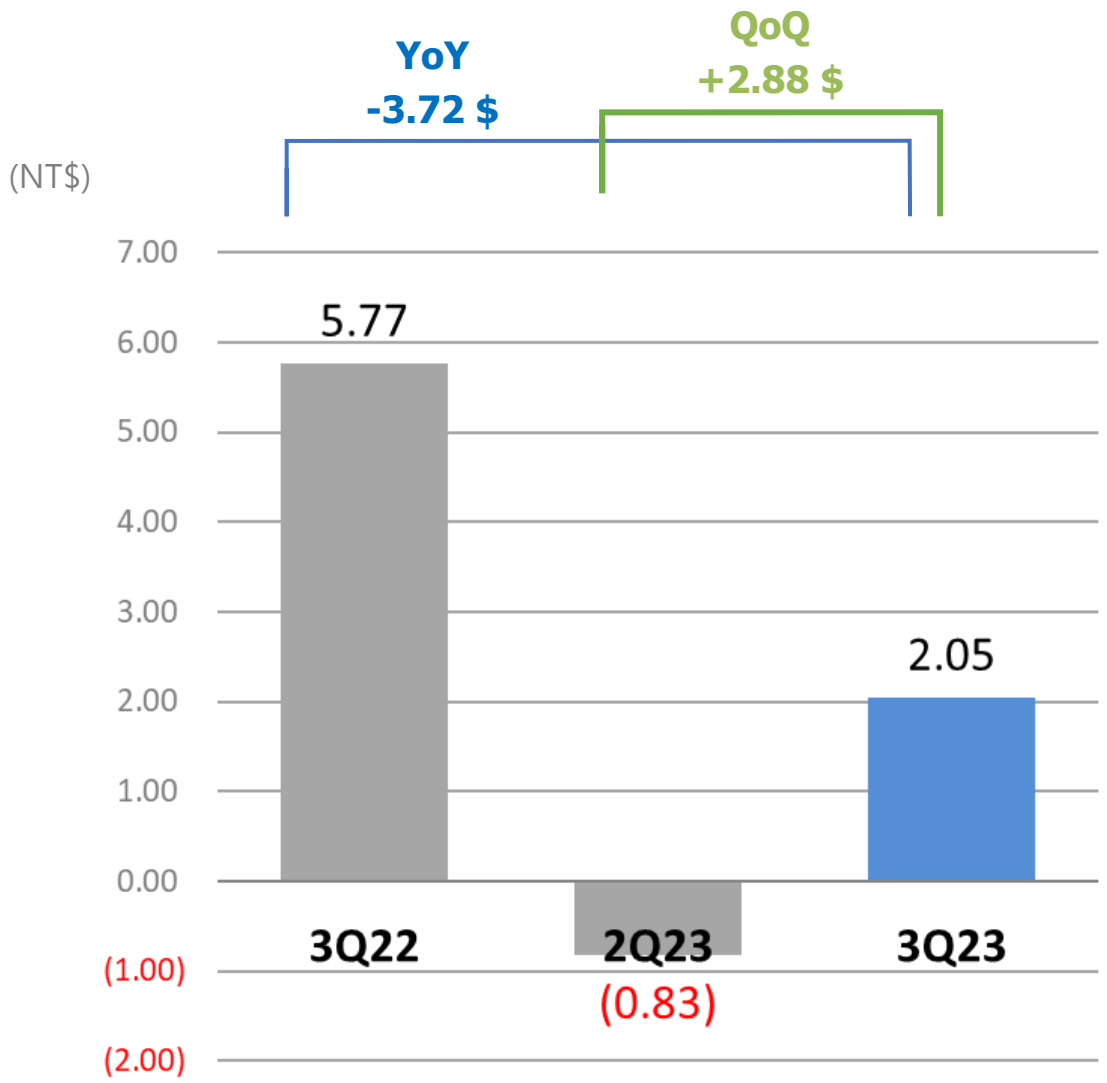
3Q23 Consolidated Net Income



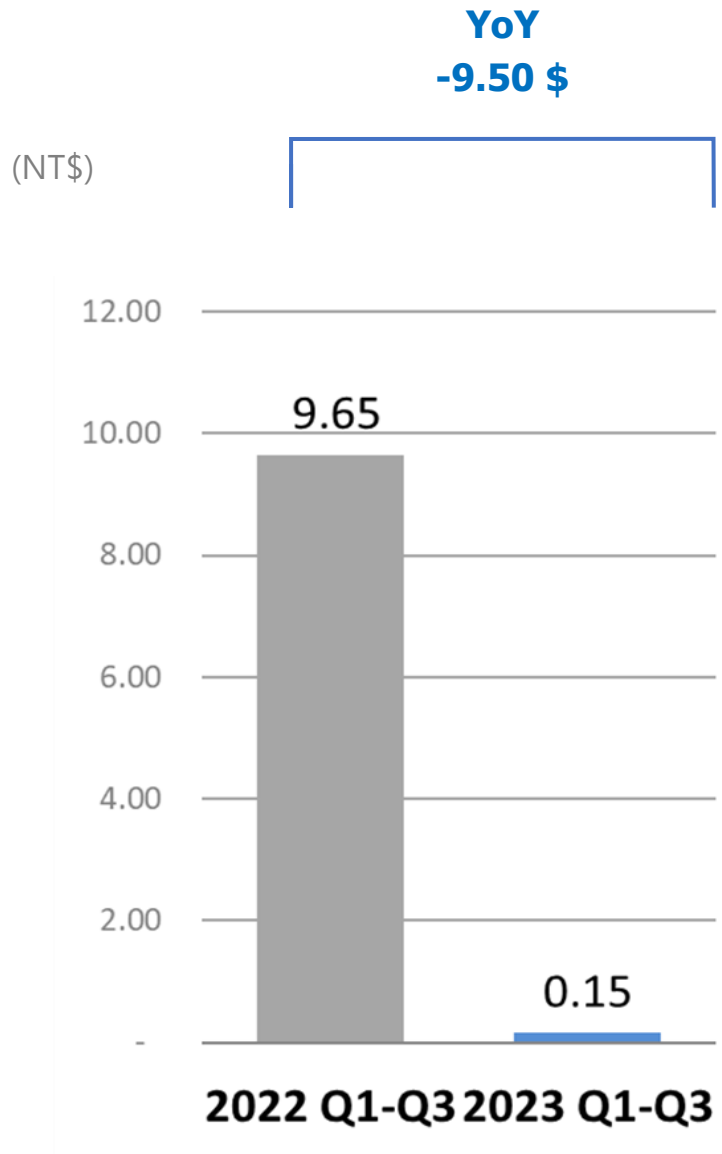
2023 Q1-Q3 Consolidated Net Income



3Q23 Consolidated EPS



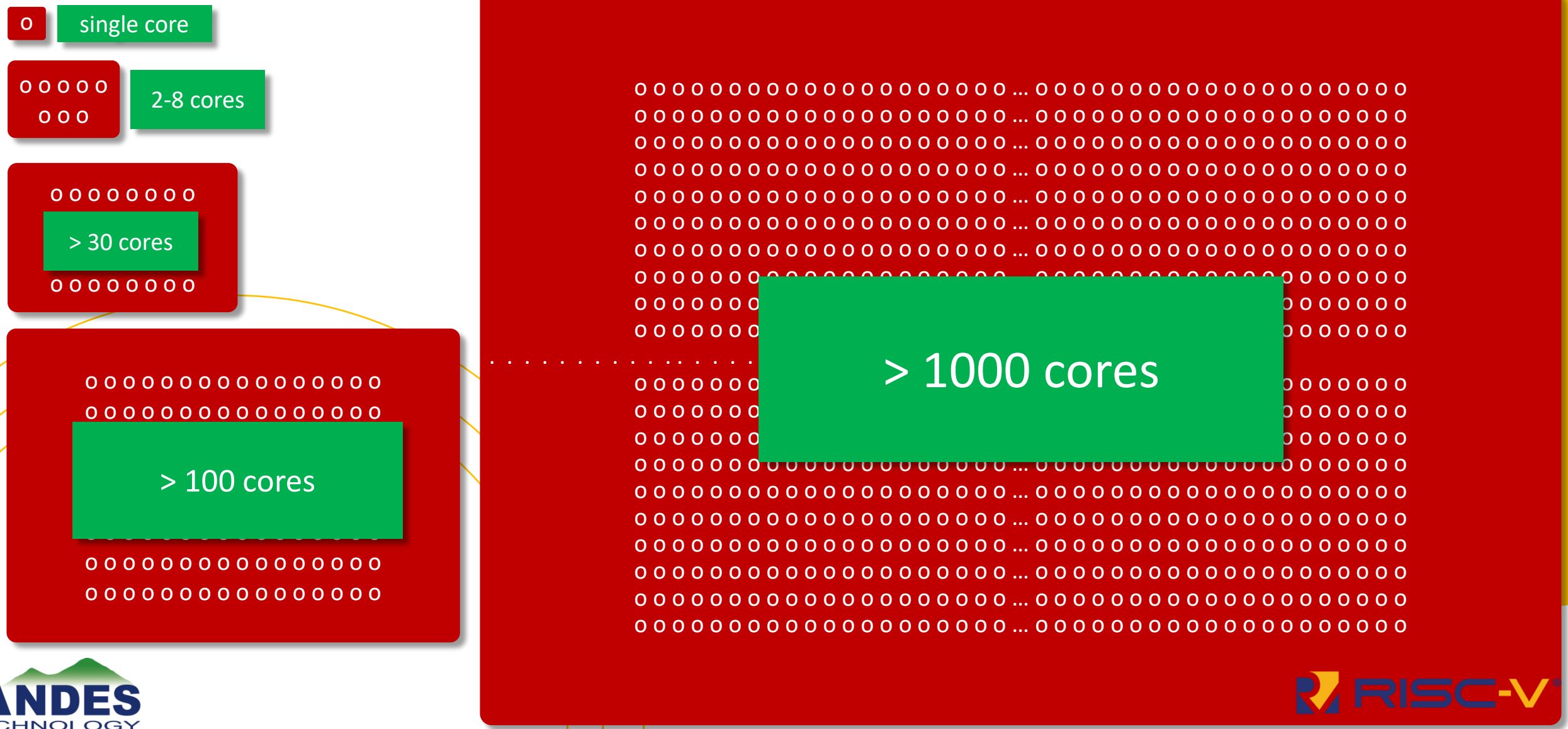
2023 Q1-Q3 Consolidated EPS



Product Applications

http://www.andestech.com

Andes RISC-V Cores Adopted in SoC



ANDES TECHNOLOGY

RISC-V

Andes RISC-V Powering Rich Applications

Mobile

Performance, code size

N25F, N45

MPU/MCU/AIoT

RENESAS, HPMicro, Kneron, Telink, Internet Company

D25F, D45, AX25MP, AX45MP

Endpoints. Edge. Cloud. Space.

Cloud AI

STREAM COMPUTING, 后摩智能 HOUMO.AI, SK telecom

Accelerate, accelerate, accelerate

NX27V, AX25, AX27, AX45MP, AX45MPV

Space

Secure, control, compute, communicate, position

N25F

Storage

Performance, bandwidth, real-time

N25F, N45, AX45MP

5G Networks

N25F, A25, A45MP, AX45MP

MTIA: Meta Training and Inference Accelerator

- ISCA 2023 paper, “MTIA: First Generation Silicon Targeting Meta’s Recommendation Systems”
- Proc-A/B: Andes AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models

Figure 3: High-level architecture of the accelerator

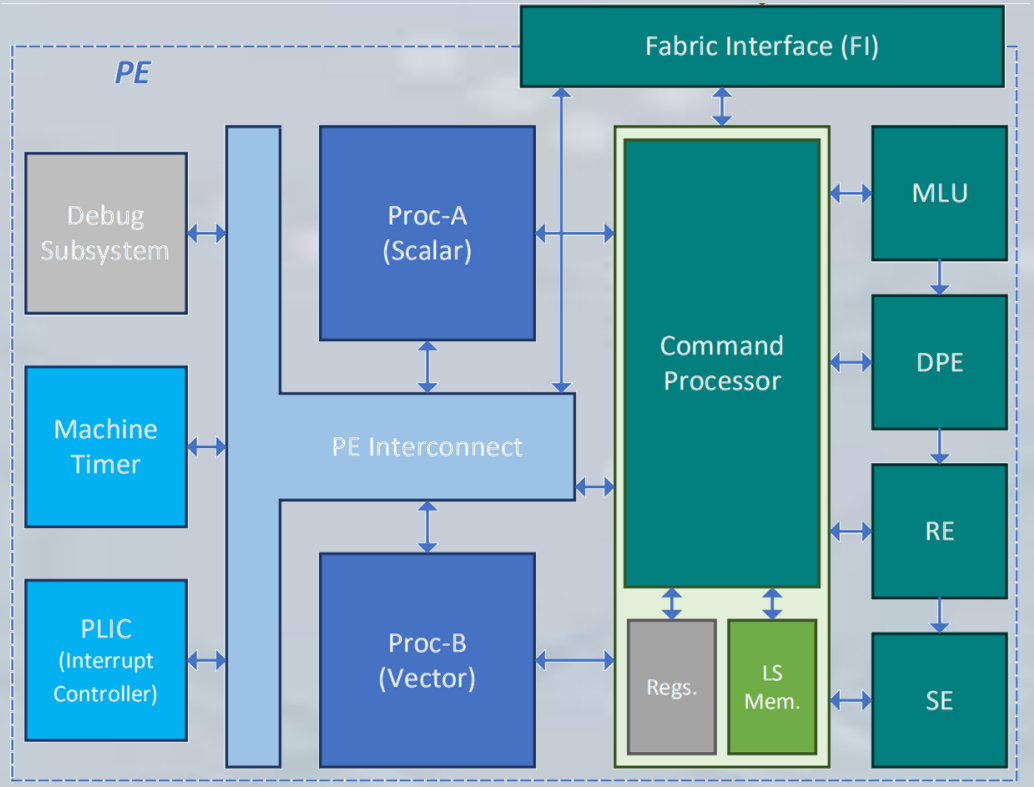


Figure 4: PE’s internal organization

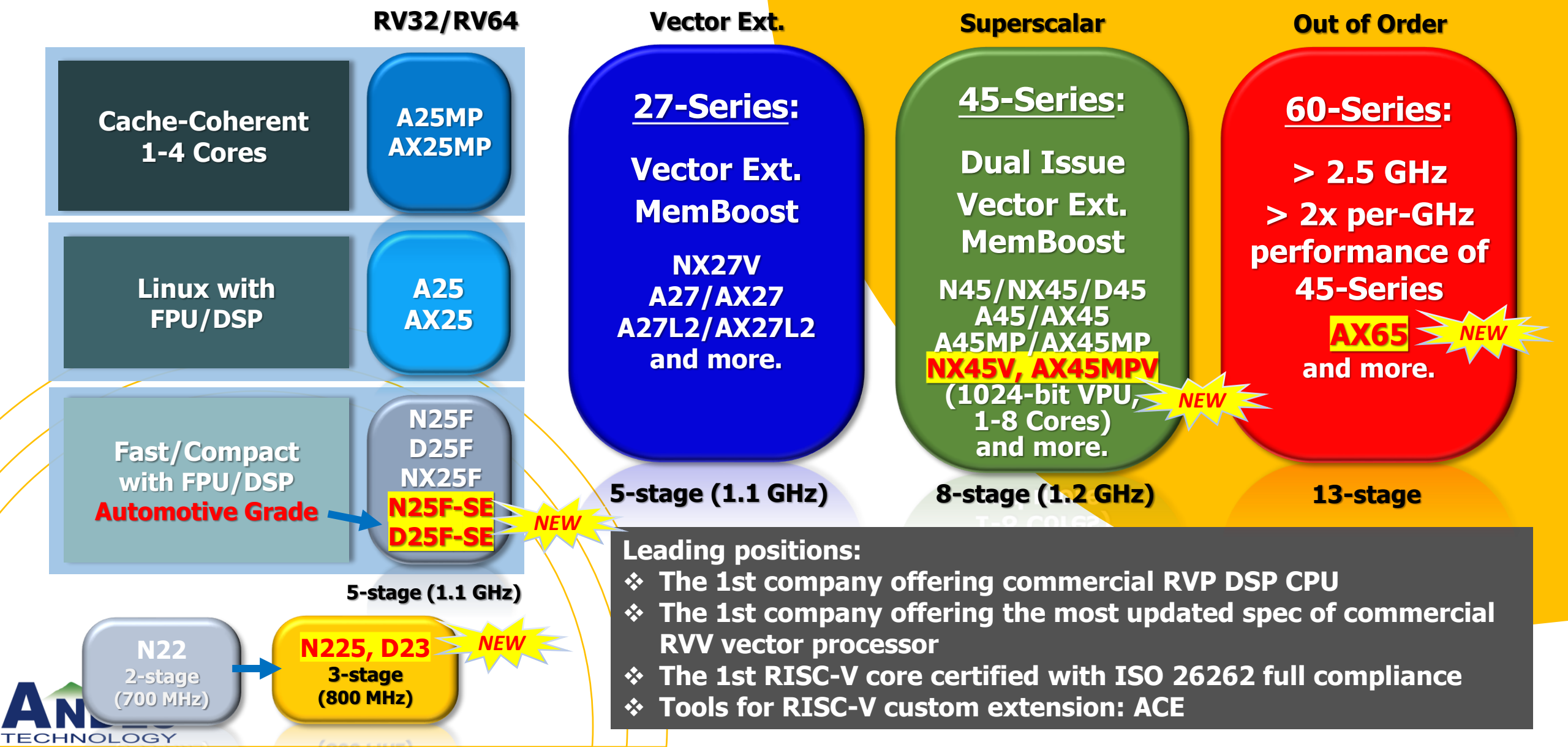
All photos: courtesy of ACM

Powered by Andes NX27V+ACE

New Products and Ecosystems

http://www.andestech.com

Andes RISC-V Product Roadmap



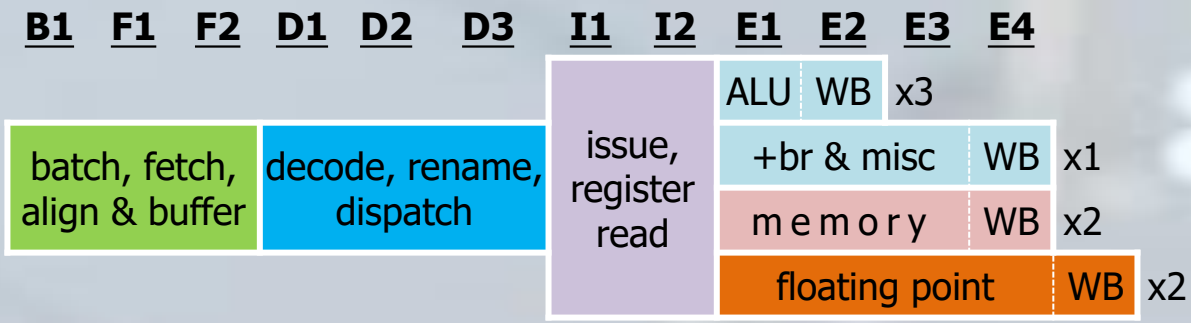
Leading positions:

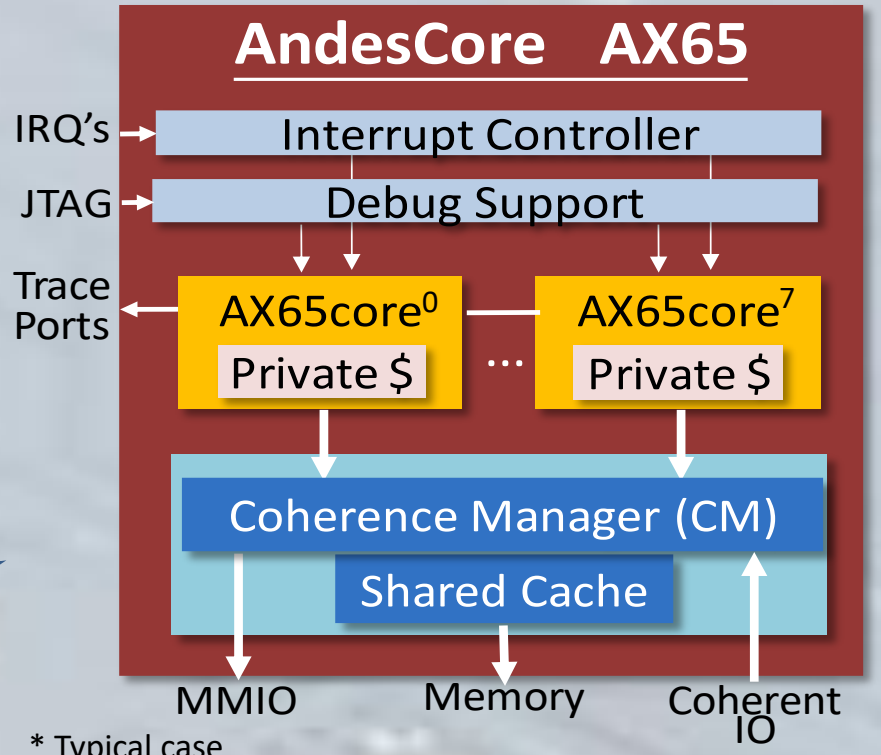
- The 1st company offering commercial RVP DSP CPU
- The 1st company offering the most updated spec of commercial RVV vector processor
- The 1st RISC-V core certified with ISO 26262 full compliance
- Tools for RISC-V custom extension: ACE

ANDES TECHNOLOGY

AndesCore™ AX65 OOO Application Processor

- 13-stage 4-way 64-bit OOO processor
- RVA22+ profile
- Multicore cluster up to 8 cores
- 8 Execution Pipes: 4 ALU, 2 LD/ST, 2 FP
- 2-Level BTB with TAGE-L Branch Predictor
- Caches:
  - Private I/D caches: 64 KB, 4-way, 4-bank
  - Shared cache: up to 8 MB, 16-way
- 256-bit AXI4 for Memory, MMIO and IOCP
- Performance:
  - 2.4 GHz* @7nm without overdrive
  - Specint2006: 8.25/GHz
  - Specfp2006: 10.2/GHz





Best spec2k6 with 2-level caches

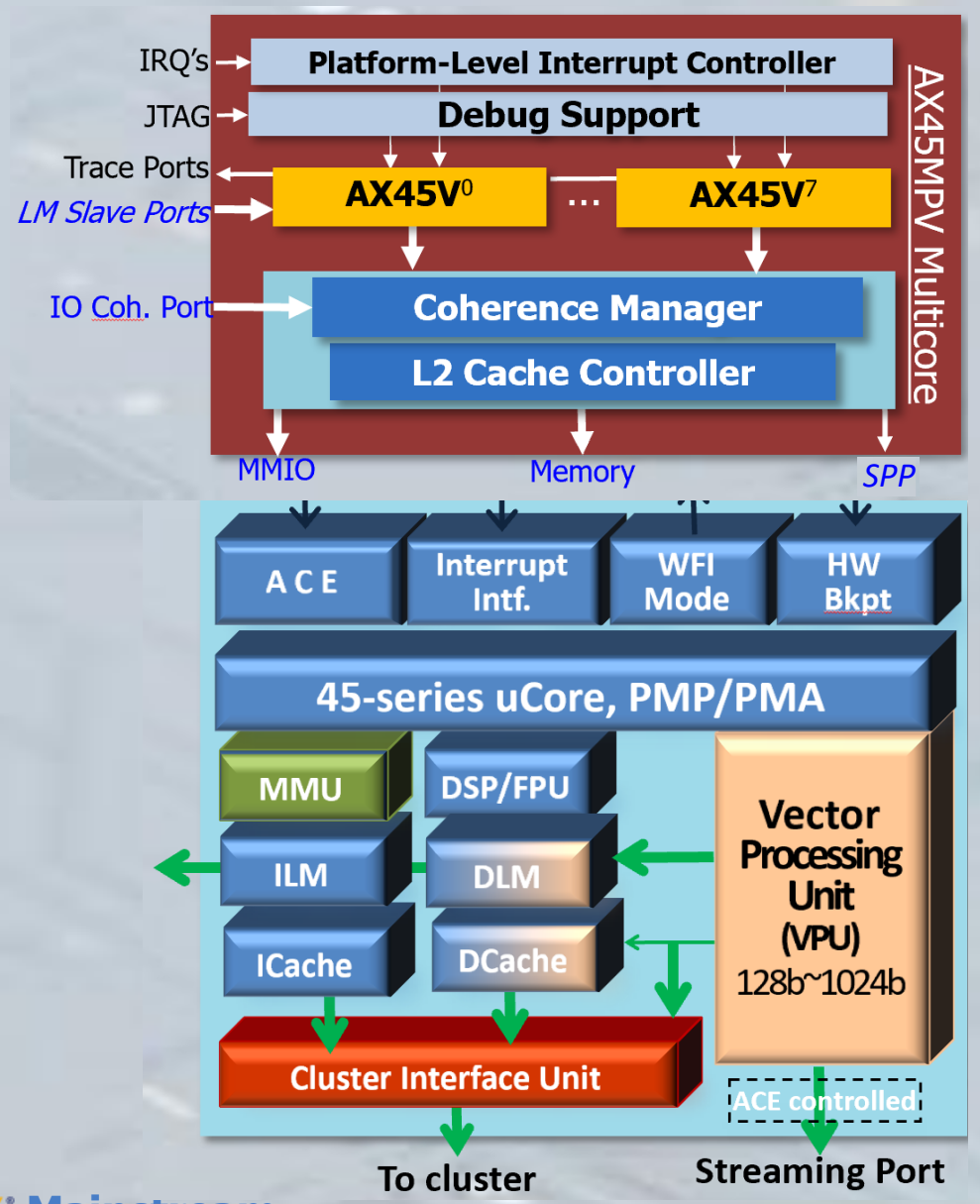
* Typical case

Roadmap for the AX60 Series

Efficient	*Mid-range*	*Extended*
AX60 Series: 13-stage OOO Linux MP		

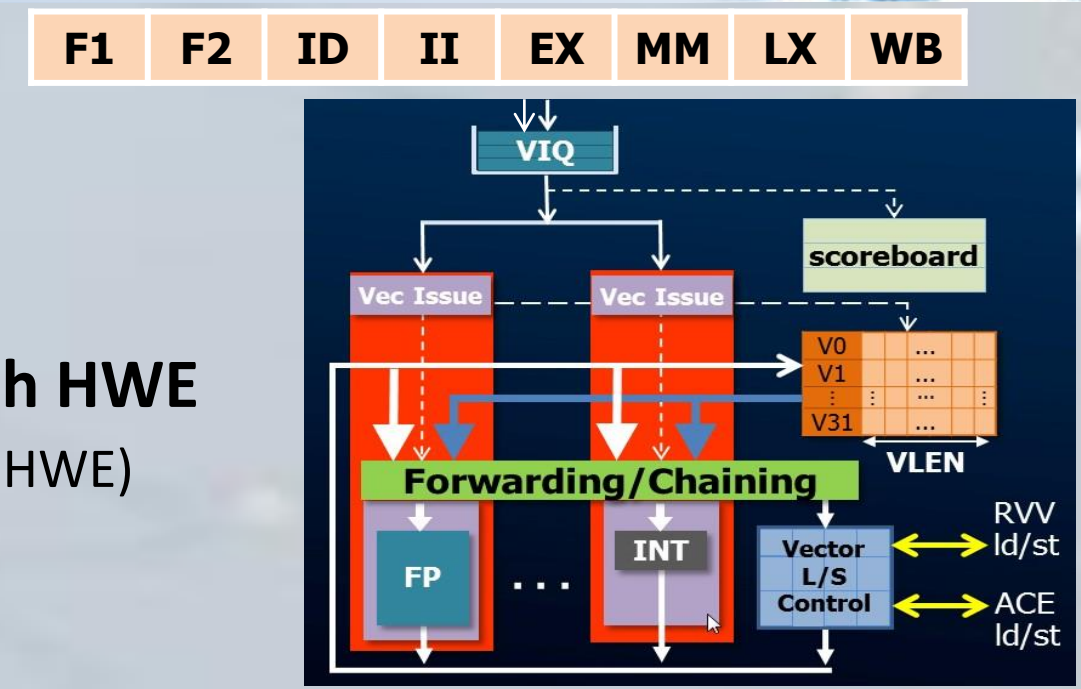
AX45MPV Multicore Cluster

- **At multicore cluster level:**
  - Up to 8 cores
  - CM/L2$ subsystem
    - 128KB to 8MB, 64B line, 16-way
    - Multi-cycle support for high-density SRAMs
    - I/D prefetch, up to 64 outstanding requests
  - AXI Bus Interfaces up to 512 bits
- **Scalar Unit: RV64GCBP**
  - 8-stage In-order dual-issue
  - MMU/SV48, M/S/U modes
  - I/D caches: 8K~64KB; Parity (I$) or ECC (both)
- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, **bf16**
  - VLEN/DLEN: 128~**1024** bits, 1:1 or 2:1 ratio
  - Up to 6 DLEN results per cycle

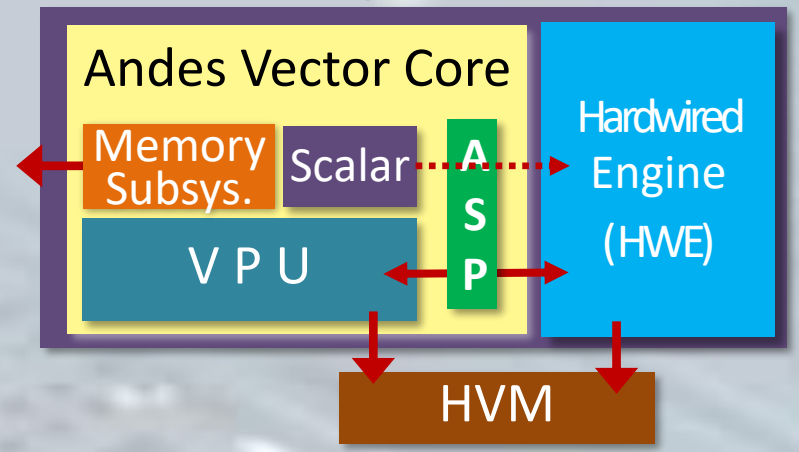


AX45MPV: 1024-bit Vector Processor

- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, **bf16**
  - VLEN/DLEN: 128~**1024** bits, 1:1 or 2:1 ratio
  - Up to 6 DLEN results per cycle
- **Efficient support needed for tight coupling with HWE**
  1. Data exchange performance (from/to shared memory in HWE)
  2. Efficient control to the HWE
- **2 solutions offered in AX45MPV:**
  - Andes Streaming Port™ (ASP) thru ACE
    - Data bus: data transfer btw VR and HWE
    - Command bus: to control/synchronize HWE operations
  - HVM: High-speed Vector Memory
    - CPU side: DLEN-wide load/store interface with dynamic wait cycles
    - HVM module: accepting multiple accesses to multi-bank SRAM's



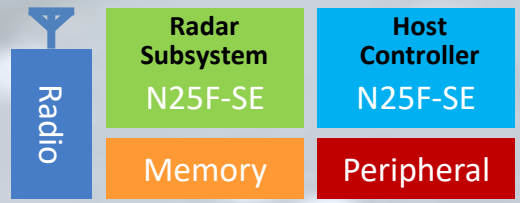
Processing Element (PE)



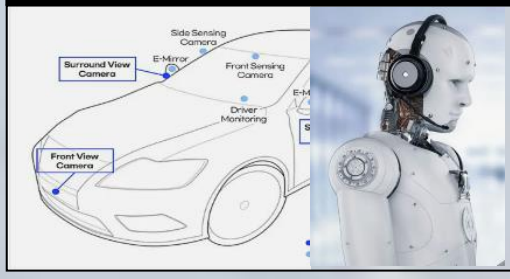
Andes is *Driving* Innovations in Automotive

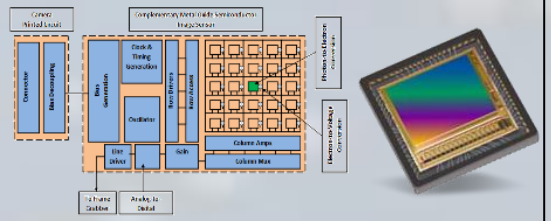
with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar

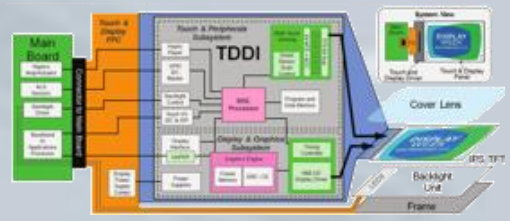


CMOS Sensor



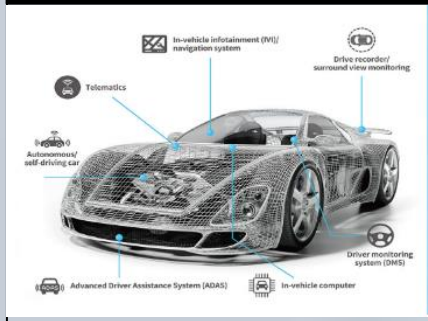


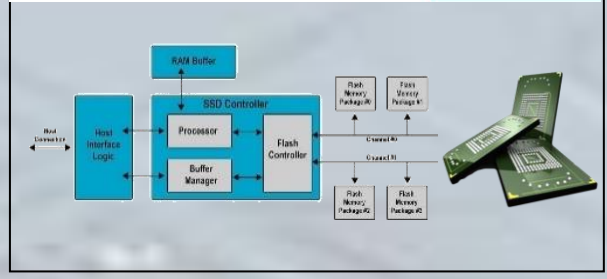
Auto TDDI



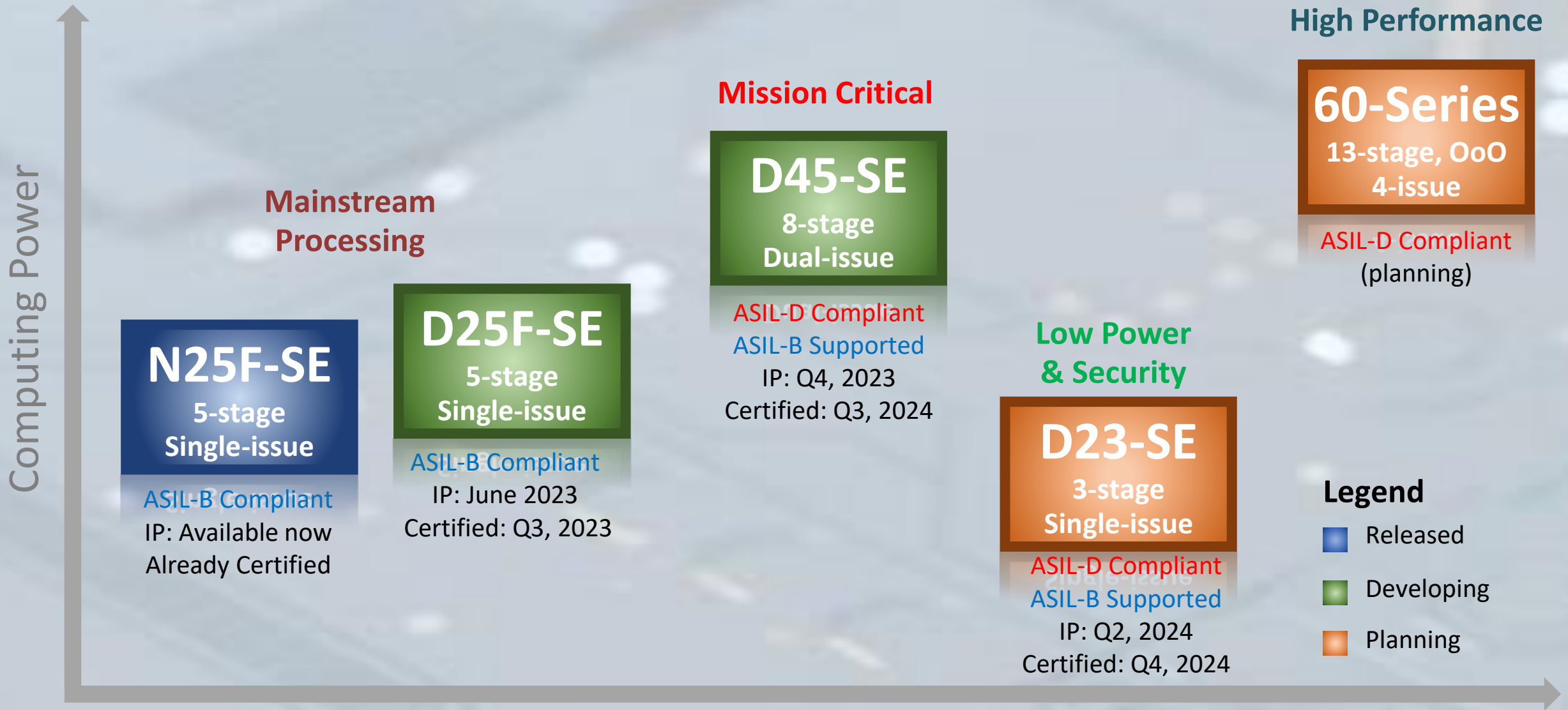
Auto MCU

Auto Storage



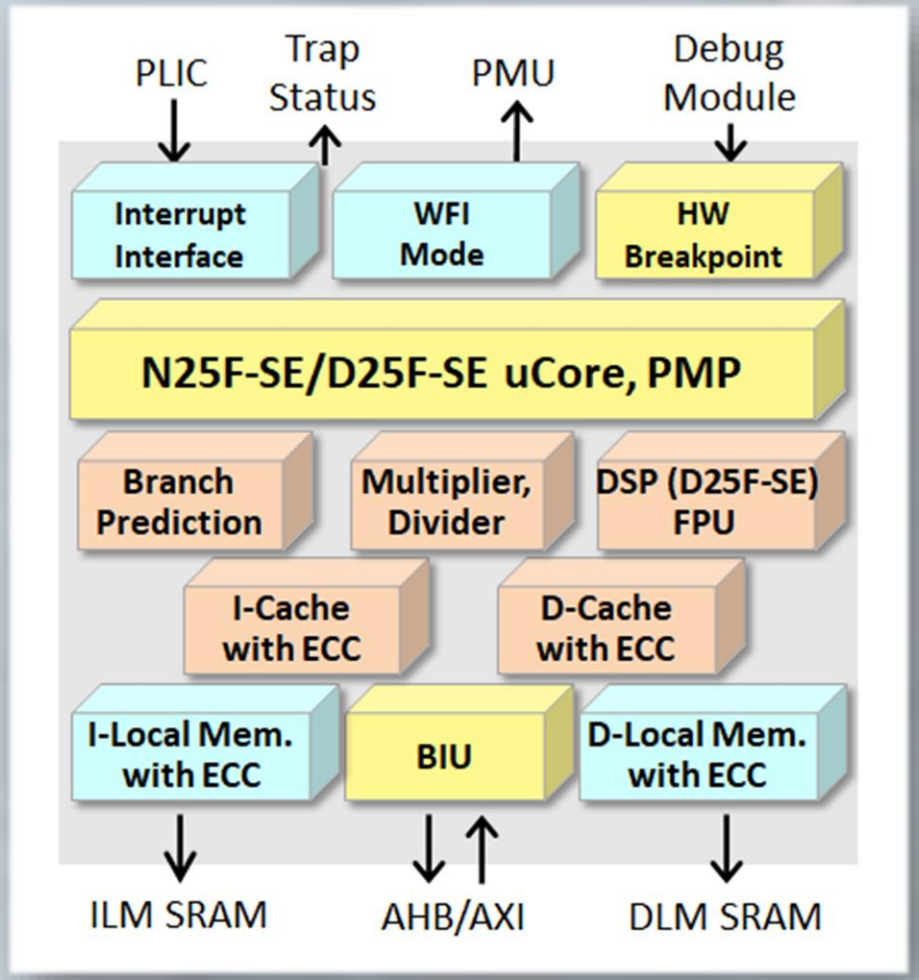


AndesCore™ RISC-V Functional Safety Roadmap



N25F-SE, D25F-SE 5-Stage, ASIL-B Full Compliant

- **CPU Core**
  - 5-stage, in-order, single-issue architecture
  - RISC-V RV32 GCB[P]* ISA, with Andes Extensions
    - D25F-SE with the RVP (SIMD/DSP) instruction extension
    - RVB bit-manipulation instructions for cryptography, … applications
  - AndeStar™ V5 32-bit architecture
- **Memory Subsystem**
  - Instruction and data caches, up to 32KB each
  - Instruction and data local memories, up to 16MB each
- **Bus Interfaces and System Integration**
  - AXI or AHB bus master port
  - Local memory direct access port
- **Functional Safety**
  - Core trap status bus interface,
  - ECC protection, StackSafe™, PMP …
  - N25F-SE, ASIL-B certified. D25F-SE, ASIL-B certified at Q3/2023



AndesCore™ N25F-SE Certified by ISO 26262

SGS

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID	LICENSED TEST MARK	Report No.
S280	SGS TÜV SAAR ASIL B COMPLIANT Functional Safety ISO 26262	S2800001

Tested according to ISO 26262:2018 (Parts 2, 4 partly, 5, 8, 9)

Certified Product(s) **CPU IP "N25F-SE"**
Version: R320

Technical Data/Parameter The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance **with ASIL B** requirements.

Specific Requirements The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval.
The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

Munich, October 28th, 2022

Marcus Rau

The validation status is documented via SGS Certification Database.

The test mark regulation is an integral part of this certificate.

SGS-TÜV Saar GmbH, Hofmannstr. 50, D-81379 München, Deutschland / Germany.
Website: www.sgs-tuv-saar.com/fs
E-Mail: fs@sgs.com

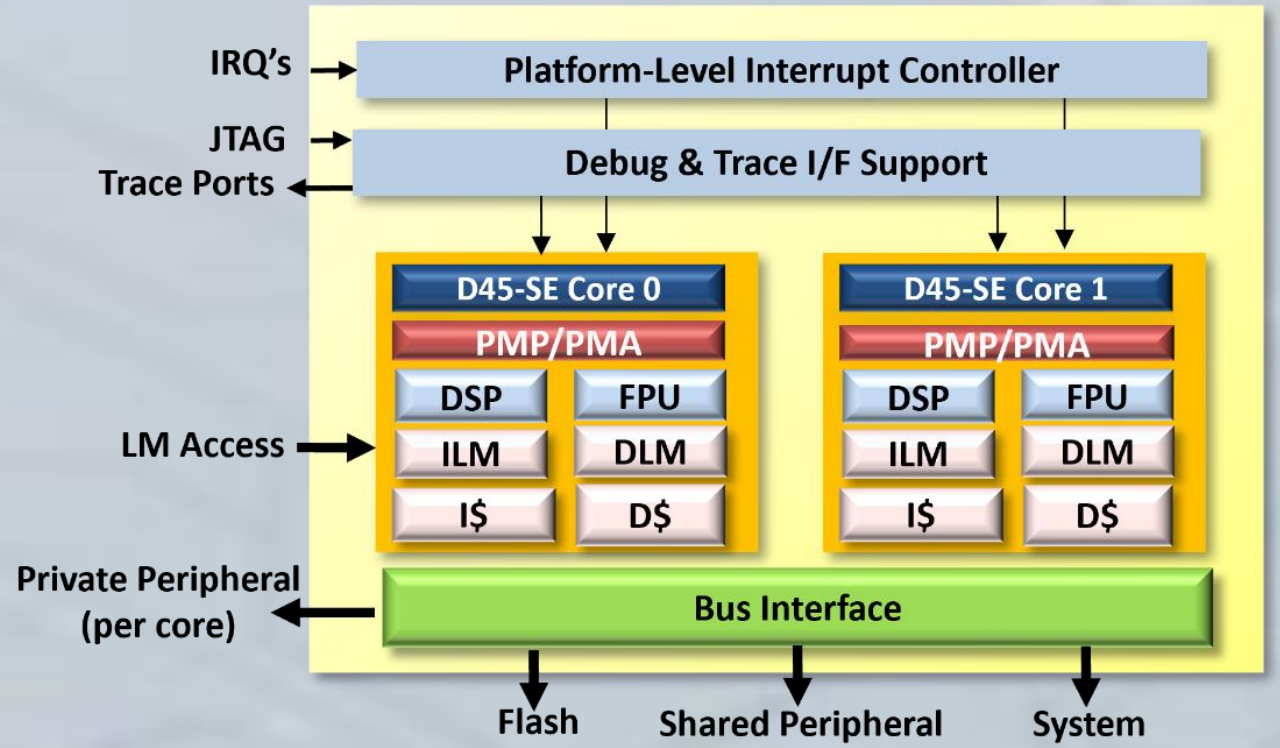
CERTIFICATE

- **"The product has been approved in compliance with ASIL B requirements"**
- **ISO 26262 Edition 2018, parts:**
  - ISO 26262-2:2018
  - ISO 26262-4:2018*
  - ISO 26262-5:2018
  - ISO 26262-8:2018
  - ISO 26262-9:2018
- **Certification Body**
  - SGS-TÜV Saar GmbH
  - SGS-TÜV Saar GmbH accredited by German accreditation body DAkkS

* Part-4 System/item level integration, validation is not applicable to CPU IP

D45-SE 8-Stage, Dual-Issue, up to ASIL-D

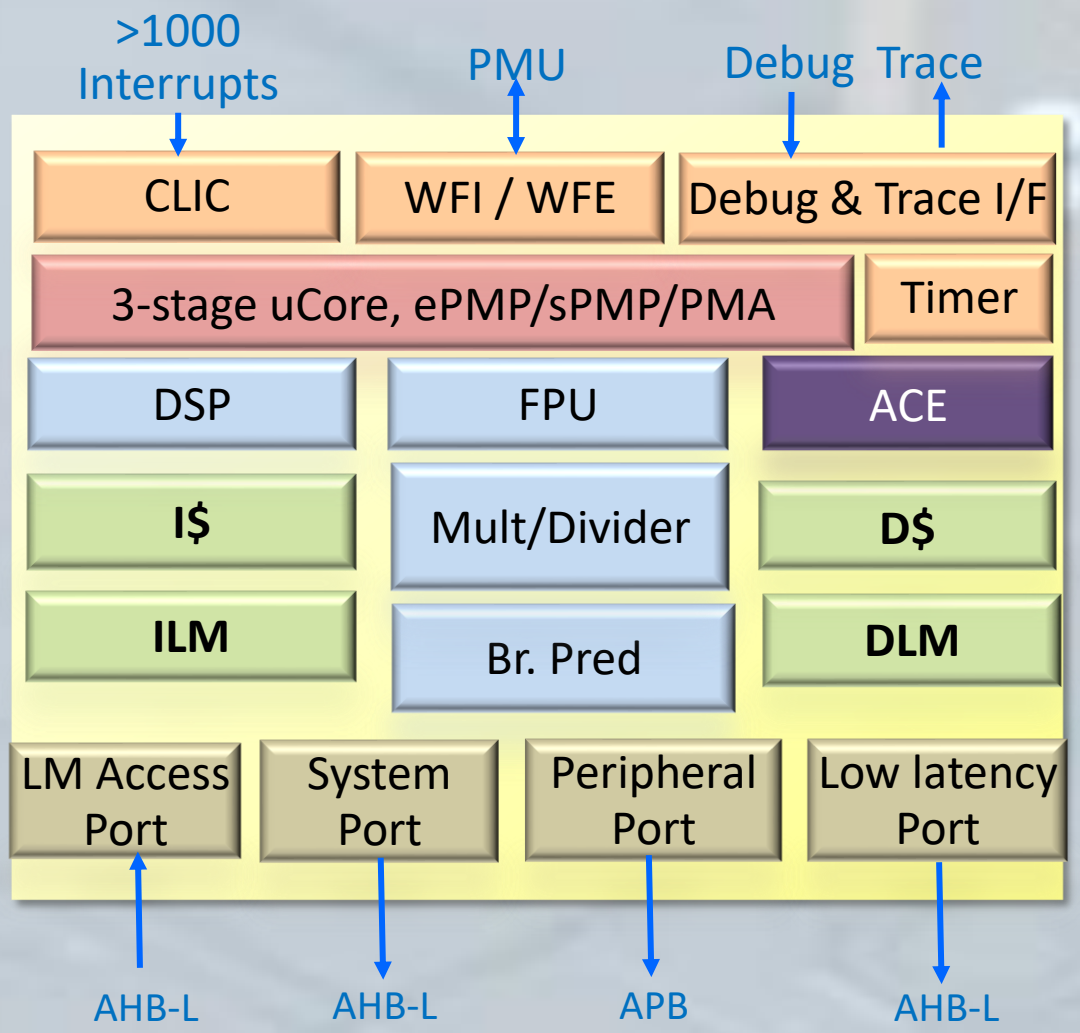
- **CPU Core**
  - 8-stage, in-order, superscalar, dual-issue most instruction pairs
  - RISC-V RV32 GCBP* support, Andes Extensions
  - AndeStar™ V5 32-bit architecture
- **Memory Subsystem**
  - Instruction and data cache, up to 64KB
  - Instruction and data local memory, up to 16MB
  - MemBoost
- **AXI Bus Interfaces**
  - System port, and flash port (64/128-bit)
  - LM access port (64/128-bit)
  - Private, and shared peripheral interface (64-bit)
- **Functional Safety**
  - Lockstep and Split mechanism
  - Configurable ECC for every memory
  - Core trap status bus interface
  - Bus protection, StackSafe™
  - Certified estimated by or before Q3/2024



*P: draft

D23: Compact Controller for IoT/MCU/ECU

- **3-stage, limited dual-issue (optional)**
- **ISA extensions:**
  - Base: RV32 I/E-MAC + B + Zce
  - Advanced: FD + P + K + CMO
- **Privilege modes: M, S, U**
- **Configurable features**
  - Branch prediction: none, static, dynamic
  - Multiplier options:
    Sequential: 1/2/4/8-bit per cycle
    Fast: pipelined
  - Andes Custom Extension™ (ACE)
  - Power management: WFI/WFE, PowerBrake
  - Core-Local Interrupt Controller (CLIC)
    >1000 sources, 255 priority levels
    Selective vectoring with priority preemption



D23: Compact Controller for IoT/MCU/ECU

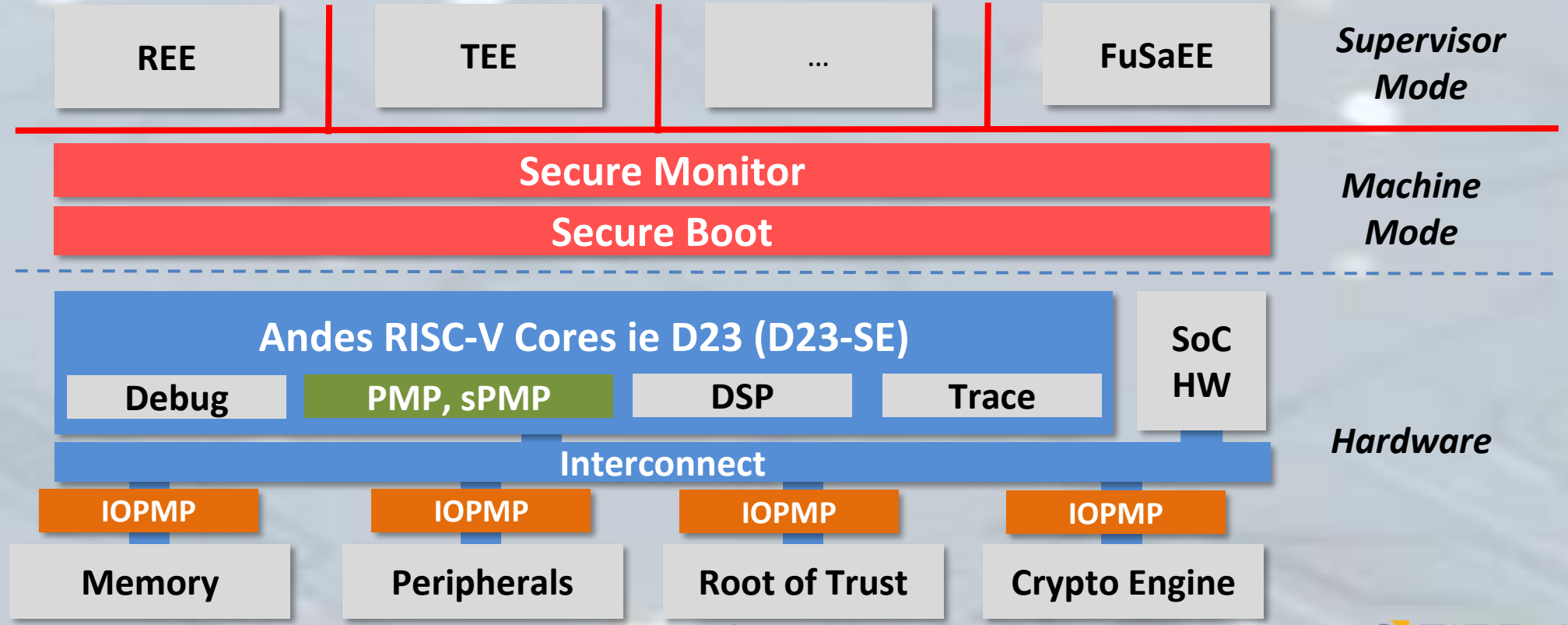
- **Memory subsystem:**
  - Caches:
    - Config:
      - Icache only: ifetch
      - RO-cache (Read-Only): ifetch and load
      - I/D caches: ifetch, load and store
    - Cache sizes: 1KB~32KB
    - Error protection: ECC for I$ and D$
  - I/D Local Memory (LM):
    - 0~512MB with ECC
    - Interface: SRAM or AHB-L

RISC-V Code Size Benchmarks							
ISA	IMAC	IMAC + V5 (N22)		IMABC + V5 (N25F)		**IMABZce + V5 (D23)**	
SPEC CPU	2,840	2,360	-16.9%	2,346	-17.4%	**2,247**	**20.9%**
CSiBE	1,462	1,204	-17.6%	1,190	-18.6%	**1,144**	**21.8%**
Audio Codec	842	682	-19.0%	671	-20.3%	**656**	**22.1%**
Embench-IoT	63.6	51.2	-19.5%	48.9	-23.1%	**48.4**	**23.9%**

- D23-SE Safety-Enhanced D23 for Automotive designs, ASIL-D compliant & ASIL-B supported

Security System Architecture for D23 (D23-SE)

- Create multiple zones protection by PMP/sPMP
  - REEs (Rich Execution Environment)
  - TEEs (Trusted Execution Environment)
- IOPMP for IO protection



The Rise of

AndesAIRE™ AnDLA™ I350

The First Generation of Andes Deep Learning Accelerator

AndesAIRE™ NN SDK

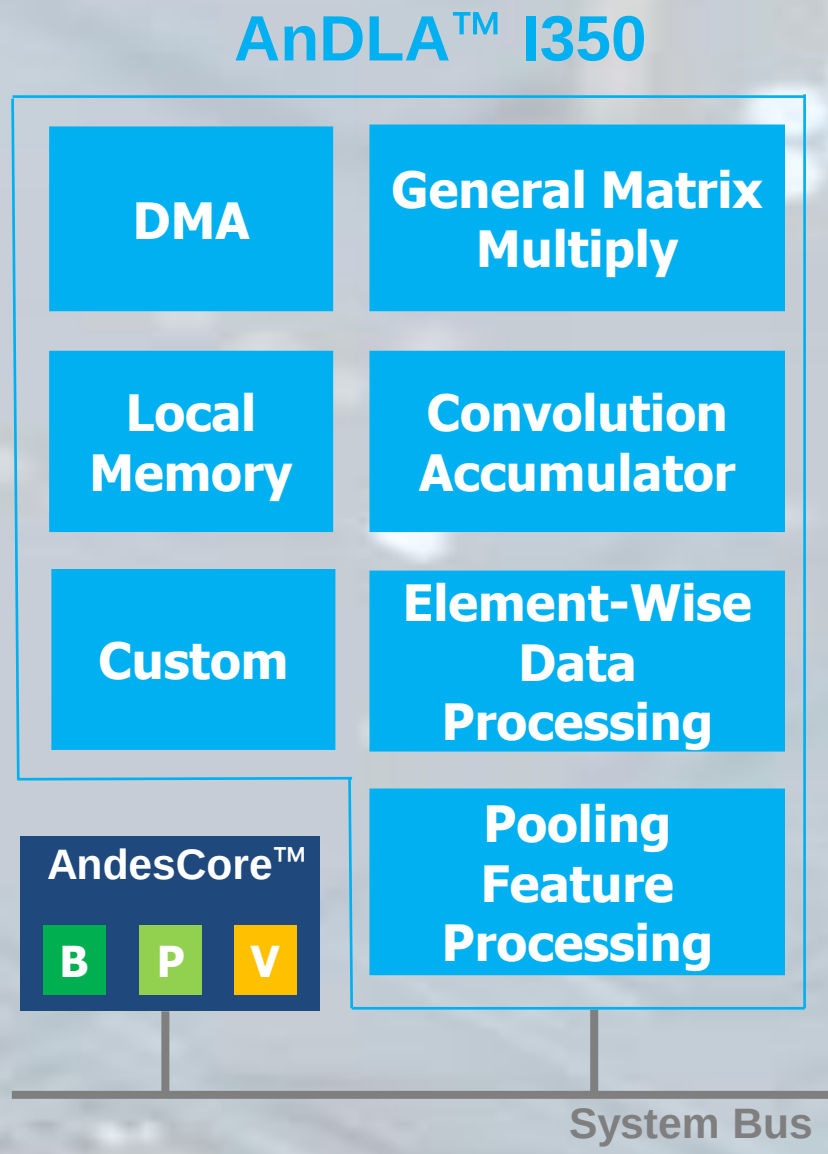
Unleash the maximum AI/ML performance
and synergy of RISC-V CPU and AnDLA™

AndesAIRE™

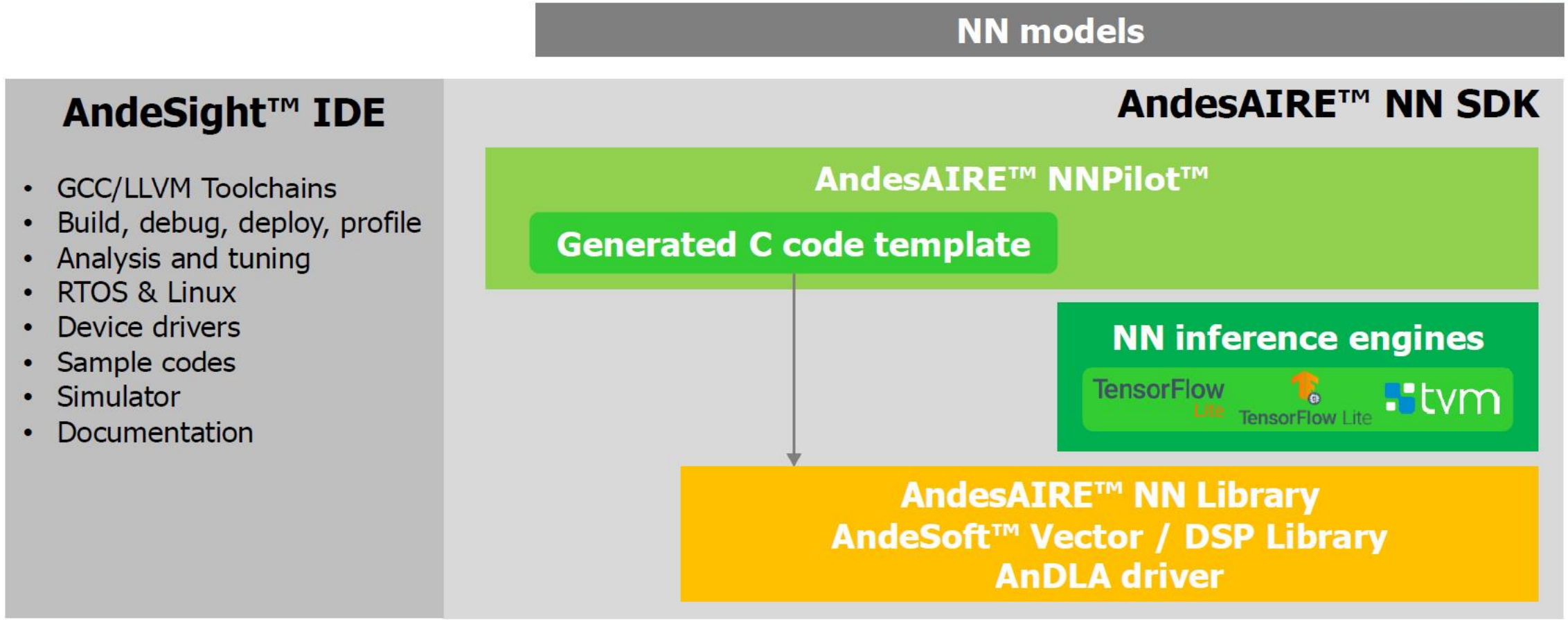
Andes AI Runs Everywhere

AndesAIRE™ AnDLA™ I350

- Andes Deep Learning Accelerator (AnDLA™)
  - High performance-efficient deep learning accelerator for edge and end-point inference
  - Scalable and multi-DLA
  - Cooperate with AndesCore™ full series (22/23/25/27/45/65)
- Accelerating for most of NN Applications
  - Image and video
  - Speech/voice and audio
- Target performance
  - Configurable MACs: 32 to 4096 (INT8)
  - Performance: 64 GOPS to 8 TOPS (INT8 @1GHz)
  - Configurable local memory: 16KB to 4MB
  - Leading power efficiency >5 TOPS/W (@28nm)
- Integrated DMA and local memory



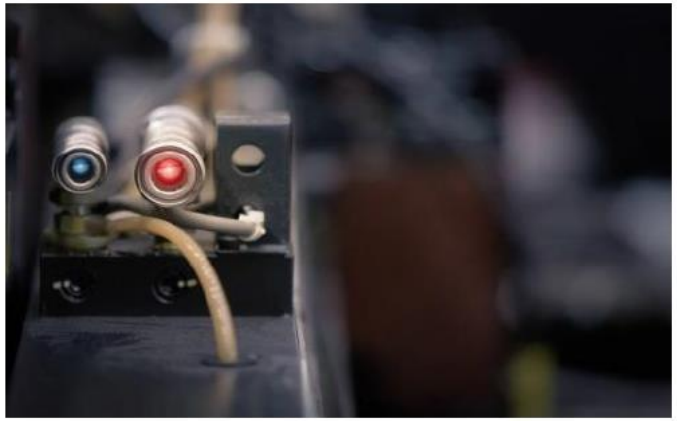
Andes AI Total Solutions



AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera

Smart Sensor



Smart Home Appliance

AIoT / tinyML

Robotics

Wearable

Taking RISC-V® Mainstream

Thank You

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