



晶心科技股份有限公司

投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱



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公司簡介



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營運成果



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產品應用



04

新產品及生態系統



05

總結



公司簡介

<http://www.andestech.com>



晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數超過450人；80%為工程師。
- 獲得TSMC 2015年新的 IP OIP Award 。
- 晉升為RISC-V國際聯盟(前身為RISC-V基金會) 首席會員。(2020)
- 獲得AI Global Media頒發「2020年最傑出嵌入式處理器IP供應商」。
- EE Awards亞洲金選獎 - 「Taiwan 產品獎」, 「Asia 企業獎」(2021)
- 2023亞太區 前五百大高成長企業



晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

晶心利基

- 智能及環保之電子設備
- 雲端應用,人工智慧及物聯網

重要里程碑

❖ 300+ commercial licensees

- Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
- 600+ license agreements signed

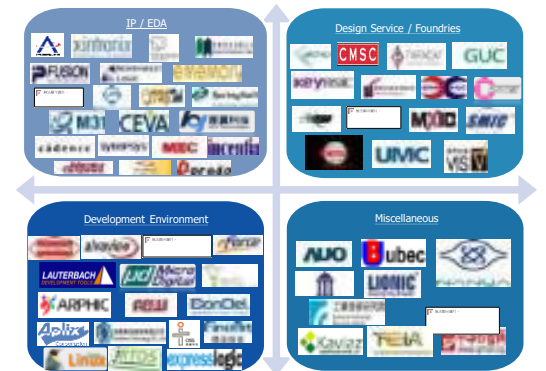
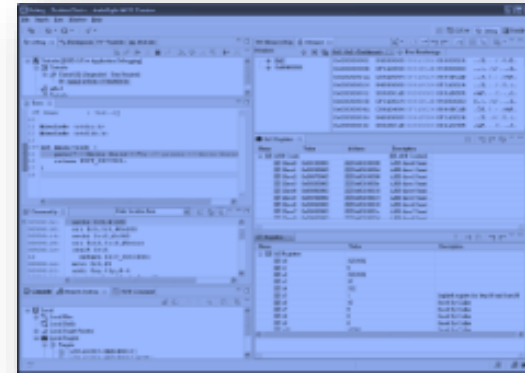
❖ AndeSight™ IDE:

- 25,000+ installations

❖ Eco-system:

- 500+ partners

❖ >13B Accumulative SoC Shipped





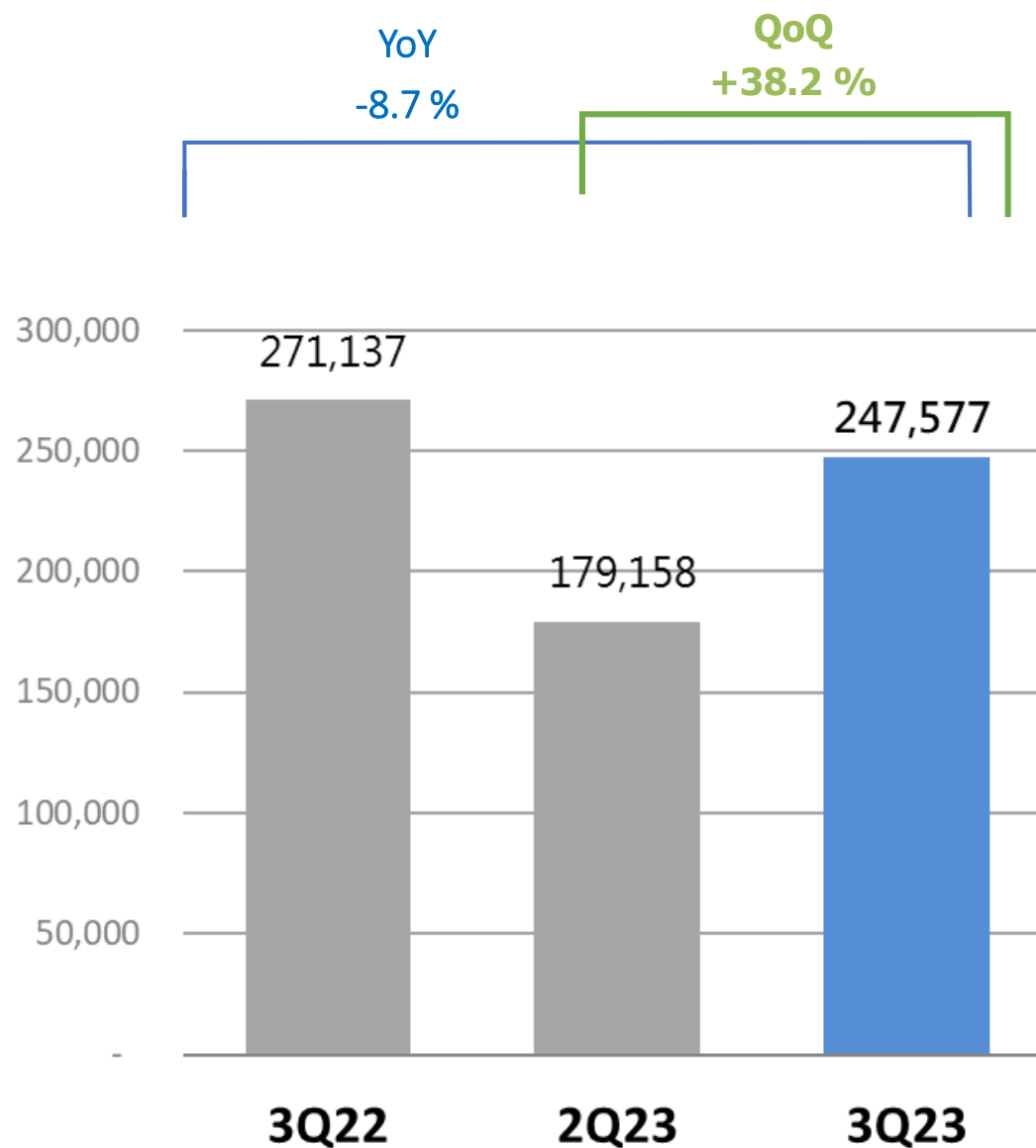
營運成果

<http://www.andestech.com>

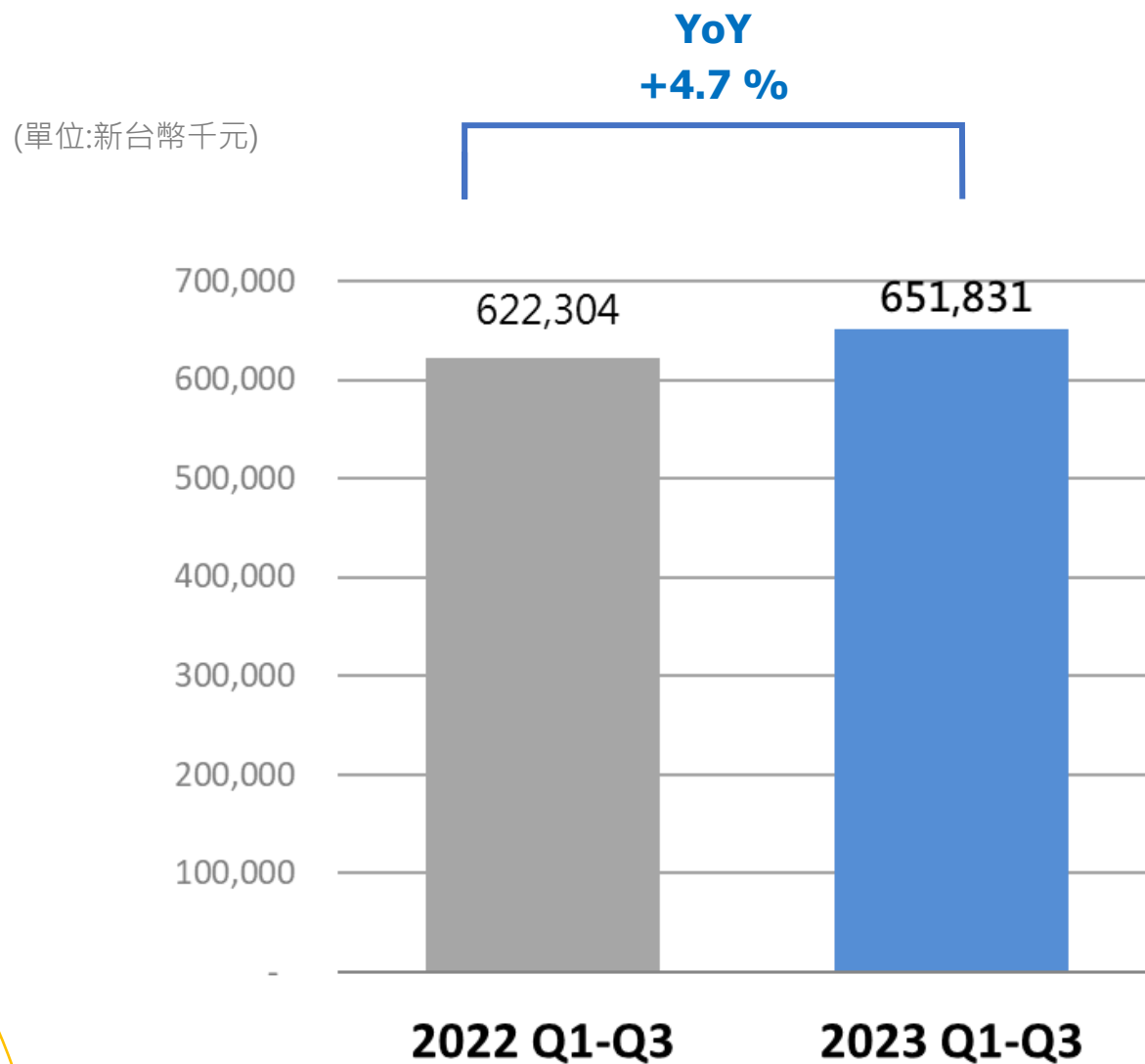


2023年第三季營業收入

(單位:新台幣千元)



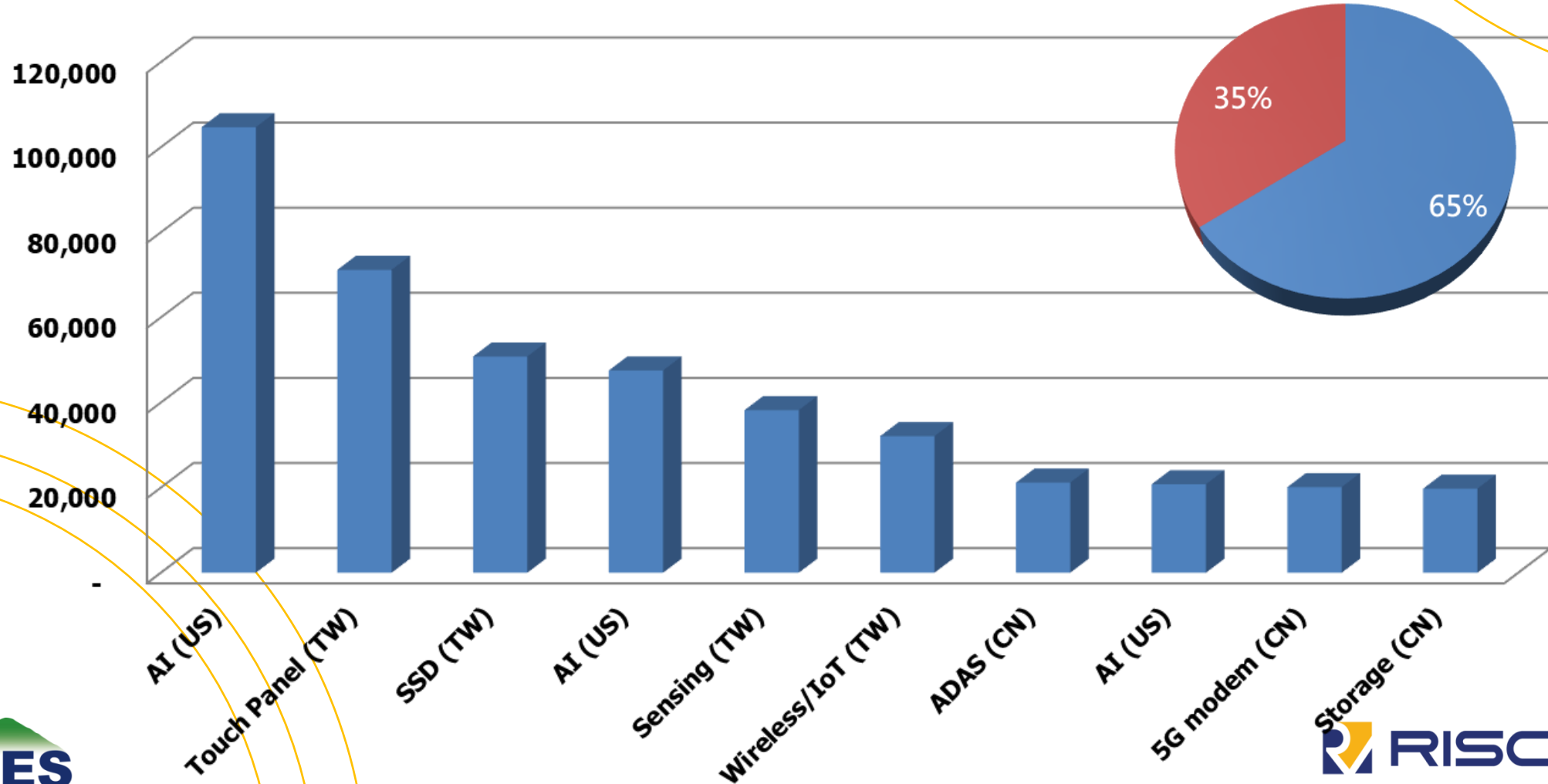
2023年前三季營業收入



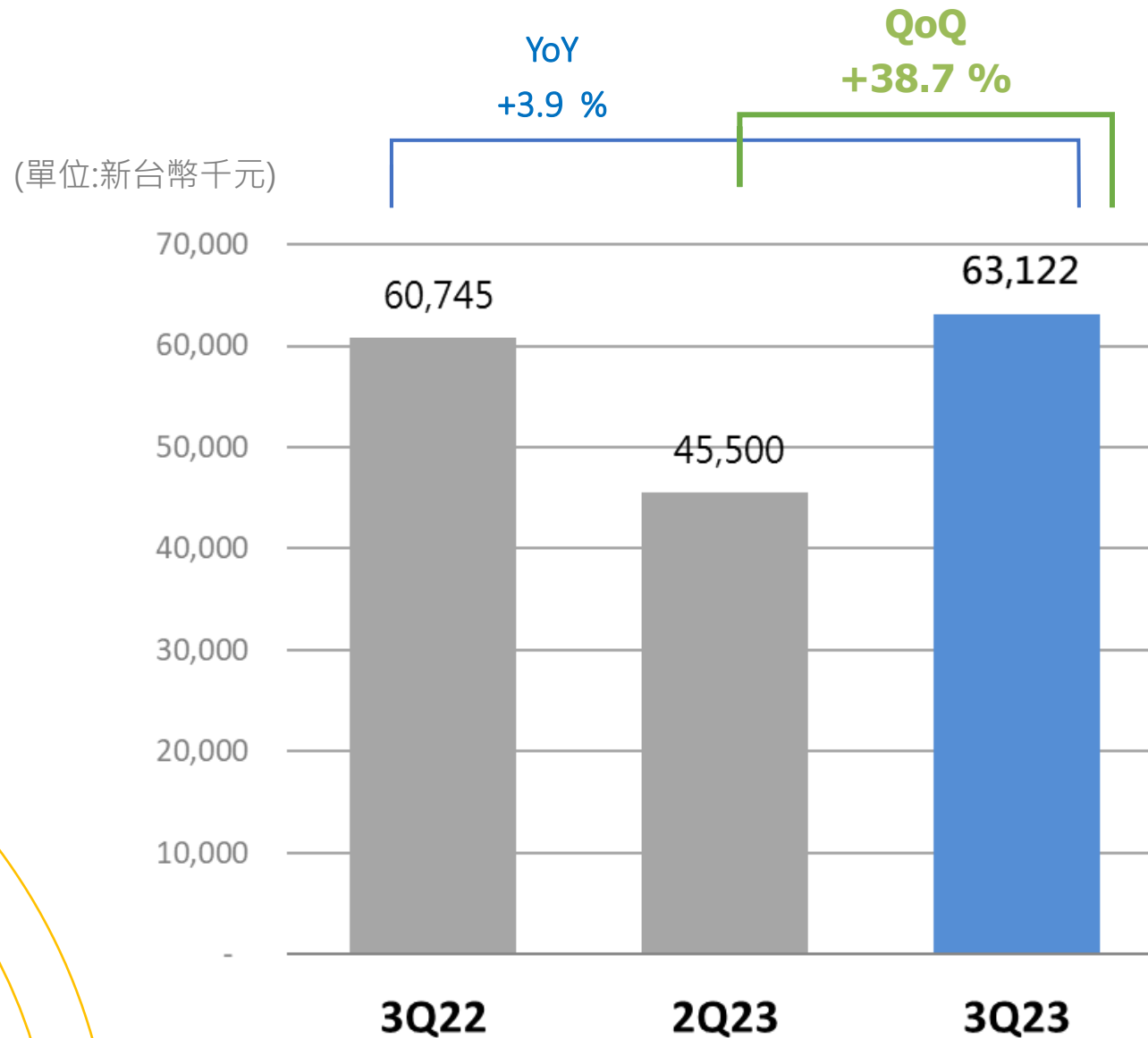
2023年前三季 前十大客戶之應用分析

單位: 新台幣千元

前十大客戶貢獻65%的營收



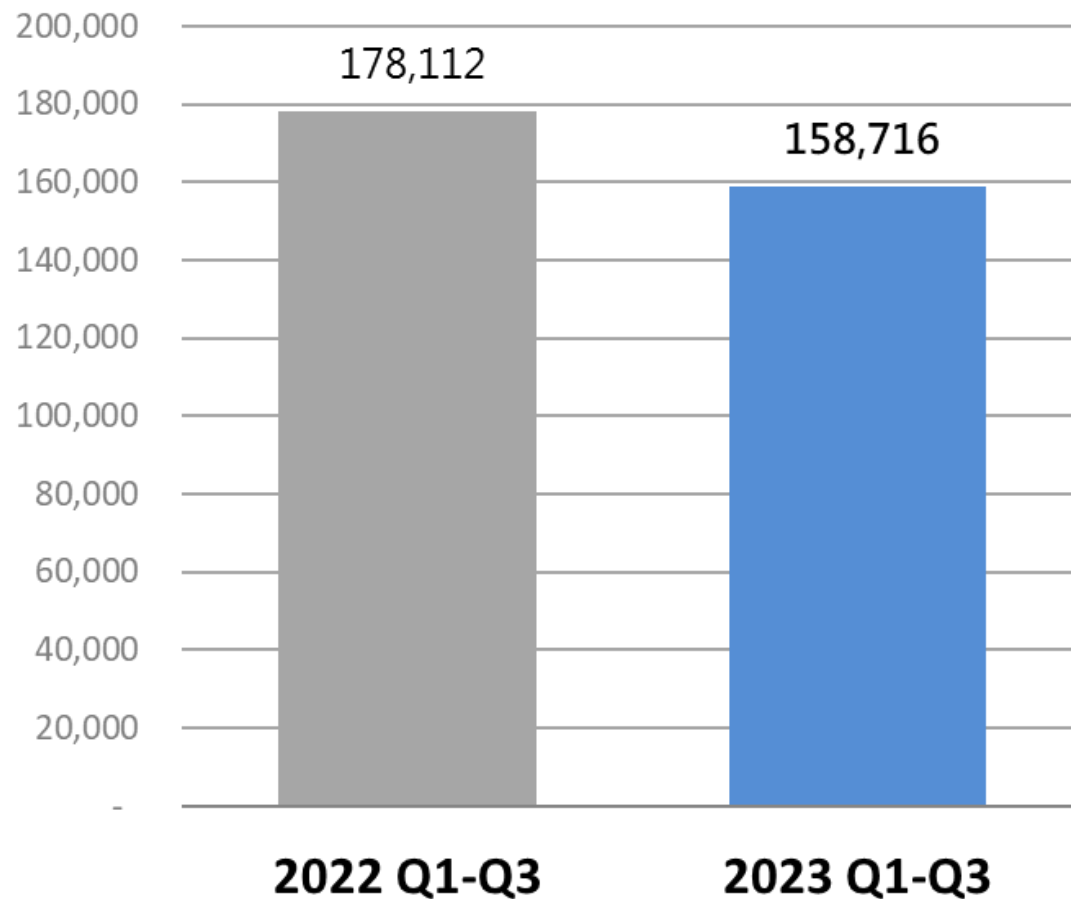
2023年第三季度 權利金收入



2023年前三季權利金收入

YoY
-10.9 %

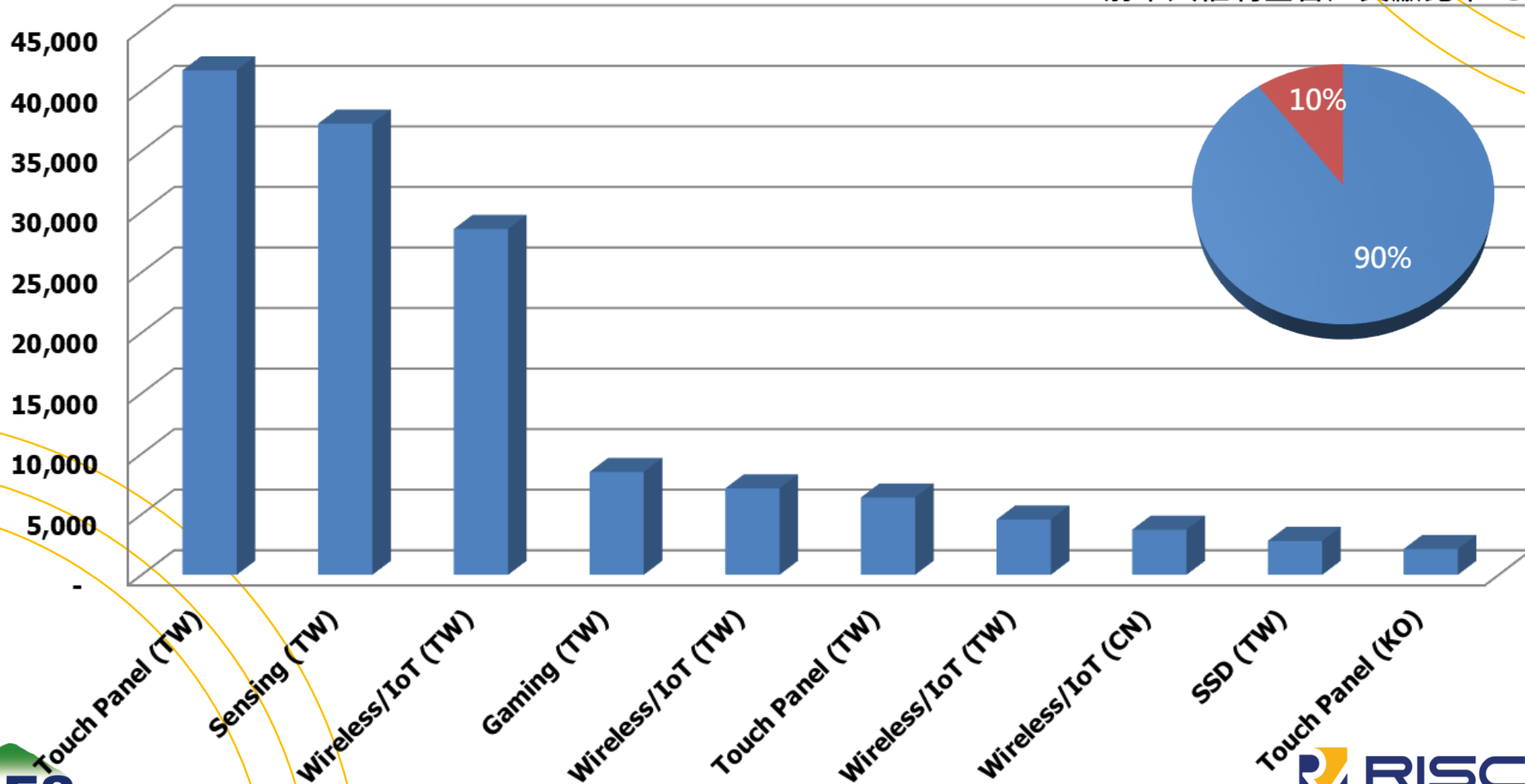
(單位:新台幣千元)



2023年前三季權利金應用分析

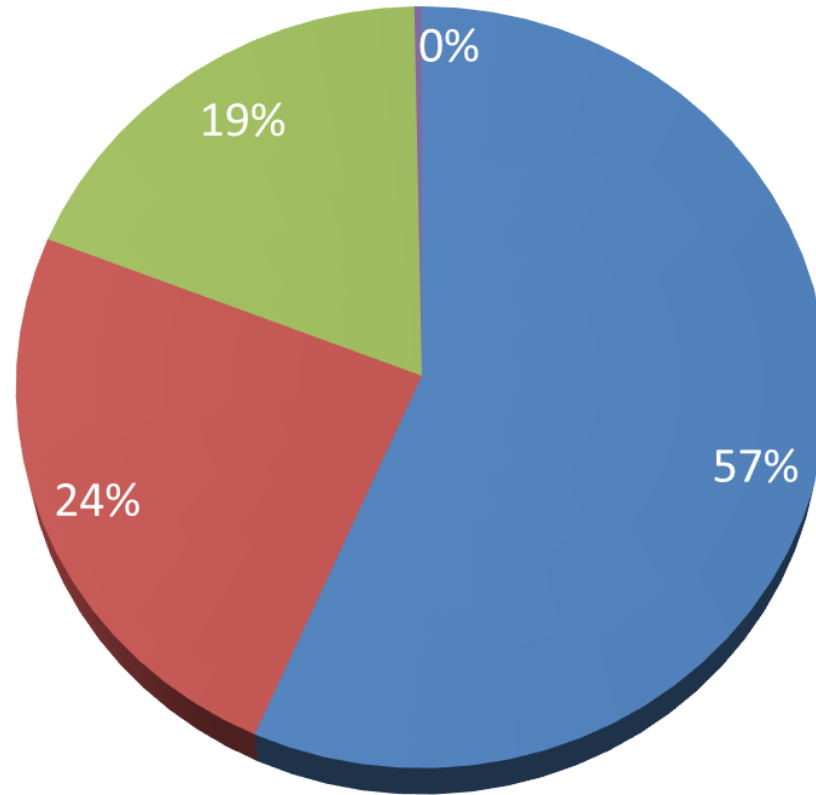
單位: 新台幣千元

前十大權利金客戶貢獻比率 90%



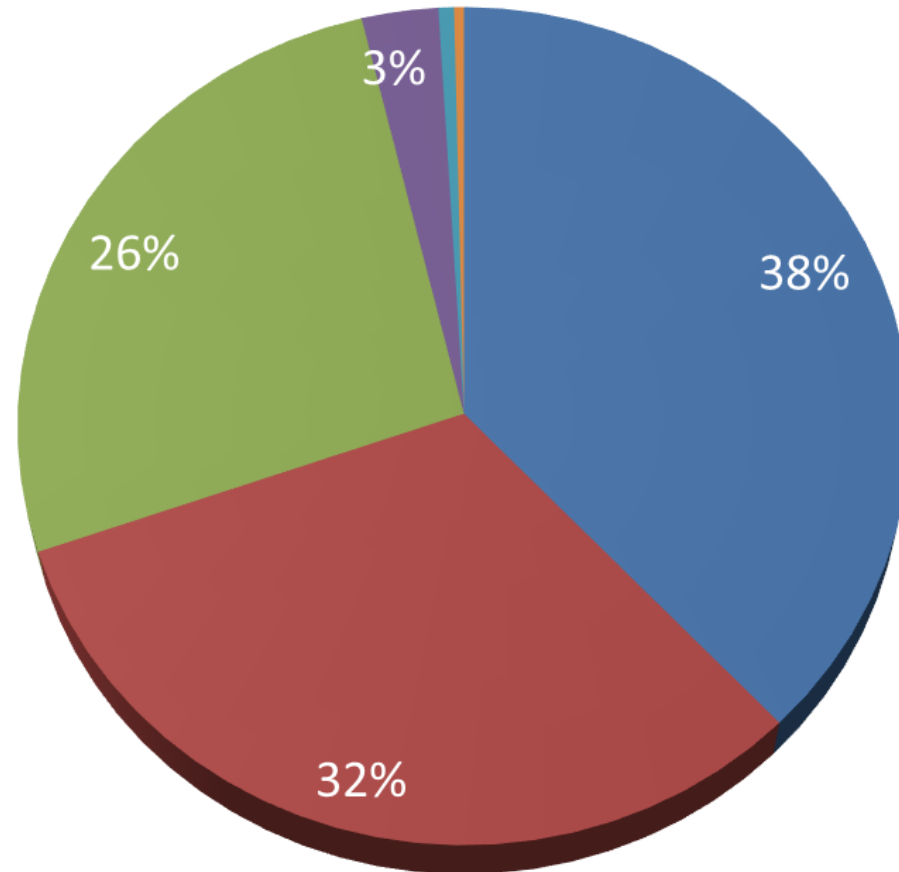
2023年前三季度 銷售分析-收入模式

■ License Fee ■ Running Royalty ■ Maintenance ■ Others

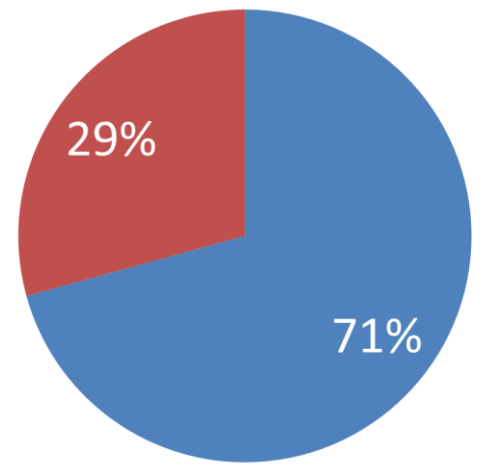


2023年前三季 銷售分析-地區別

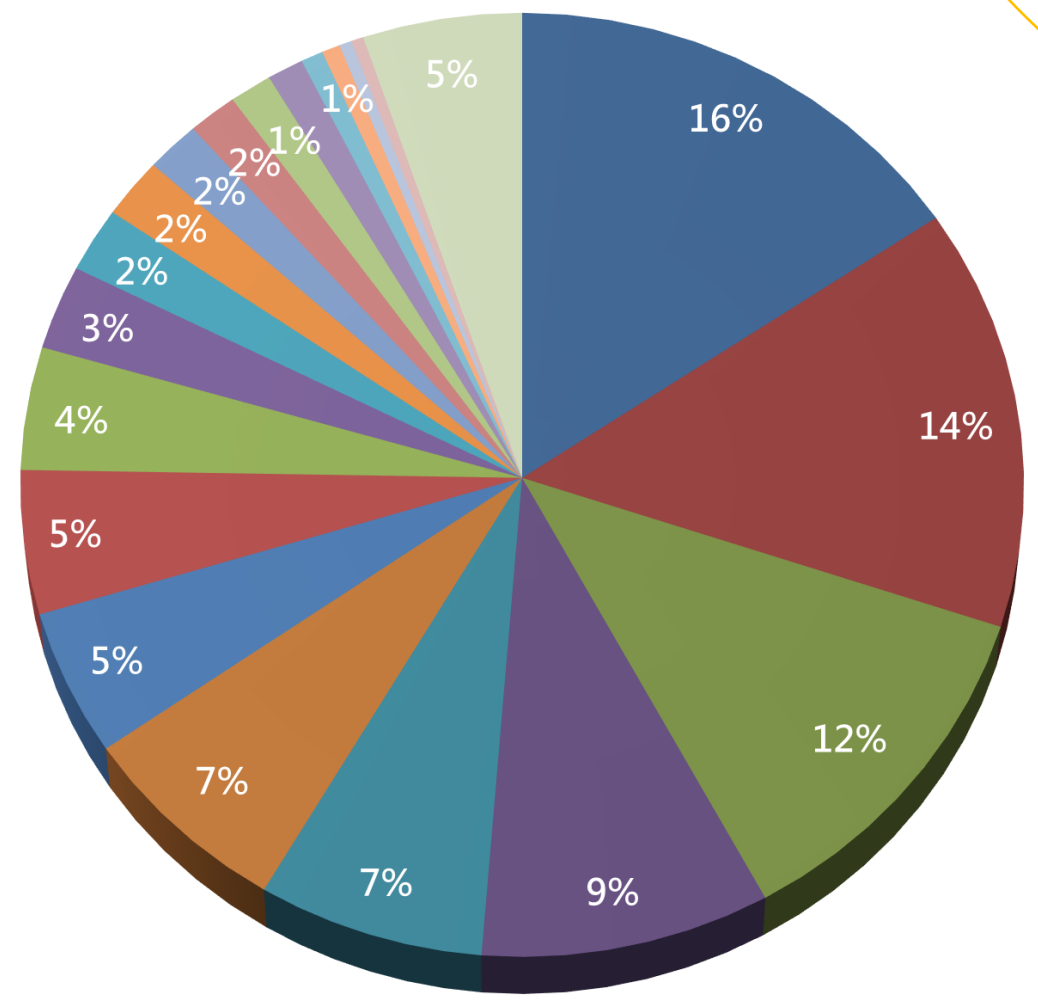
■ Taiwan ■ USA ■ China ■ Korea ■ Japan ■ Europe



2023年前三季度 銷售分析-產品別



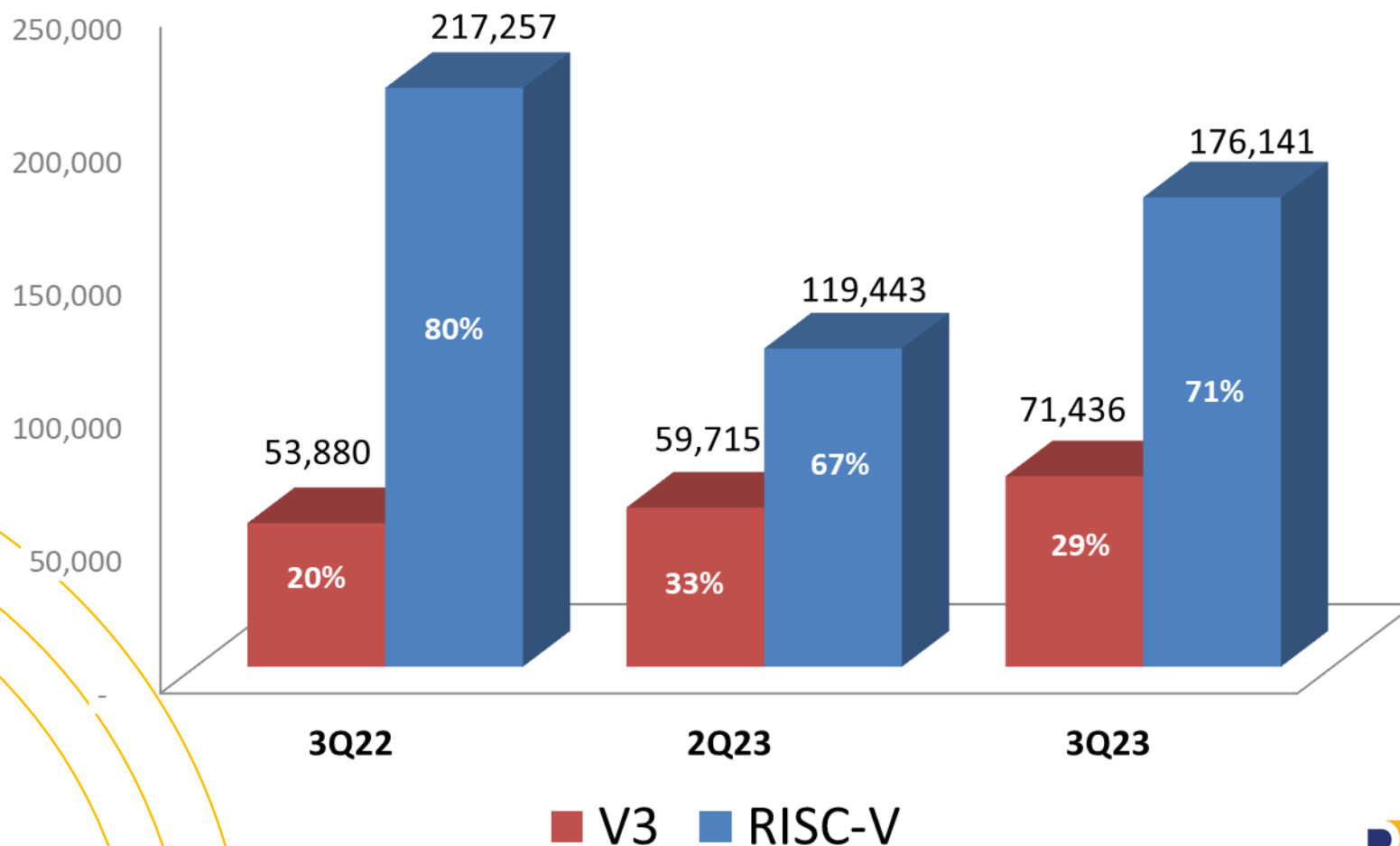
■ RISC-V
■ V3



- N25
- AX45
- N8
- NX45
- N9
- ACE
- N45
- NX27
- N10
- A45
- N13
- NX25
- LLVM
- D25
- N7
- D10
- E8
- AE250
- A27
- Pipeline
- OTHERS

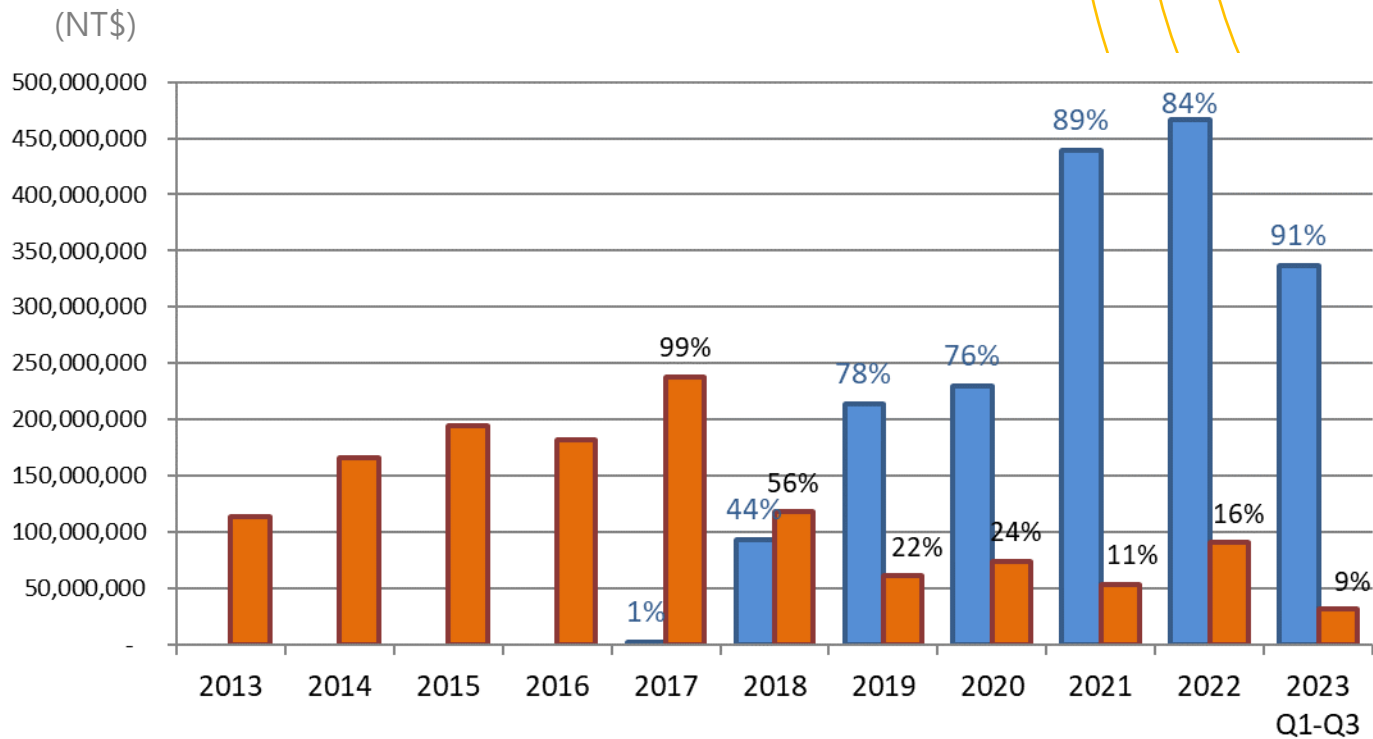
2023年前三季 銷售分析- RISC-V

(單位:新台幣千元)

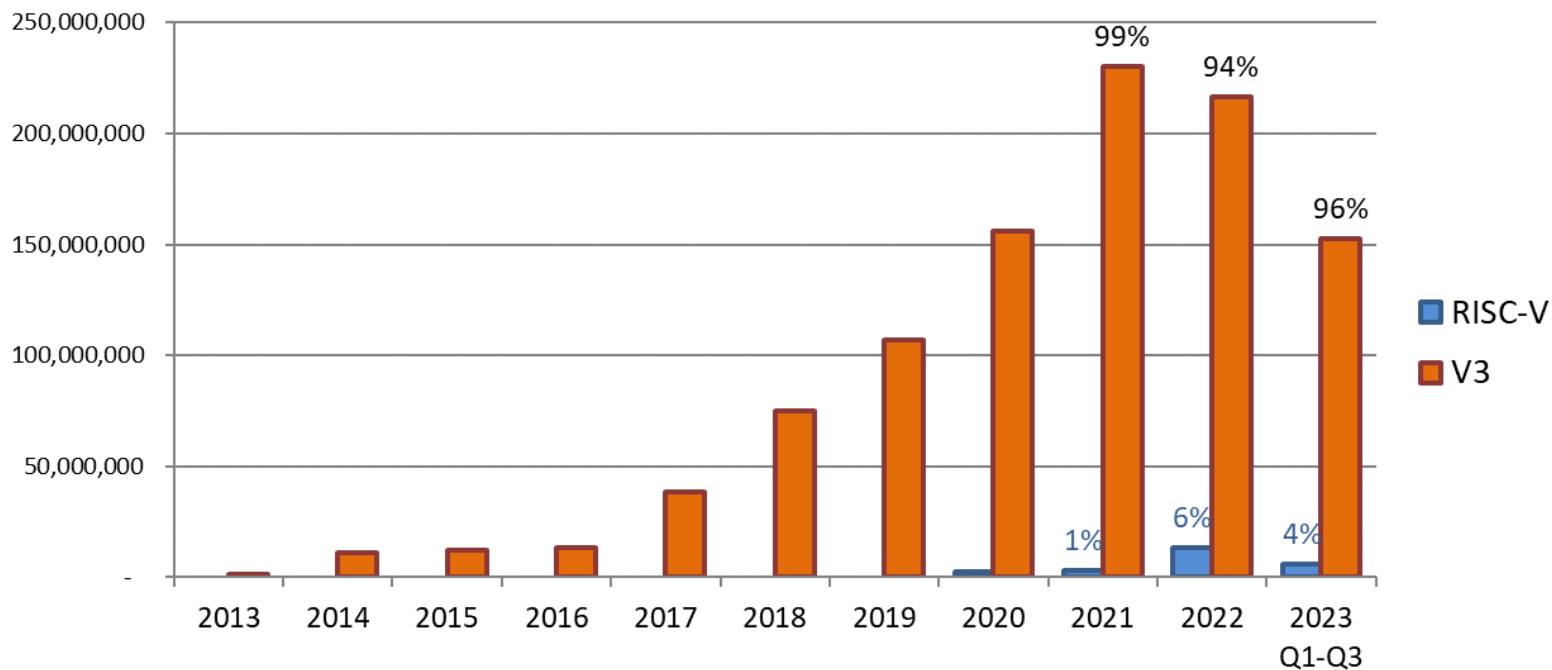


歷年收入分析

License

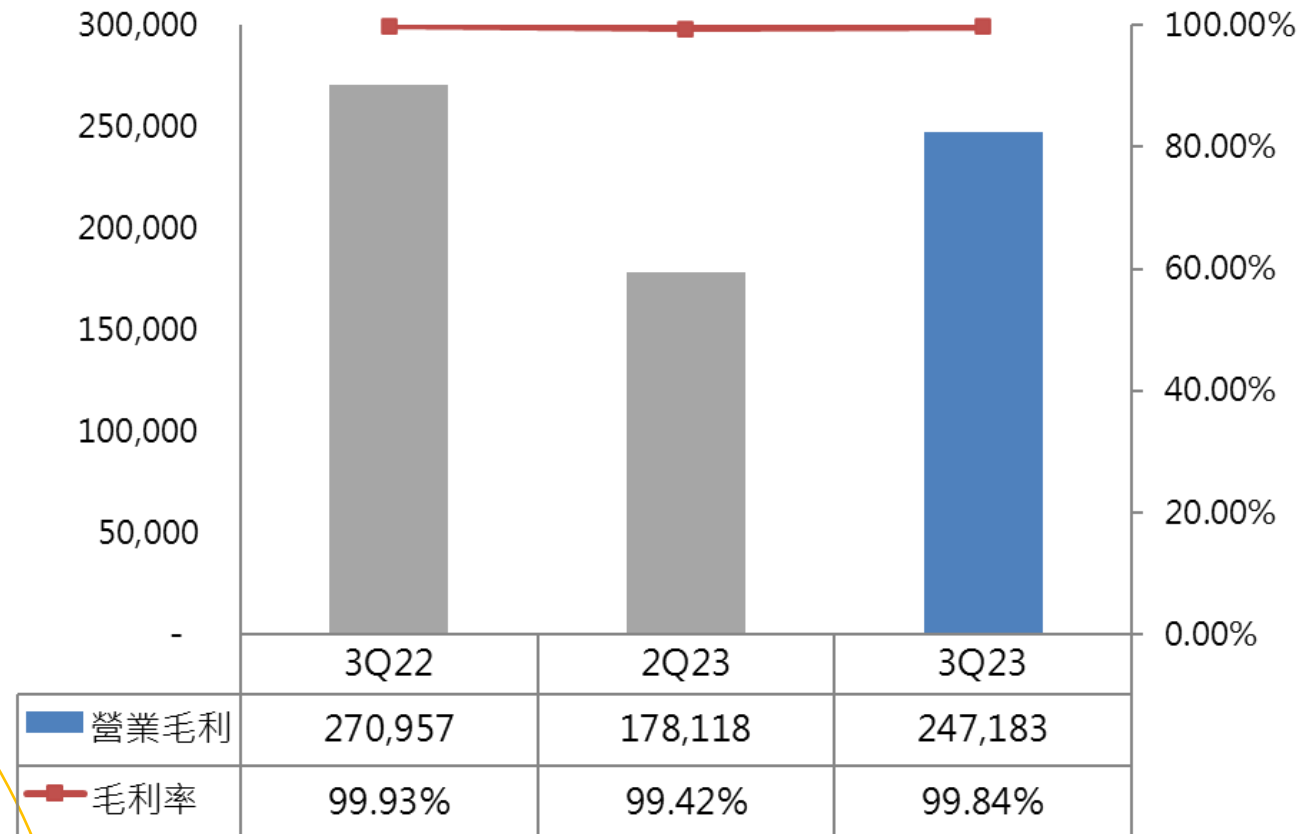


Royalty



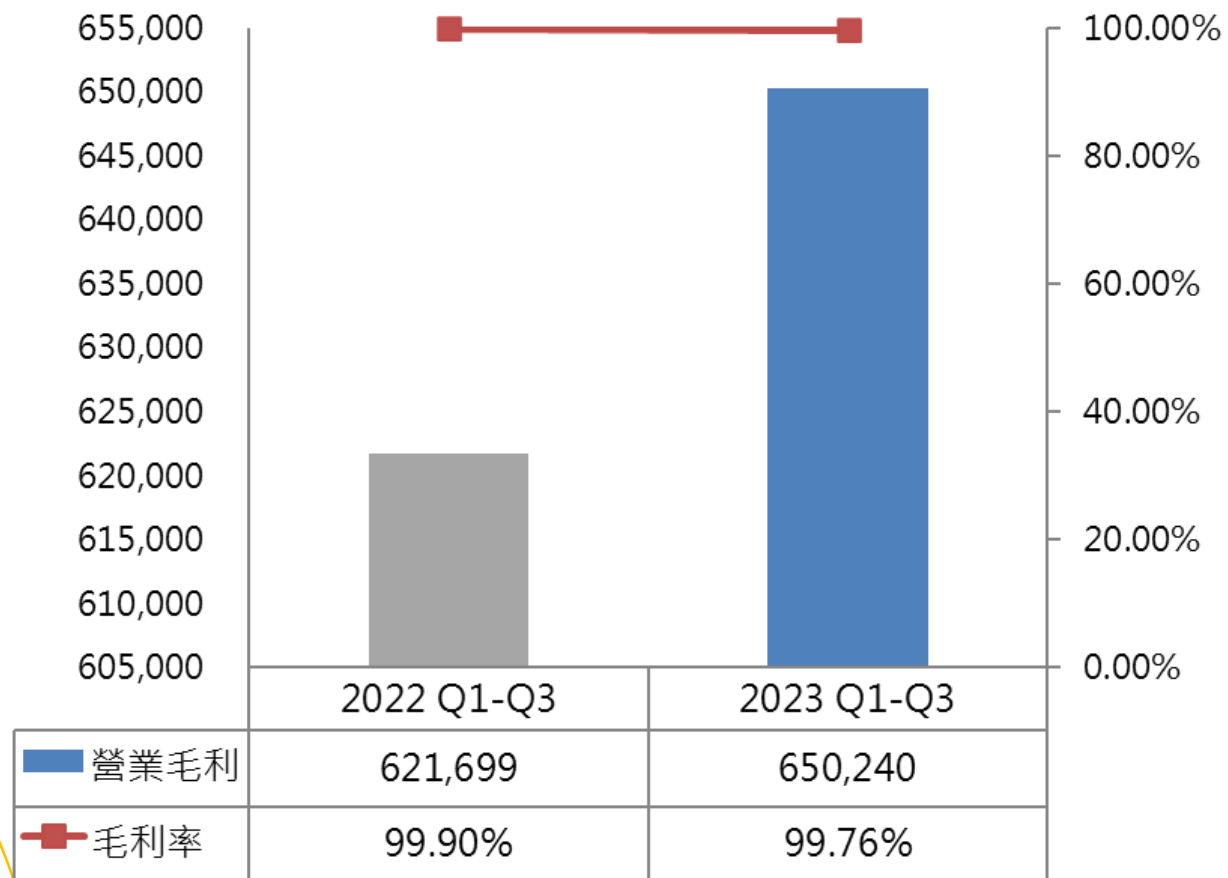
2023年第三季度 營業毛利與毛利率

(單位:新台幣千元)



2023年前三季營業毛利與毛利率

(單位:新台幣千元)

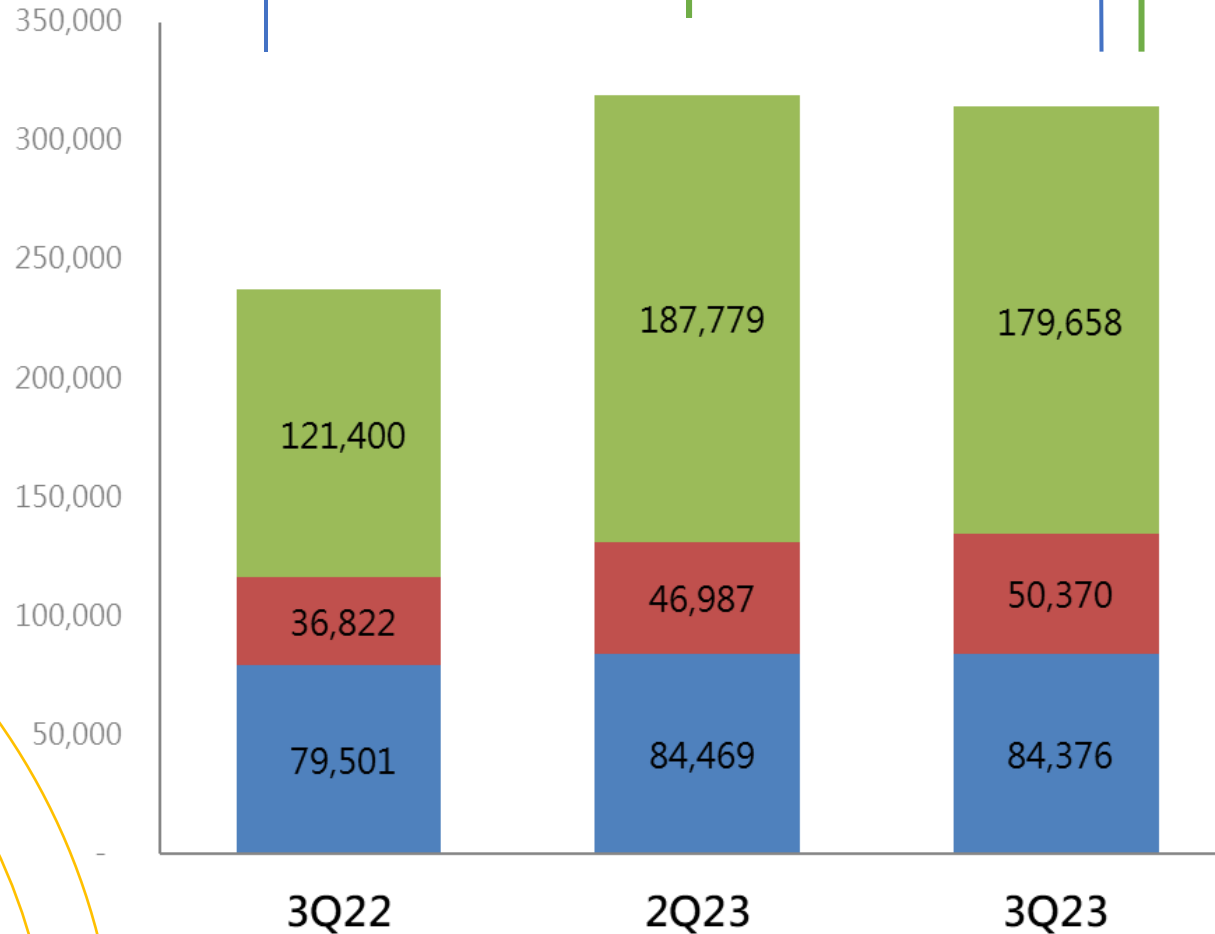


2023年第三季度 營業費用

YoY
+32.3 %

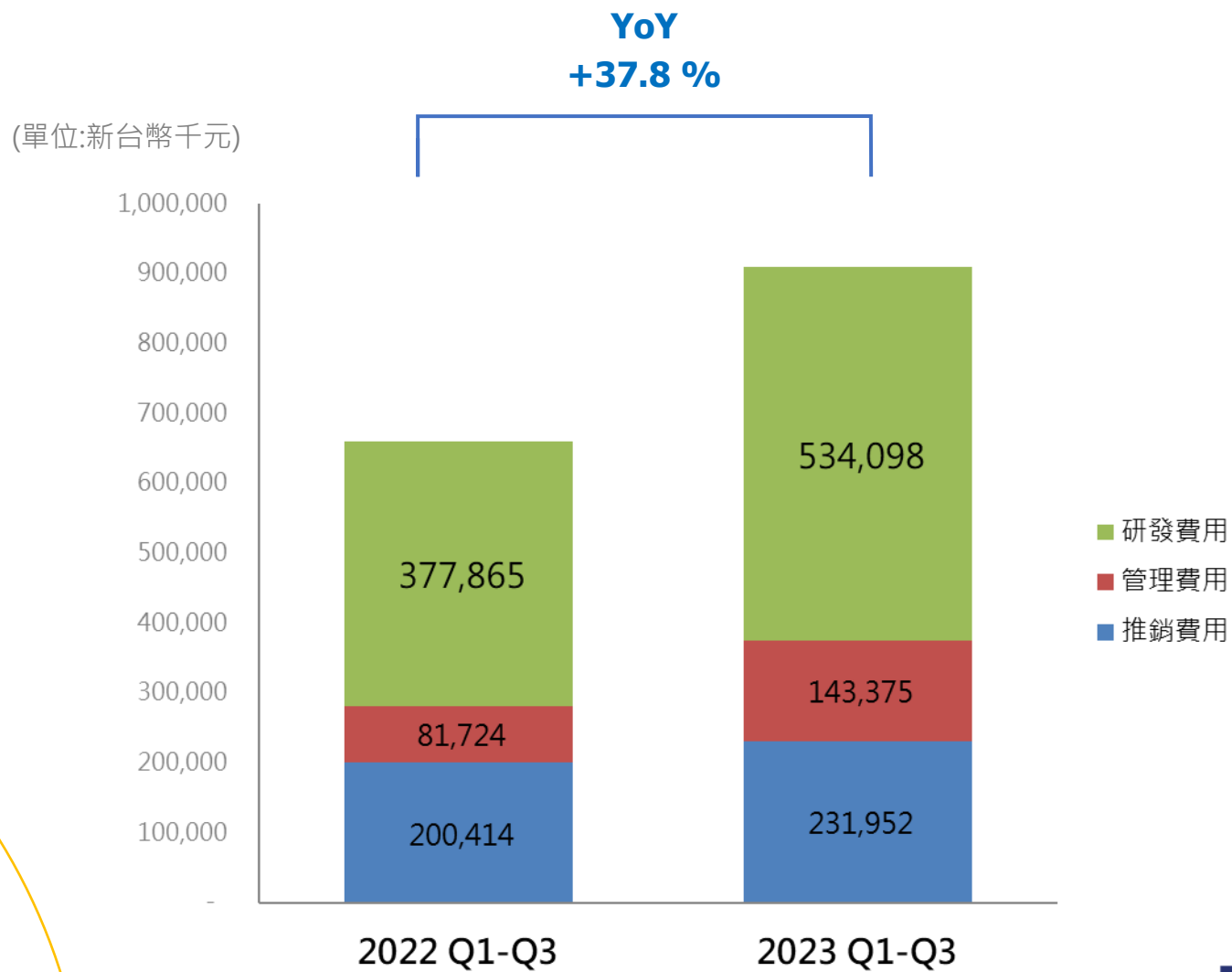
QoQ
-1.5 %

(單位:新台幣千元)

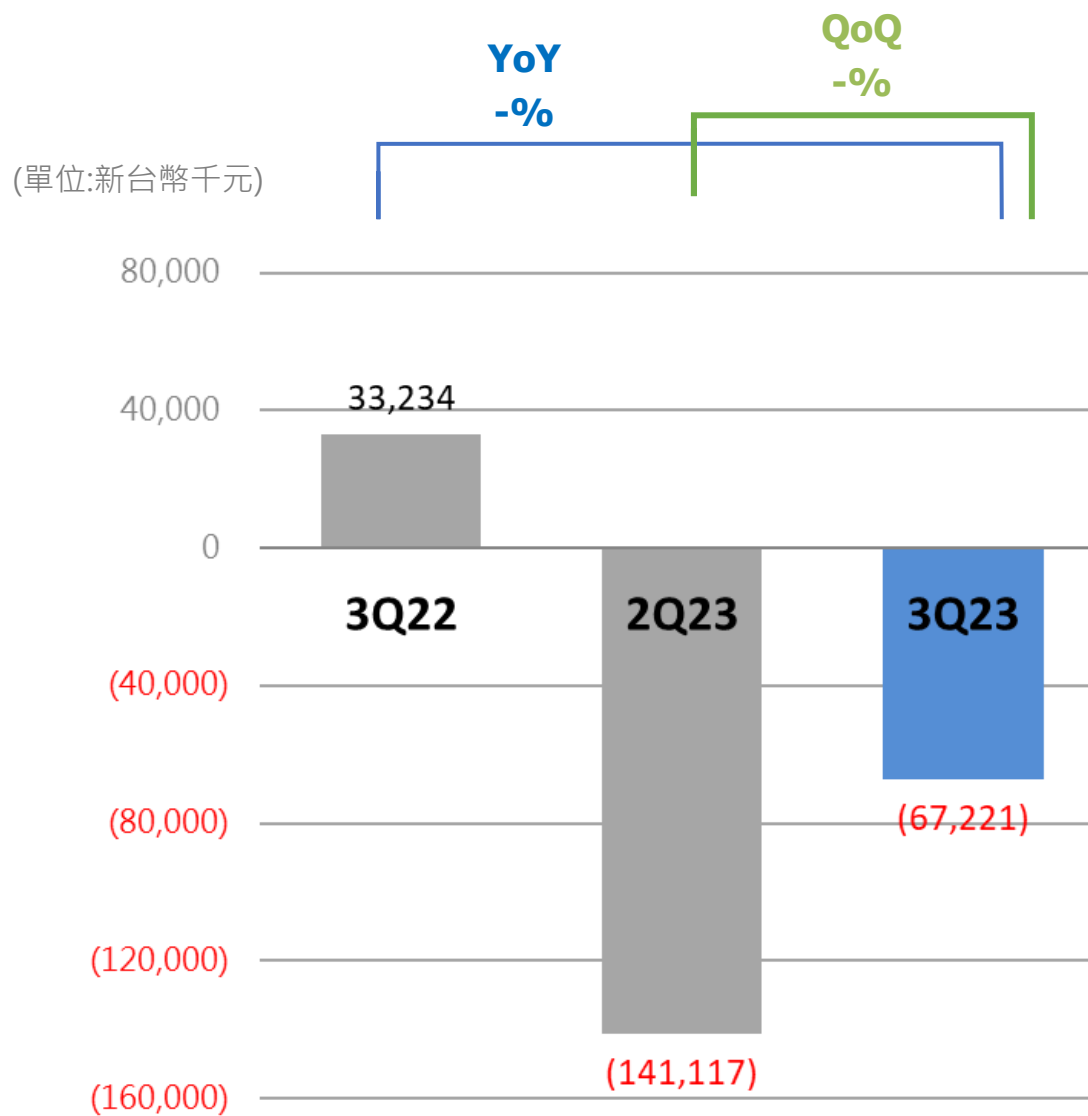


- 研發費用
- 管理費用
- 推銷費用

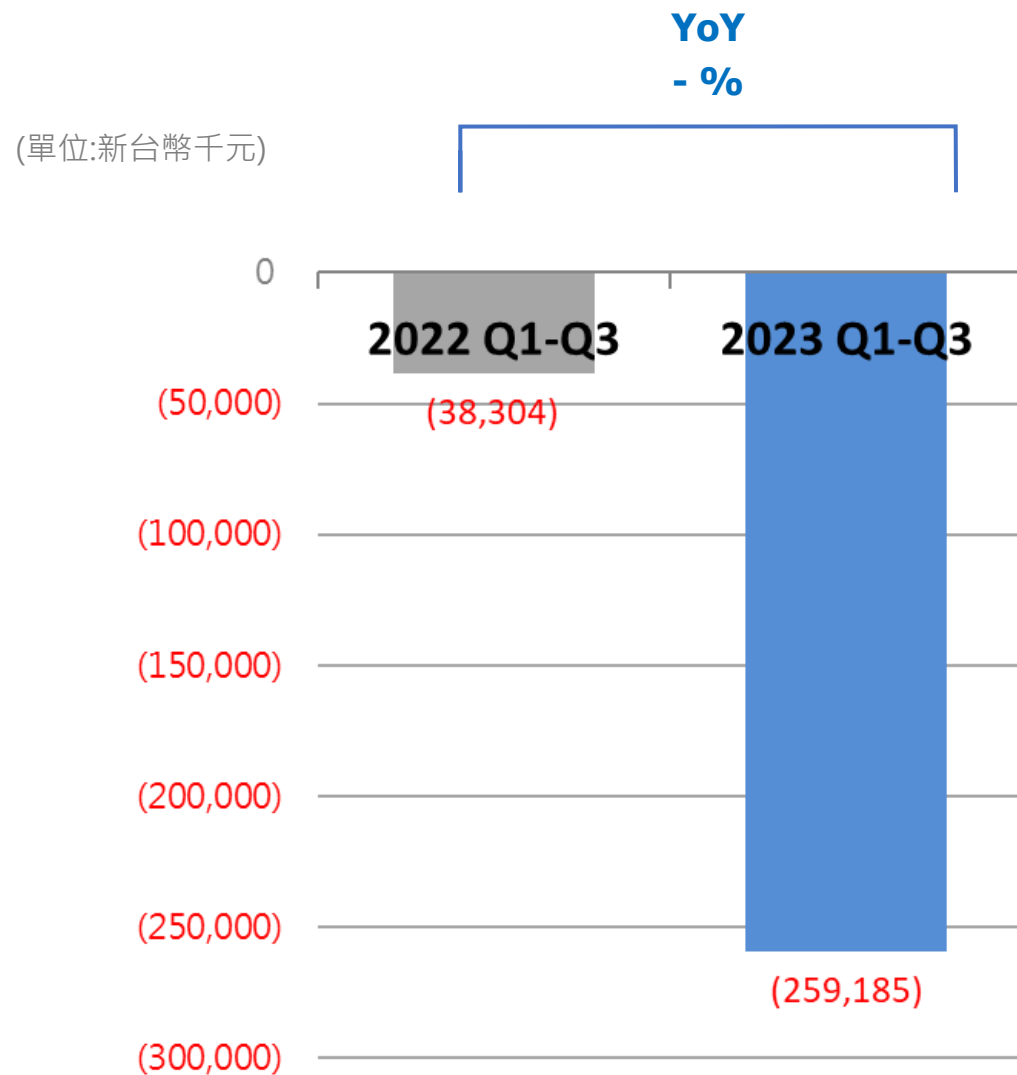
2023年前三季營業費用



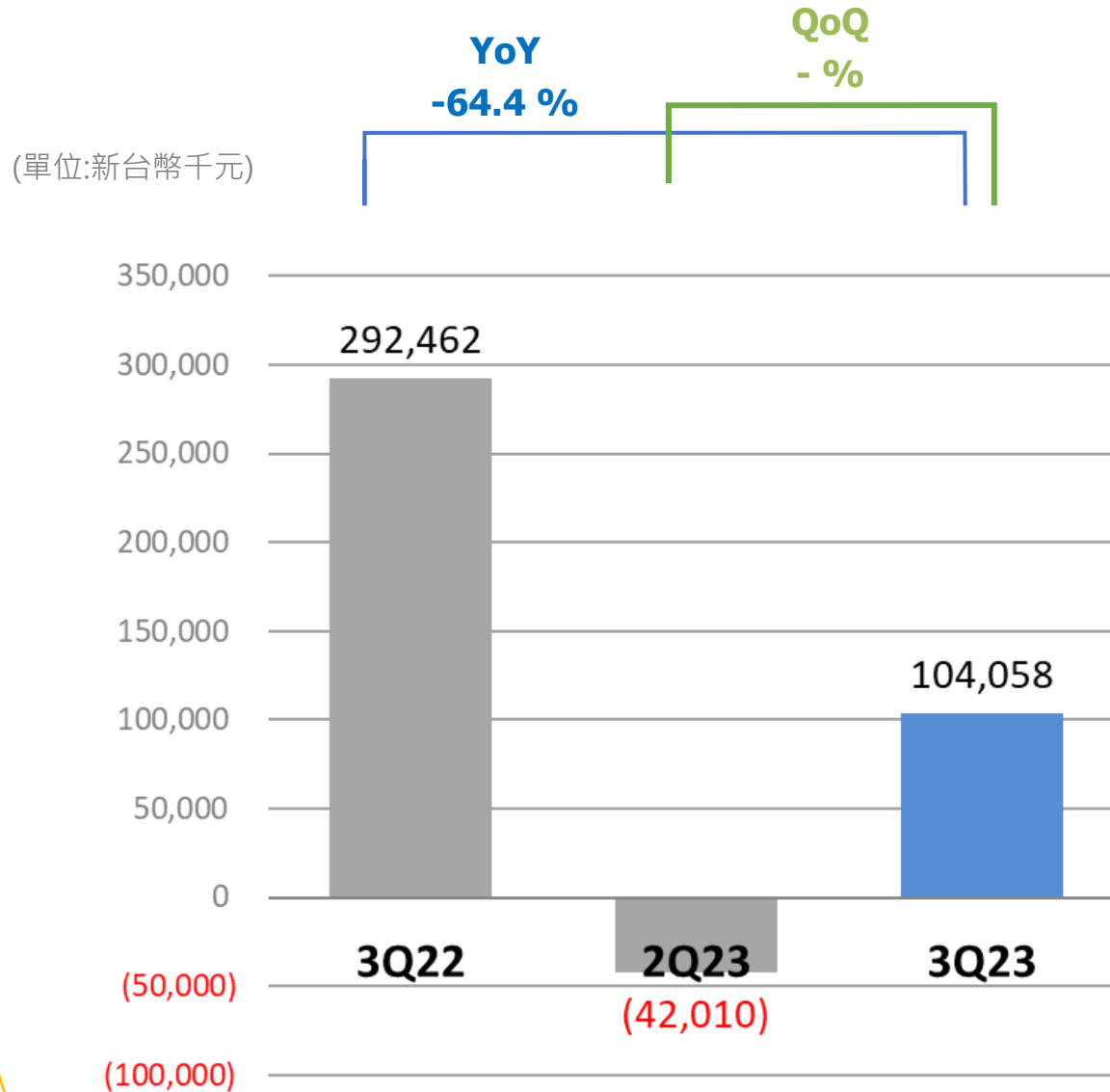
2023年第三季度 營業利益(損失)



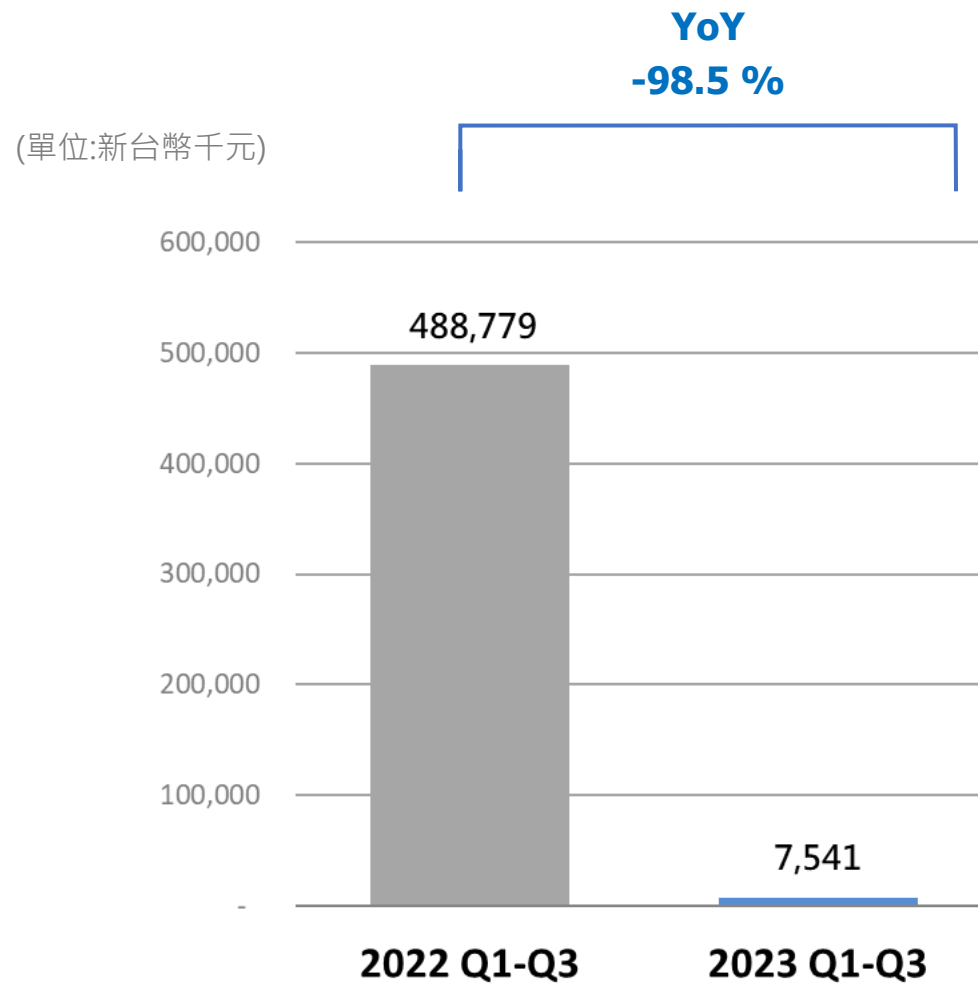
2023年前三季營業利益(損失)



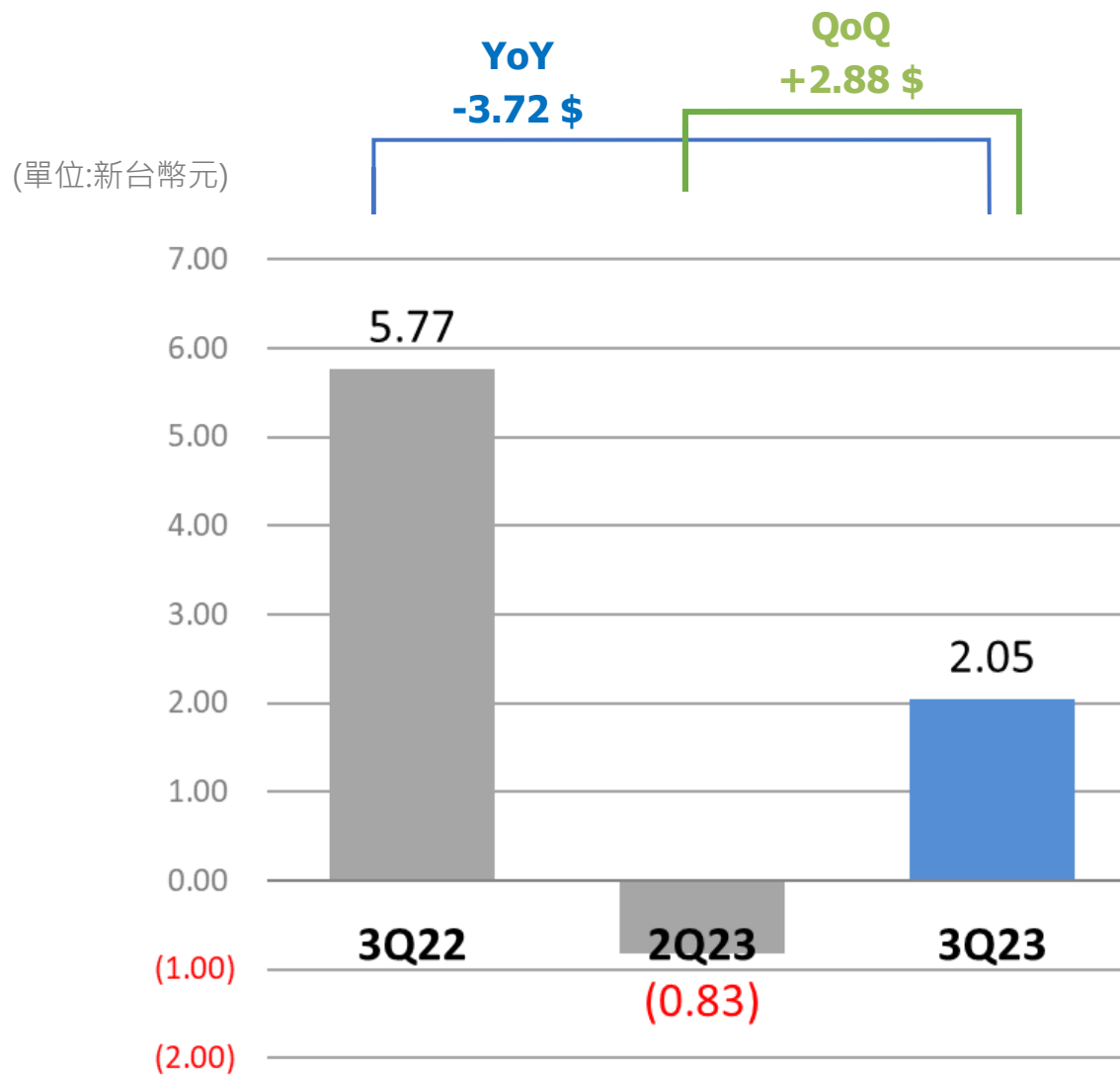
2023年第三季度 合併淨利(損)



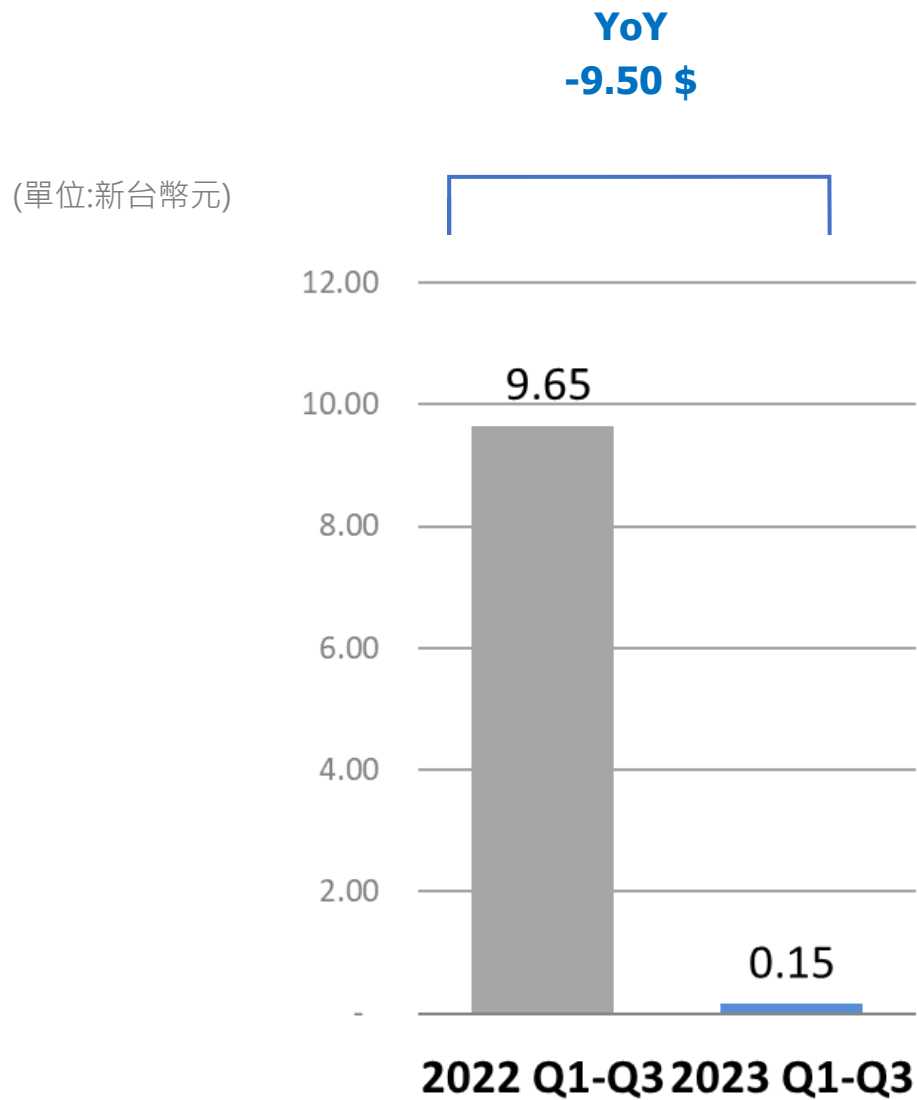
2023年前三季合併淨利



2023年第三季度 每股盈餘



2023年前三季 每股盈餘





產品應用

<http://www.andestech.com>



Andes RISC-V Powering Rich Applications



Mobile

Performance, code size

N25F, N45

MPU/MCU/AIoT

RENESAS
HPMicro
Kneron
Telink
Internet Company

D25F, D45, AX25MP, AX45MP

Endpoints. Edge. Cloud. Space.

Storage

PHISON

Performance, bandwidth, real-time

N25F, N45, AX45MP

5G Networks

EDGE
5G WITH AN EDGE
picocom
Empowering Wireless

N25F, A25, A45MP, AX45MP

Cloud AI

LIGHTELLIGENCE

STREAM COMPUTING 后摩智能 HOUMO.AI
SK telecom

Accelerate, accelerate, accelerate

NX27V, AX25, AX27, AX45MP, AX45MPV

Space

Secure, control, compute, communicate, position

N25F

MTIA: Meta Training and Inference Accelerator



- ISCA 2023 paper, “MTIA: First Generation Silicon Targeting Meta’s Recommendation Systems”
- Proc-A/B: Andes AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models



Figure 3: High-level architecture of the accelerator

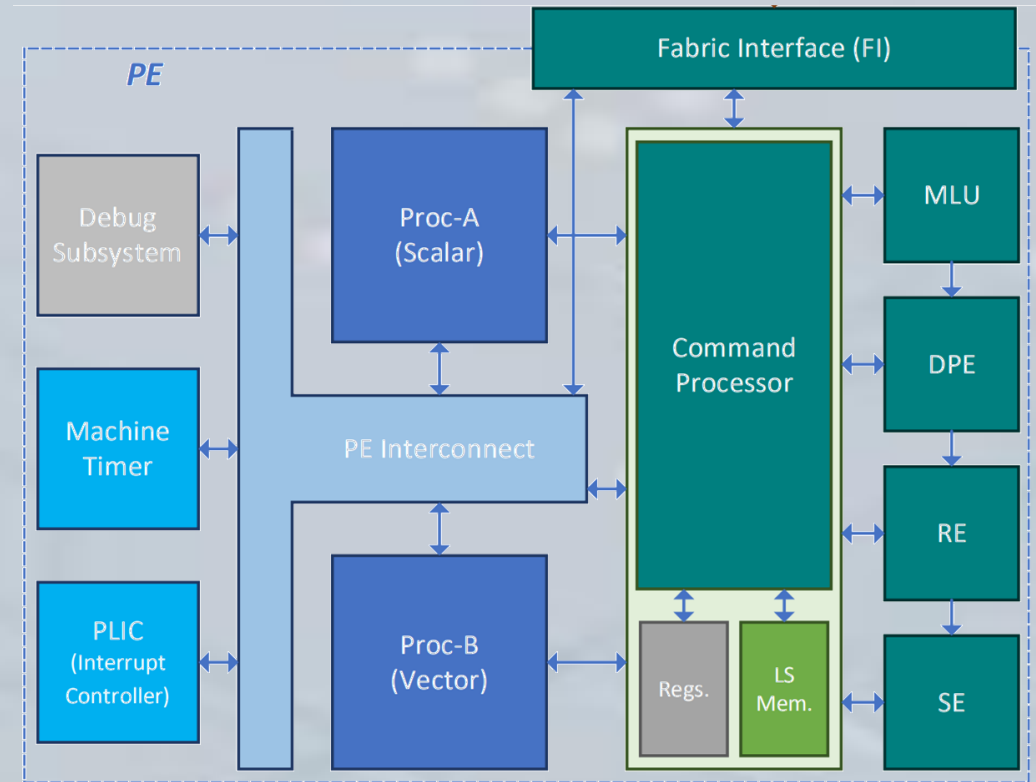


Figure 4: PE's internal organization

Powered by Andes NX27V+ACE

All photos: courtesy of ACM



New Products and Ecosystems

<http://www.andestech.com> 

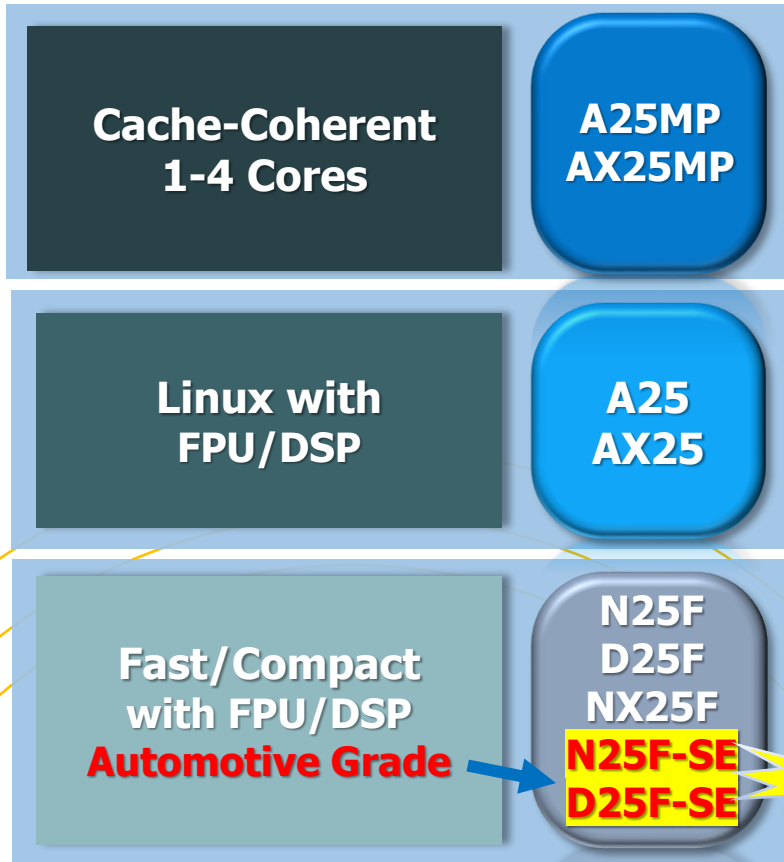
晶心RISC-V產品路線圖

RV32/RV64

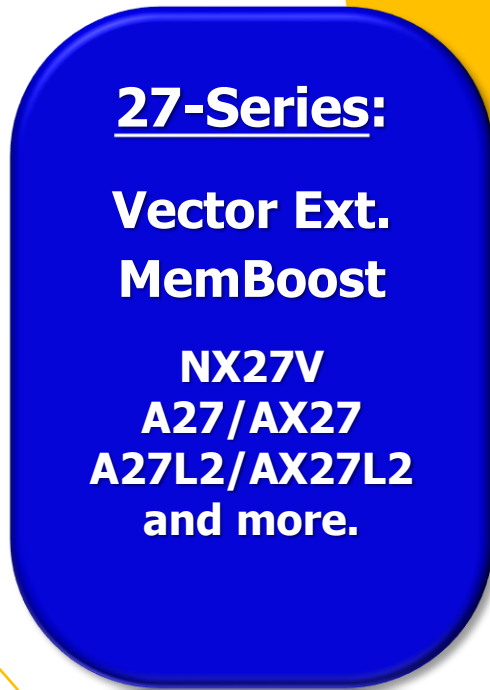
Vector Ext.

Superscalar

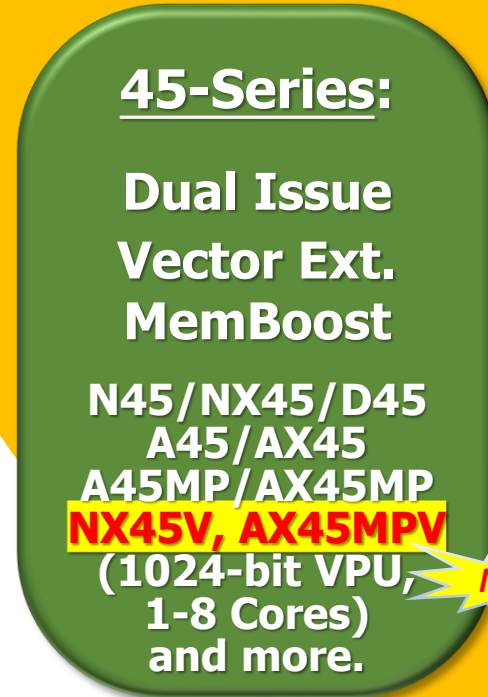
Out of Order



5-stage (1.1 GHz)



5-stage (1.1 GHz)



8-stage (1.2 GHz)



13-stage



Leading positions:

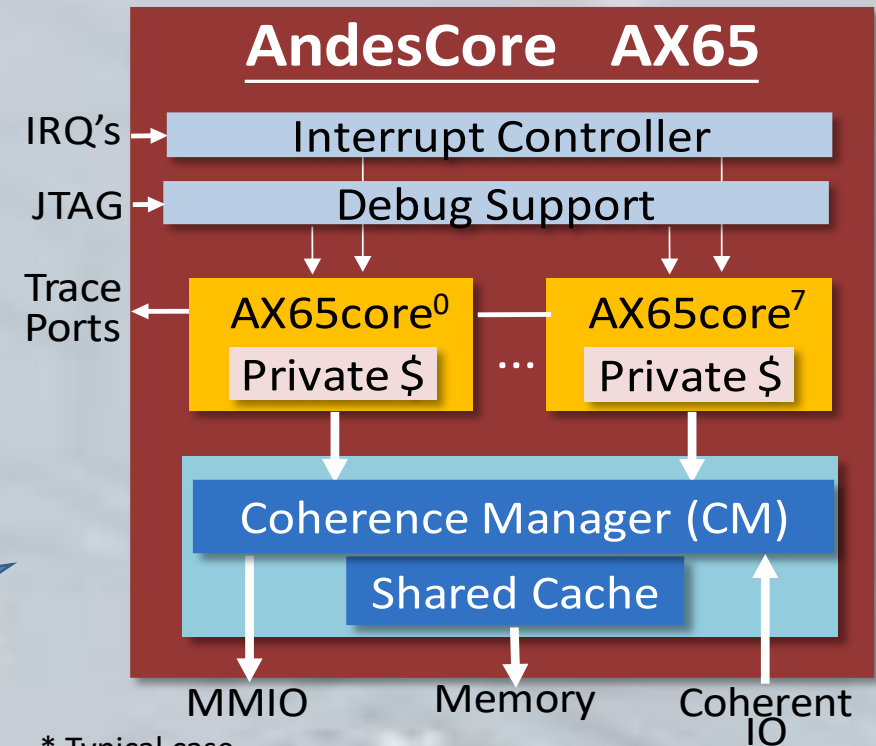
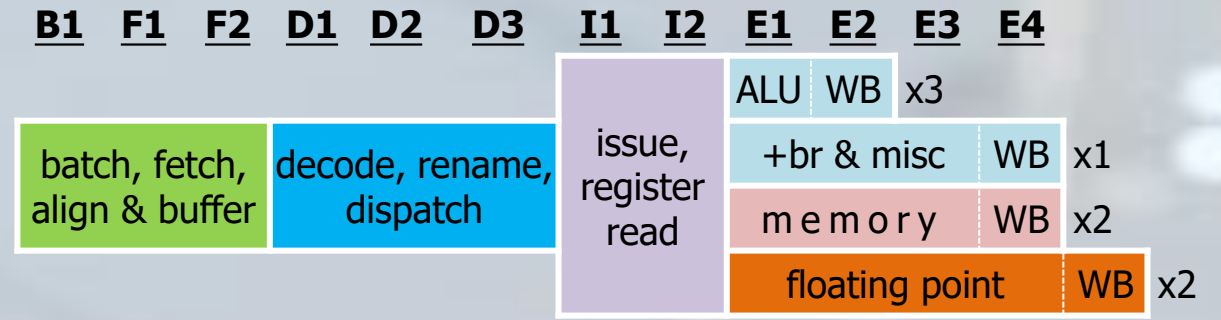
- ❖ The 1st company offering commercial RVP DSP CPU
- ❖ The 1st company offering the most updated spec of commercial RVV vector processor
- ❖ The 1st RISC-V core certified with ISO 26262 full compliance
- ❖ Tools for RISC-V custom extension: ACE

AndesCore™ AX65 000 Application Processor



- 13-stage 4-way 64-bit OOO processor
- RVA22+ profile
- Multicore cluster up to 8 cores
- 8 Execution Pipes: 4 ALU, 2 LD/ST, 2 FP
- 2-Level BTB with TAGE-L Branch Predictor
- Caches:
 - Private I/D caches: 64 KB, 4-way, 4-bank
 - Shared cache: up to 8 MB, 16-way
- 256-bit AXI4 for Memory, MMIO and IOCP
- Performance:
 - 2.4 GHz* @7nm without overdrive
 - Specint2006: 8.25/GHz
 - Specfp2006: 10.2/GHz

Best spec2k6 with 2-level caches



* Typical case

Roadmap for the AX60 Series



AX60 Series: 13-stage 000 Linux MP

AX45MPV Multicore Cluster



■ At multicore cluster level:

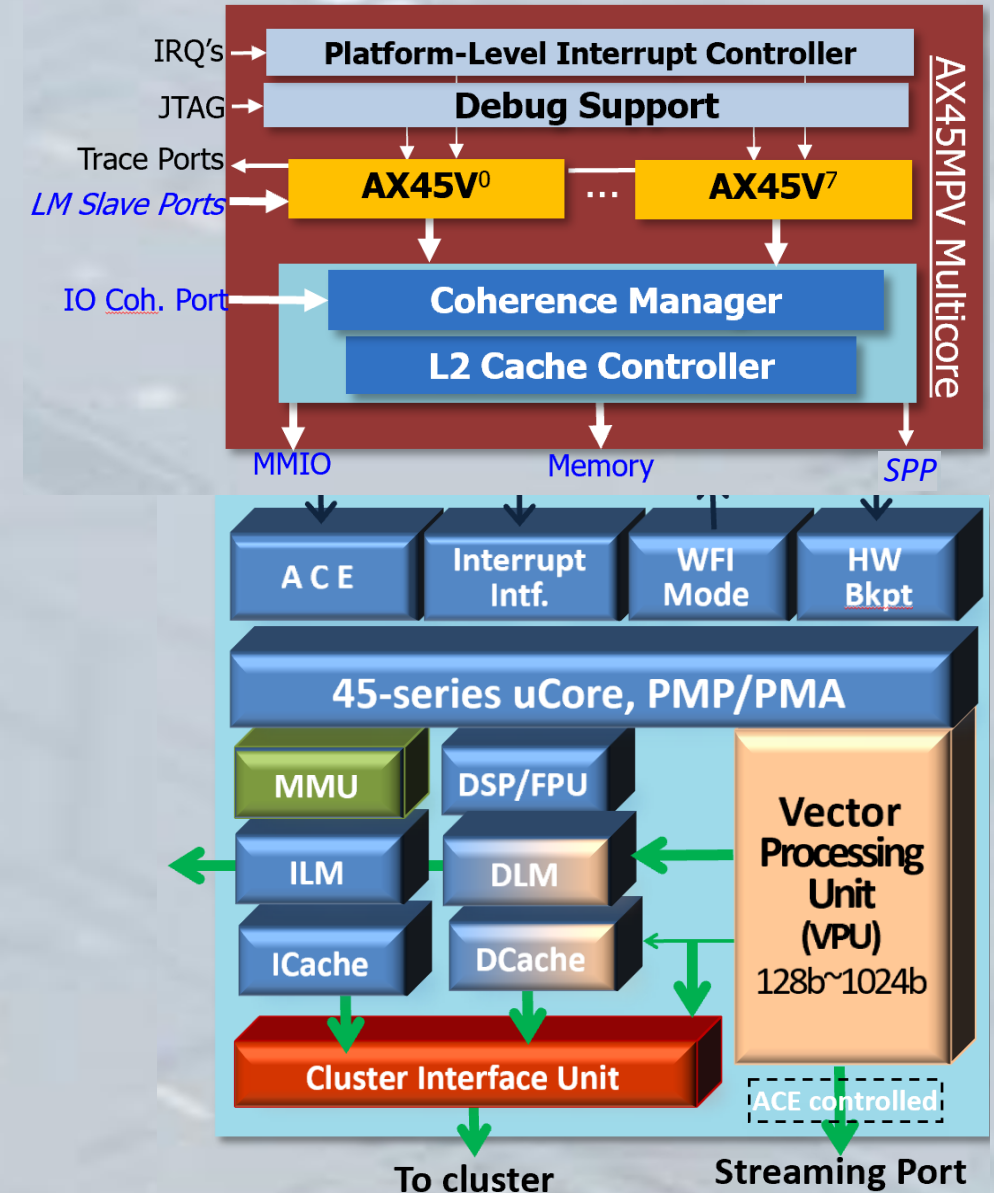
- Up to 8 cores
- CM/L2\$ subsystem
 - 128KB to 8MB, 64B line, 16-way
 - Multi-cycle support for high-density SRAMs
 - I/D prefetch, up to 64 outstanding requests
- AXI Bus Interfaces up to 512 bits

■ Scalar Unit: RV64GCBP

- 8-stage In-order dual-issue
- MMU/SV48, M/S/U modes
- I/D caches: 8K~64KB; Parity (I\$) or ECC (both)

■ RISC-V Vector Extension (RVV v1.0)

- data format: int8~64, fp16~64; int4, **bf16**
- VLEN/DLEN: 128~**1024** bits, 1:1 or 2:1 ratio
- Up to 6 DLEN results per cycle



AX45MPV: 1024-bit Vector Processor



■ RISC-V Vector Extension (RVV v1.0)

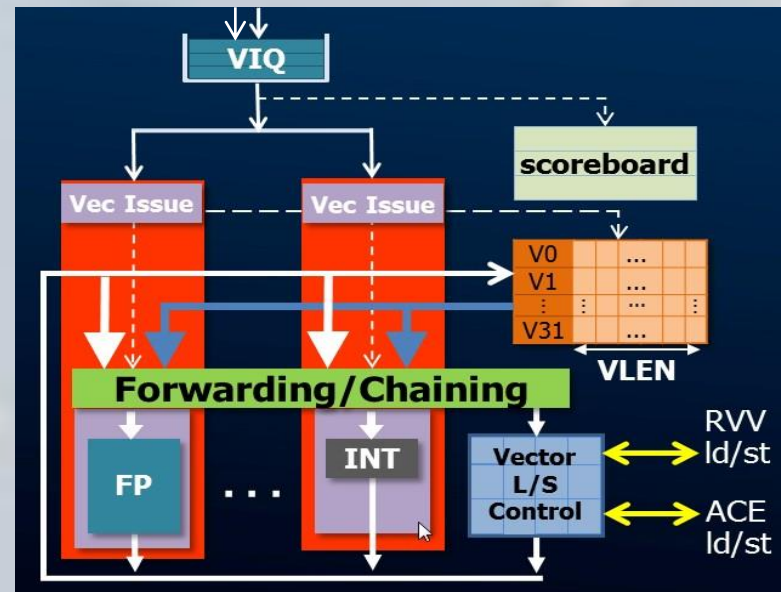
- data format: int8~64, fp16~64; int4, bf16
- VLEN/DLEN: 128~1024 bits, 1:1 or 2:1 ratio
- Up to 6 DLEN results per cycle

■ Efficient support needed for tight coupling with HWE

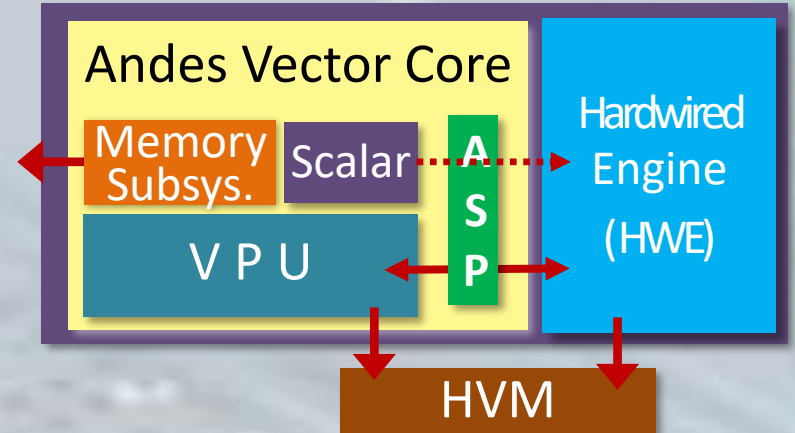
1. Data exchange performance (from/to shared memory in HWE)
2. Efficient control to the HWE

■ 2 solutions offered in AX45MPV:

- Andes Streaming Port™ (ASP) thru ACE
 - Data bus: data transfer btw VR and HWE
 - Command bus: to control/synchronize HWE operations
- HVM: High-speed Vector Memory
 - CPU side: DLEN-wide load/store interface with dynamic wait cycles
 - HVM module: accepting multiple accesses to multi-bank SRAM's



Processing Element (PE)




Andes is *Driving* Innovations in Automotive



with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar



Radio	Radar Subsystem N25F-SE	Host Controller N25F-SE
	Memory	Peripheral

CMOS Sensor

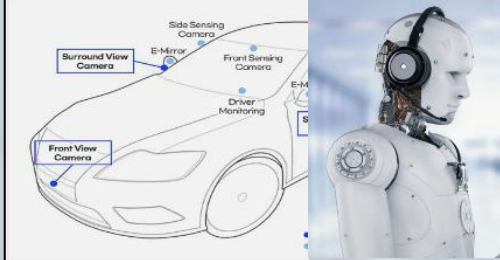
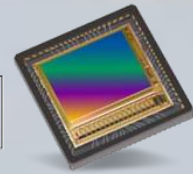



Diagram illustrating the integration of CMOS sensors in automotive applications, showing various sensor types (Surround View Camera, Front Sensing Camera, Driver Monitoring, E-Mirror, Side Sensing Camera, Front View Camera) and their connection to a central processing unit (CPU) and other components like Memory, Peripheral, and Host Controller.

Auto TDDI








Diagram illustrating the integration of TDDI (Time-to-Digital Converter) in automotive applications, showing its connection to various components like Main Board, RAM, and Display & Output.

Auto MCU




芯片	MCU	微处理器
AD9PAC1	RISC-V CPU 0	ARM V7-M
AD9PAC2	RISC-V CPU 1	ARM V7-M
AD9PAC3	RISC-V CPU 2	ARM V7-M
AD9PAC4	RISC-V CPU 3	ARM V7-M
AD9PAC5	RISC-V CPU 4	ARM V7-M
AD9PAC6	RISC-V CPU 5	ARM V7-M
AD9PAC7	RISC-V CPU 6	ARM V7-M
AD9PAC8	RISC-V CPU 7	ARM V7-M
AD9PAC9	RISC-V CPU 8	ARM V7-M
AD9PAC10	RISC-V CPU 9	ARM V7-M
AD9PAC11	RISC-V CPU 10	ARM V7-M
AD9PAC12	RISC-V CPU 11	ARM V7-M
AD9PAC13	RISC-V CPU 12	ARM V7-M
AD9PAC14	RISC-V CPU 13	ARM V7-M
AD9PAC15	RISC-V CPU 14	ARM V7-M
AD9PAC16	RISC-V CPU 15	ARM V7-M
AD9PAC17	RISC-V CPU 16	ARM V7-M
AD9PAC18	RISC-V CPU 17	ARM V7-M
AD9PAC19	RISC-V CPU 18	ARM V7-M
AD9PAC20	RISC-V CPU 19	ARM V7-M
AD9PAC21	RISC-V CPU 20	ARM V7-M
AD9PAC22	RISC-V CPU 21	ARM V7-M
AD9PAC23	RISC-V CPU 22	ARM V7-M
AD9PAC24	RISC-V CPU 23	ARM V7-M
AD9PAC25	RISC-V CPU 24	ARM V7-M
AD9PAC26	RISC-V CPU 25	ARM V7-M
AD9PAC27	RISC-V CPU 26	ARM V7-M
AD9PAC28	RISC-V CPU 27	ARM V7-M
AD9PAC29	RISC-V CPU 28	ARM V7-M
AD9PAC30	RISC-V CPU 29	ARM V7-M
AD9PAC31	RISC-V CPU 30	ARM V7-M
AD9PAC32	RISC-V CPU 31	ARM V7-M
AD9PAC33	RISC-V CPU 32	ARM V7-M
AD9PAC34	RISC-V CPU 33	ARM V7-M
AD9PAC35	RISC-V CPU 34	ARM V7-M
AD9PAC36	RISC-V CPU 35	ARM V7-M
AD9PAC37	RISC-V CPU 36	ARM V7-M
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AD9PAC40	RISC-V CPU 39	ARM V7-M
AD9PAC41	RISC-V CPU 40	ARM V7-M
AD9PAC42	RISC-V CPU 41	ARM V7-M
AD9PAC43	RISC-V CPU 42	ARM V7-M
AD9PAC44	RISC-V CPU 43	ARM V7-M
AD9PAC45	RISC-V CPU 44	ARM V7-M
AD9PAC46	RISC-V CPU 45	ARM V7-M
AD9PAC47	RISC-V CPU 46	ARM V7-M
AD9PAC48	RISC-V CPU 47	ARM V7-M
AD9PAC49	RISC-V CPU 48	ARM V7-M
AD9PAC50	RISC-V CPU 49	ARM V7-M
AD9PAC51	RISC-V CPU 50	ARM V7-M
AD9PAC52	RISC-V CPU 51	ARM V7-M
AD9PAC53	RISC-V CPU 52	ARM V7-M
AD9PAC54	RISC-V CPU 53	ARM V7-M
AD9PAC55	RISC-V CPU 54	ARM V7-M
AD9PAC56	RISC-V CPU 55	ARM V7-M
AD9PAC57	RISC-V CPU 56	ARM V7-M
AD9PAC58	RISC-V CPU 57	ARM V7-M
AD9PAC59	RISC-V CPU 58	ARM V7-M
AD9PAC60	RISC-V CPU 59	ARM V7-M
AD9PAC61	RISC-V CPU 60	ARM V7-M
AD9PAC62	RISC-V CPU 61	ARM V7-M
AD9PAC63	RISC-V CPU 62	ARM V7-M
AD9PAC64	RISC-V CPU 63	ARM V7-M
AD9PAC65	RISC-V CPU 64	ARM V7-M
AD9PAC66	RISC-V CPU 65	ARM V7-M
AD9PAC67	RISC-V CPU 66	ARM V7-M
AD9PAC68	RISC-V CPU 67	ARM V7-M
AD9PAC69	RISC-V CPU 68	ARM V7-M
AD9PAC70	RISC-V CPU 69	ARM V7-M
AD9PAC71	RISC-V CPU 70	ARM V7-M
AD9PAC72	RISC-V CPU 71	ARM V7-M
AD9PAC73	RISC-V CPU 72	ARM V7-M
AD9PAC74	RISC-V CPU 73	ARM V7-M
AD9PAC75	RISC-V CPU 74	ARM V7-M
AD9PAC76	RISC-V CPU 75	ARM V7-M
AD9PAC77	RISC-V CPU 76	ARM V7-M
AD9PAC78	RISC-V CPU 77	ARM V7-M
AD9PAC79	RISC-V CPU 78	ARM V7-M
AD9PAC80	RISC-V CPU 79	ARM V7-M
AD9PAC81	RISC-V CPU 80	ARM V7-M
AD9PAC82	RISC-V CPU 81	ARM V7-M
AD9PAC83	RISC-V CPU 82	ARM V7-M
AD9PAC84	RISC-V CPU 83	ARM V7-M
AD9PAC85	RISC-V CPU 84	ARM V7-M
AD9PAC86	RISC-V CPU 85	ARM V7-M
AD9PAC87	RISC-V CPU 86	ARM V7-M
AD9PAC88	RISC-V CPU 87	ARM V7-M
AD9PAC89	RISC-V CPU 88	ARM V7-M
AD9PAC90	RISC-V CPU 89	ARM V7-M
AD9PAC91	RISC-V CPU 90	ARM V7-M
AD9PAC92	RISC-V CPU 91	ARM V7-M
AD9PAC93	RISC-V CPU 92	ARM V7-M
AD9PAC94	RISC-V CPU 93	ARM V7-M
AD9PAC95	RISC-V CPU 94	ARM V7-M
AD9PAC96	RISC-V CPU 95	ARM V7-M
AD9PAC97	RISC-V CPU 96	ARM V7-M
AD9PAC98	RISC-V CPU 97	ARM V7-M
AD9PAC99	RISC-V CPU 98	ARM V7-M
AD9PAC100	RISC-V CPU 99	ARM V7-M

Auto Storage

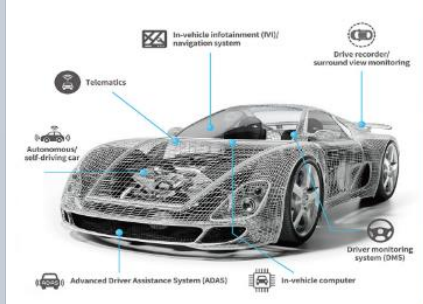



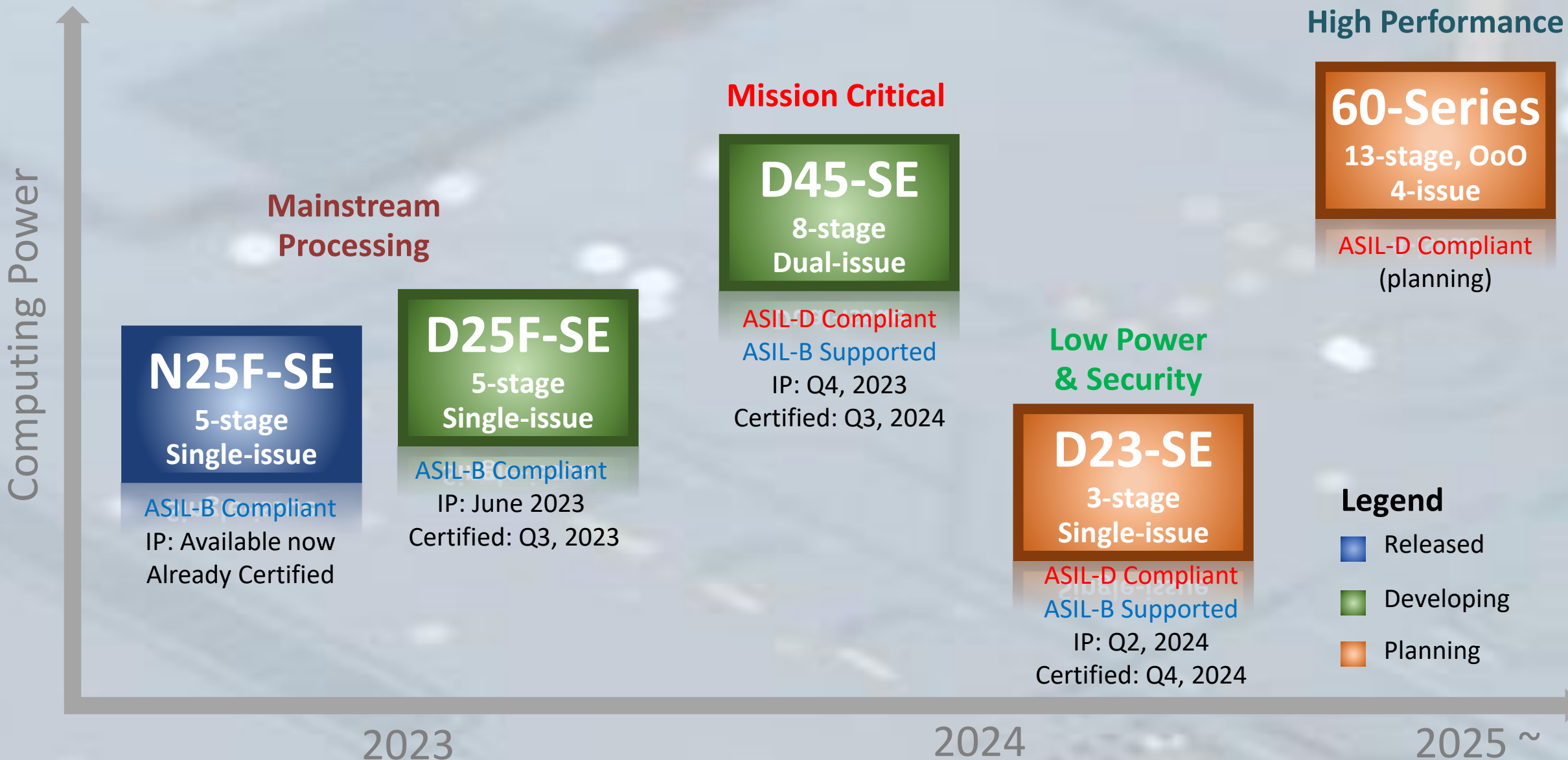





Diagram illustrating the integration of Auto Storage in automotive applications, showing its connection to various components like Telematics, In-vehicle entertainment (IVI)/navigation system, Drive recorder/surround view monitoring, Map, dashboard camera, In-vehicle computer, Driver monitoring system (DMS), and Advanced Driver Assistance System (ADAS).

AndesCore™ RISC-V Functional Safety Roadmap



N25F-SE, D25F-SE 5-Stage, ASIL-B Full Compliant

■ CPU Core

- 5-stage, in-order, single-issue architecture
- RISC-V RV32 GCB[P]* ISA, with Andes Extensions
 - D25F-SE with the RVP (SIMD/DSP) instruction extension
 - RVB bit-manipulation instructions for cryptography, ... applications
- AndeStar™ V5 32-bit architecture

■ Memory Subsystem

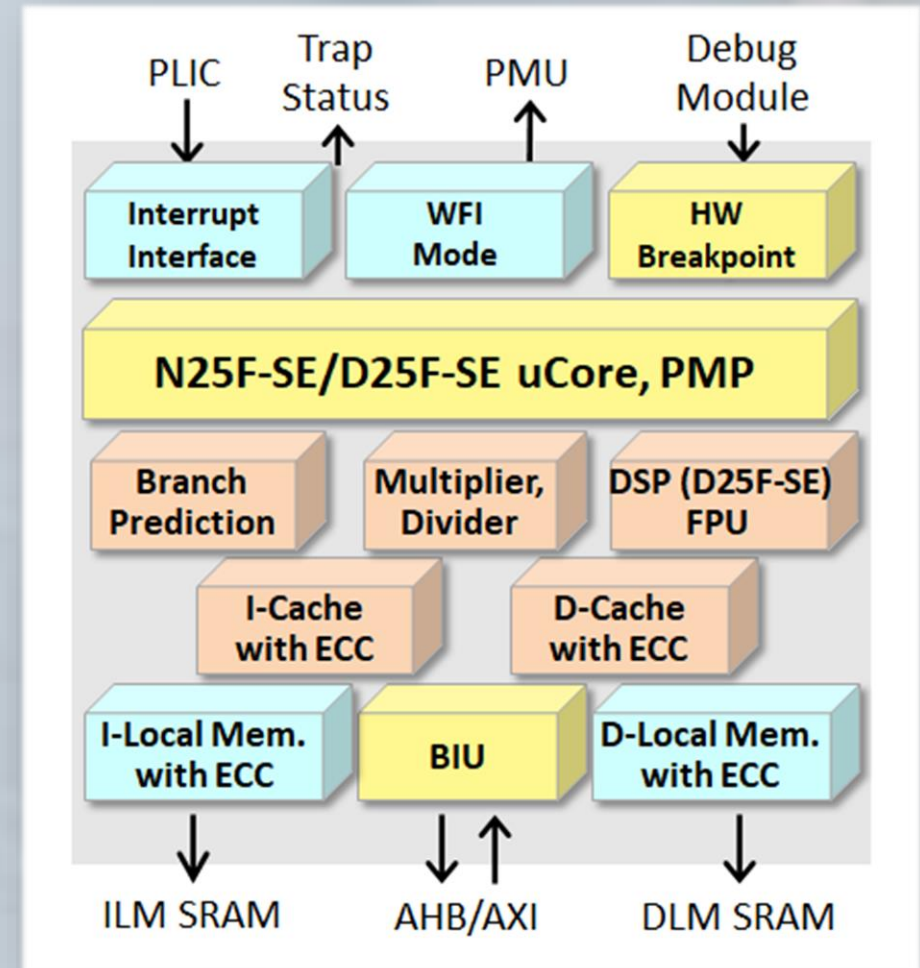
- Instruction and data caches, up to 32KB each
- Instruction and data local memories, up to 16MB each

■ Bus Interfaces and System Integration

- AXI or AHB bus master port
- Local memory direct access port

■ Functional Safety

- Core trap status bus interface,
- ECC protection, StackSafe™, PMP ...
- N25F-SE, ASIL-B certified. D25F-SE, ASIL-B certified at Q3/2023



AndesCore™ N25F-SE Certified by ISO 26262



SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID LICENSED TEST MARK Report No.

S280  S2800001

Tested according to **ISO 26262:2018 (Parts 2, 4 party, 5, 8, 9)**

Certified Product(s) CPU IP "N25F-SE"
Version: R320

Technical Data/Parameter The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance with **ASIL B** requirements.

Specific Requirements The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval. The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body for Functional Safety
SGS-TÜV Saar GmbH

Munich, October 28th, 2022


Marcus Rau

SGS-TÜV Saar GmbH, Wissensstr. 80,
D-61275 Wiesbaden, Deutschland / Germany.
WebSite: www.sgs-tuv-saar.com/en
E-Mail: tu@sgs.com

The validation status is documented via SGS Certification Database:

The test mark regulation is an integral part of this certificate.

CERTIFICATE

■ “The product has been approved in compliance with ASIL B requirements”

■ ISO 26262 Edition 2018, parts:

- ISO 26262-2:2018
- ISO 26262-4:2018*
- ISO 26262-5:2018
- ISO 26262-8:2018
- ISO 26262-9:2018

■ Certification Body

- SGS-TÜV Saar GmbH
- SGS-TÜV Saar GmbH accredited by German accreditation body DAkkS

* Part-4 System/item level integration, validation is not applicable to CPU IP

D45-SE 8-Stage, Dual-Issue, up to ASIL-D



■ CPU Core

- 8-stage, in-order, superscalar, dual-issue most instruction pairs
- RISC-V RV32 GCBP* support, Andes Extensions
- AndeStar™ V5 32-bit architecture

■ Memory Subsystem

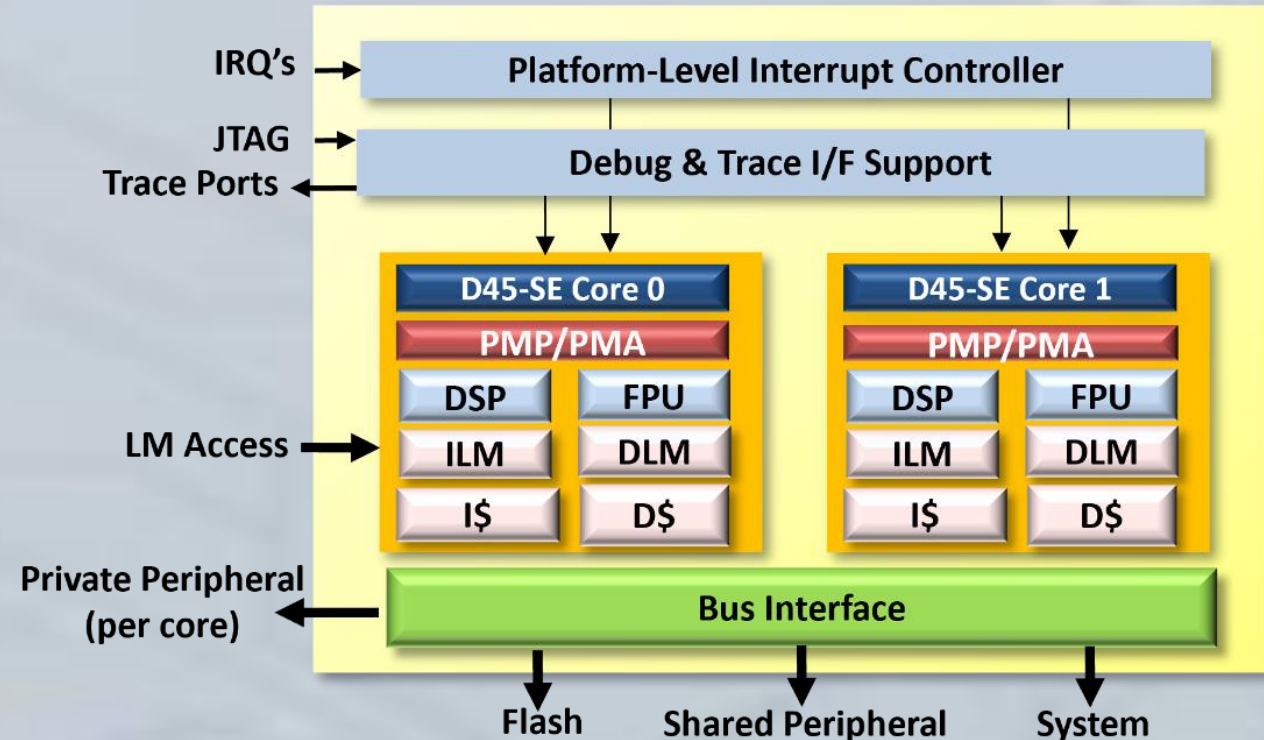
- Instruction and data cache, up to 64KB
- Instruction and data local memory, up to 16MB
- MemBoost

■ AXI Bus Interfaces

- System port, and flash port (64/128-bit)
- LM access port (64/128-bit)
- Private, and shared peripheral interface (64-bit)

■ Functional Safety

- Lockstep and Split mechanism
- Configurable ECC for every memory
- Core trap status bus interface
- Bus protection, StackSafe™
- Certified estimated by or before Q3/2024

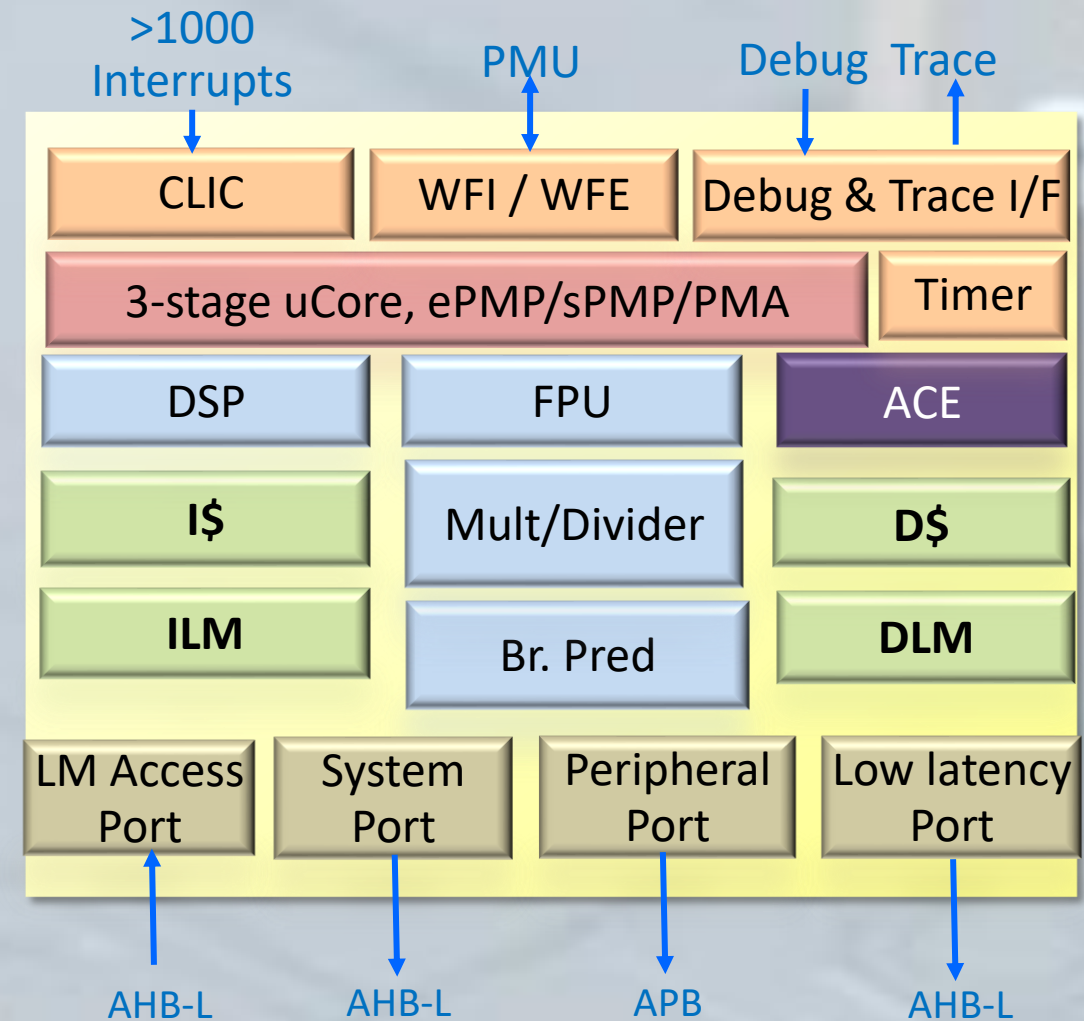


*P: draft

D23: Compact Controller for IoT/MCU/ECU



- 3-stage, limited dual-issue (optional)
- ISA extensions:
 - Base: RV32 I/E-MAC + B + Zce
 - Advanced: FD + P + K + CMO
- Privilege modes: M, S, U
- Configurable features
 - Branch prediction: none, static, dynamic
 - Multiplier options:
 - Sequential: 1/2/4/8-bit per cycle
 - Fast: pipelined
 - Andes Custom Extension™ (ACE)
 - Power management: WFI/WFE, PowerBrake
 - Core-Local Interrupt Controller (CLIC)
 - >1000 sources, 255 priority levels
 - Selective vectoring with priority preemption



D23: Compact Controller for IoT/MCU/ECU

■ Memory subsystem:

● Caches:

➤ Config:

- Icache only: ifetch
- RO-cache (Read-Only): ifetch and load
- I/D caches: ifetch, load and store

➤ Cache sizes: 1KB~32KB

➤ Error protection: ECC for I\$ and D\$

● I/D Local Memory (LM):

➤ 0~512MB with ECC

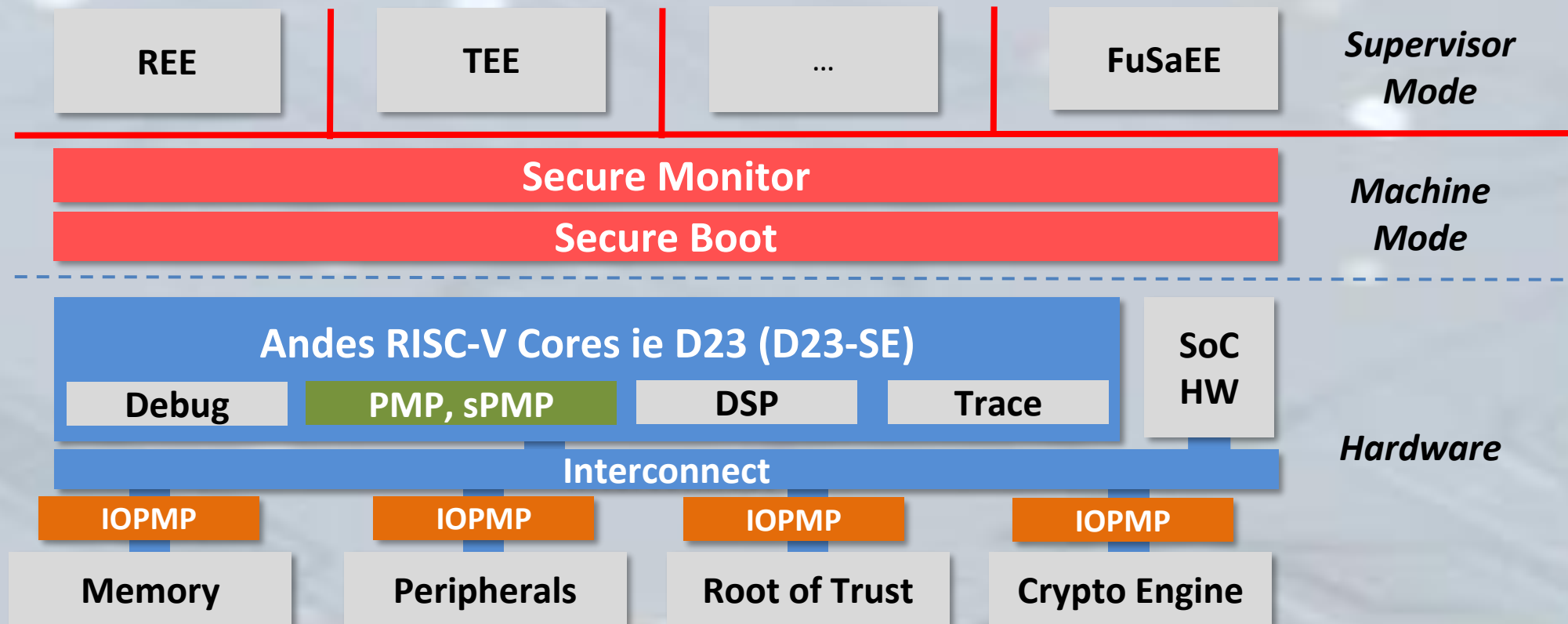
➤ Interface: SRAM or AHB-L

RISC-V Code Size Benchmarks							
ISA	IMAC	IMAC + V5 (N22)		IMABC + V5 (N25F)		IMABZce + V5 (D23)	
SPEC CPU	2,840	2,360	-16.9%	2,346	-17.4%	2,247	20.9%
CSiBE	1,462	1,204	-17.6%	1,190	-18.6%	1,144	21.8%
Audio Codec	842	682	-19.0%	671	-20.3%	656	22.1%
Embench-IoT	63.6	51.2	-19.5%	48.9	-23.1%	48.4	23.9%

■ D23-SE Safety-Enhanced D23 for Automotive designs, ASIL-D compliant & ASIL-B supported

Security System Architecture for D23 (D23-SE)

- Create multiple zones protection by PMP/sPMP
 - REEs (Rich Execution Environment)
 - TEEs (Trusted Execution Environment)
- IOPMP for IO protection



The Rise of

AndesAIRE™ AnDLA™ I350

The First Generation of Andes Deep Learning Accelerator

AndesAIRE™ NN SDK

Unleash the maximum AI/ML performance
and synergy of RISC-V CPU and AnDLA™

AndesAIRE™

Andes AI Runs Everywhere

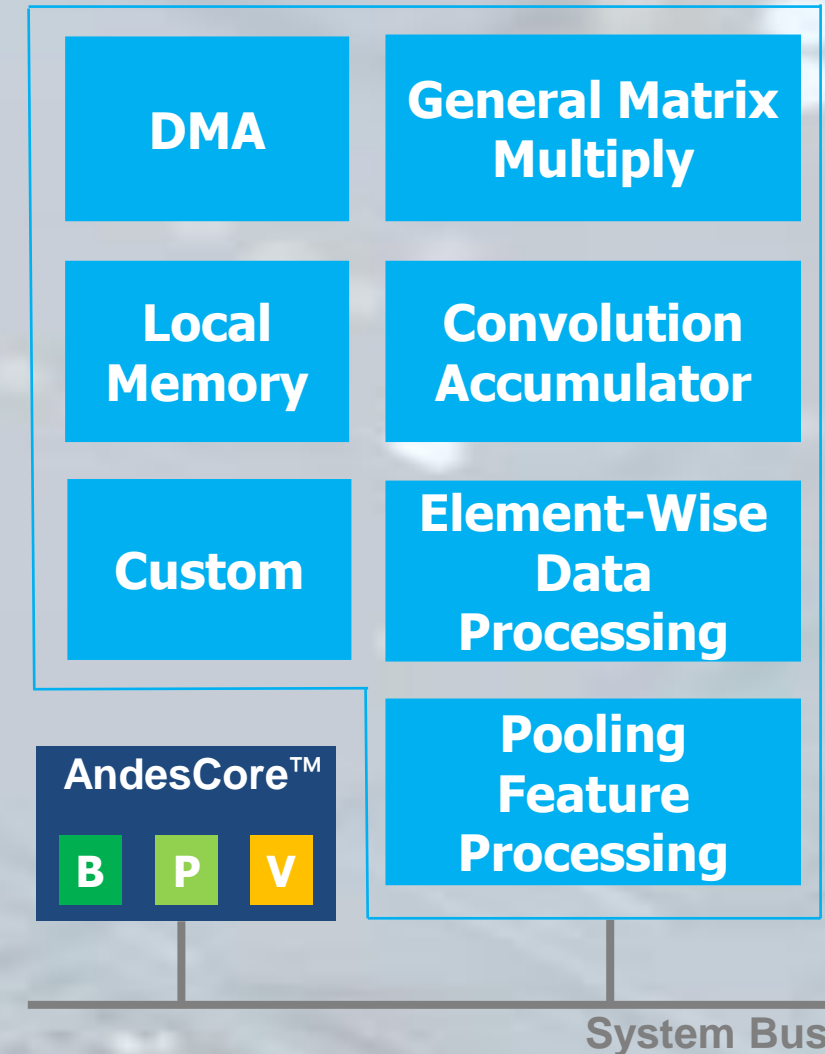


AndesAIRE™ AnDLA™ I350



- **Andes Deep Learning Accelerator (AnDLA™)**
 - High performance-efficient deep learning accelerator for edge and end-point inference
 - Scalable and multi-DLA
 - Cooperate with AndesCore™ full series (22/23/25/27/45/65)
- **Accelerating for most of NN Applications**
 - Image and video
 - Speech/voice and audio
- **Target performance**
 - Configurable MACs: 32 to 4096 (INT8)
 - Performance: 64 GOPS to 8 TOPS (INT8 @1GHz)
 - Configurable local memory: 16KB to 4MB
 - Leading power efficiency >5 TOPS/W (@28nm)
- **Integrated DMA and local memory**

AnDLA™ I350



Andes AI Total Solutions



NN models

AndeSight™ IDE

- GCC/LLVM Toolchains
- Build, debug, deploy, profile
- Analysis and tuning
- RTOS & Linux
- Device drivers
- Sample codes
- Simulator
- Documentation

AndesAIRE™ NN SDK

AndesAIRE™ NN Pilot™

Generated C code template

NN inference engines

TensorFlow Lite TensorFlow Lite tvm

AndesAIRE™ NN Library
AndeSoft™ Vector / DSP Library
AnDLA driver

Linux Host Processor
AX45MP(V), AX65

Compute Acceleration
Vector: 27V, 45V
DSP/SIMD: D25F, D45

Accelerator
AnDLA™ I350

Bus

AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera



Smart Sensor



Smart Home Appliance



AIoT / tinyML



Robotics



Wearable



Thank You

<http://www.andestech.com>

+886-3-5726533

