Andes Technology Corp.
Investor Conference Report
Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
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Company Overview

http://www.andestech.com
Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 400 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- EE Awards - “Taiwan-Product Award” & ”Asia-Company Award” (2021)
- Top 500 High-Growth Companies Asia-Pacific (2023)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning
Business Status Overview

- **300+ commercial licensees**
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - 600+ license agreements signed

- **AndeSight™ IDE:**
  - 25,000+ installations

- **Eco-system:**
  - 500+ partners

- **~13B Accumulative SoC Shipped**
Operation Results

http://www.andestech.com
2Q23 Revenue Analysis

YoY +27.8 %
QoQ -20.4 %

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>2Q22</th>
<th>1Q23</th>
<th>2Q23</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>140,138</td>
<td>225,096</td>
<td>179,158</td>
</tr>
</tbody>
</table>
1H23 Revenue Analysis

YoY
+15.1 %

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>H1 2022</th>
<th>H1 2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>351,167</td>
<td>404,254</td>
</tr>
</tbody>
</table>

YoY compared to H1 2022.
1H23 Top 10 Customers Analysis by Revenue

Top 10 Customer Contributed 72% Revenue

(NT$ thousands)
2Q23 Royalty Analysis

YoY -19.3 %
QoQ -9.2 %

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>2Q22</th>
<th>1Q23</th>
<th>2Q23</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>56,379</td>
<td>50,094</td>
<td>45,500</td>
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1H23 Royalty Analysis

YoY -18.6%

<table>
<thead>
<tr>
<th></th>
<th>NT$ thousands</th>
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<tbody>
<tr>
<td>H1 2022</td>
<td>117,367</td>
</tr>
<tr>
<td>H1 2023</td>
<td>95,594</td>
</tr>
</tbody>
</table>
1H23 Top 10 Royalty Contributors Analysis by Application

Top 10 Royalty Customers Contribution Analysis: 89%
1H23 Revenue Analysis by Payment Model

- License Fee: 56%
- Running Royalty: 24%
- Maintenance: 20%
- Others: 0%
1H23 Revenue Analysis by Region

- Taiwan: 46%
- USA: 34%
- China: 15%
- Korea: 4%
- Europe: 3%
- Japan: 3%

Chart shows distribution of revenue across different regions.
1H23 Revenue Analysis by Product
2Q23 Revenue Analysis - RISC-V

(NT$ thousands)

<table>
<thead>
<tr>
<th>Year</th>
<th>V3</th>
<th>RISC-V</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Q22</td>
<td>60,920</td>
<td>57%</td>
<td></td>
</tr>
<tr>
<td>1Q23</td>
<td>59,673</td>
<td>73%</td>
<td></td>
</tr>
<tr>
<td>2Q23</td>
<td>59,715</td>
<td>67%</td>
<td></td>
</tr>
</tbody>
</table>

Andes Technology

RISC-V
Historical Revenue Analysis

License

Royalty
1H23 Consolidated Gross Margin

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>H1 2022</th>
<th>H1 2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross Profit</td>
<td>350,742</td>
<td>403,057</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>99.88%</td>
<td>99.70%</td>
</tr>
</tbody>
</table>
2Q23 Consolidated Operating Expenses

YoY +48.3 %
QoQ +15.8 %

(NT$ thousands)

2Q22: 139,336
- R&D expenses: 53,611
- Administration expenses: 22,303
- Selling expenses: 63,107

1Q23: 166,611
- R&D expenses: 63,107
- Administration expenses: 46,018
- Selling expenses: 57,486

2Q23: 187,779
- R&D expenses: 84,469
- Administration expenses: 46,987
- Selling expenses: 56,323

R&D expenses
Administration expenses
Selling expenses
1H23 Consolidated Operating Expenses

YoY
+40.9%

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>H1 2022</th>
<th>H1 2023</th>
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</thead>
<tbody>
<tr>
<td>R&amp;D expenses</td>
<td>256,465</td>
<td>354,440</td>
</tr>
<tr>
<td>Administration expenses</td>
<td>120,913</td>
<td>93,005</td>
</tr>
<tr>
<td>Selling expenses</td>
<td>44,902</td>
<td>147,576</td>
</tr>
</tbody>
</table>

Diagram showing comparison of operating expenses between H1 2022 and H1 2023.
1H23 Consolidated Operating Income (Loss)

(NT$ thousands)

YoY - %

H1 2022: (71,538)
H1 2023: (191,964)
1H23 Consolidated Net Income

YoY
- %

(NT$ thousands)

196,317

H1 2022

H1 2023

(96,517)
1H23 Consolidated EPS

YoY
-5.79 $

3.88

H1 2022

(1.91)

H1 2023

(NT$)
Product Applications

http://www.andestech.com
Andes RISC-V Cores Adopted in SoC
Andes RISC-V Powering Rich Applications


Mobile
- Performance, code size
- N25F, N45

MPU/MCU/LoT
- D25F, D45, AX25MP, AX45MP

Cloud AI
- Accelerate, accelerate, accelerate
- N27V, AX25, AX27, AX45MP, AX45MPV

Space
- Secure, control, compute, communicate, position
- N25F

Storage
- Performance, bandwidth, real-time
- N25F, N45, AX45MP

5G Networks
- N25F, A25, A45MP, AX45MP
MTIA: Meta Training and Inference Accelerator

- Proc-A/B: Andes AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models

Figure 3: High-level architecture of the accelerator

Figure 4: PE’s internal organization

All photos: courtesy of ACM

Powered by Andes NX27V+ACE
New Products and Ecosystems

http://www.andestech.com
Andes RISC-V Product Roadmap

**RV32/RV64**

- **Cache-Coherent 1-4 Cores**
  - A25MP
  - AX25MP

- **Linux with FPU/DSP**
  - A25
  - AX25

- **Fast/Compact with FPU/DSP Automotive Grade**
  - N25F
  - D25F
  - NX25F
  - N25F-SE
  - D25F-SE
  - 5-stage (1.1 GHz)

**Vector Ext.**

- **27-Series**: Vector Ext. MemBoost
  - NX27V
  - A27/AX27
  - A27L2/AX27L2
  - and more.

**Superscalar**

- **45-Series**: Dual Issue Vector Ext. MemBoost
  - N45/NX45/D45
  - A45/AX45
  - A45MP/AX45MP
  - NX45V, AX45MPV
  - (1024-bit VPU, 1-8 Cores)
  - 5-stage (1.1 GHz)

- **60-Series**: > 2.5 GHz
  - > 2x per-GHz performance of 45-Series
  - AX65
  - 8-stage (1.2 GHz)

- **Out of Order**
  - 13-stage

**Leading positions:**
- The 1st company offering commercial RVP DSP CPU
- The 1st company offering the most updated spec of commercial RVV vector processor
- The 1st RISC-V core certified with ISO 26262 full compliance
- Tools for RISC-V custom extension: ACE
AndesCore™ AX65 OOO Application Processor

- 13-stage 4-way 64-bit OOO processor
- RVA22 profile
- Multicore cluster up to 8 cores
- 8 Execution Pipes: 4 ALU, 2 LD/ST, 2 FP
- 2-Level BTB with TAGE-L Branch Predictor
- Caches:
  - Private I/D caches: 64 KB, 4-way, 4-bank
  - Shared cache: up to 8 MB, 16-way
- 256-bit AXI4 for Memory, MMIO and IOCP
- Performance:
  - 2.4 GHz* @7nm without overdrive
  - Specint2006: 8.25/GHz
  - Specfp2006: 10.2/GHz

Best spec2k6 with 2-level caches
Roadmap for the AX60 Series

<table>
<thead>
<tr>
<th>Efficient</th>
<th>Mid-range</th>
<th>Extended</th>
</tr>
</thead>
<tbody>
<tr>
<td>AX60 Series: 13-stage OOO Linux MP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AX67
RVA24 and most performant

AX65
Multi-cluster

AX66
Balanced

AX63
Power-optimized
AX45MPV Multicore Cluster

At multicore cluster level:
- Up to 8 cores
- CM/L2$ subsystem
  - 128KB to 8MB, 64B line, 16-way
  - Multi-cycle support for high-density SRAMs
  - I/D prefetch, up to 64 outstanding requests
- AXI Bus Interfaces up to 512 bits

Scalar Unit: RV64GCBP
- 8-stage In-order dual-issue
- MMU/SV48, M/S/U modes
- I/D caches: 8K~64KB; Parity (I$) or ECC (both)

RISC-V Vector Extension (RVV v1.0)
- data format: int8~64, fp16~64; int4, bf16
- VLEN/DLEN: 128~1024 bits, 1:1 or 2:1 ratio
- Up to 6 DLEN results per cycle
**AX45MPV: 1024-bit Vector Processor**

- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, bf16
  - VLEN/DLEN: 128~\textbf{1024} bits, 1:1 or 2:1 ratio
  - Up to 6 DLEN results per cycle

- **Efficient support needed for tight coupling with HWE**
  1. Data exchange performance (from/to shared memory in HWE)
  2. Efficient control to the HWE

- **2 solutions offered in AX45MPV:**
  - Andes Streaming Port™ (ASP) thru ACE
    - Data bus: data transfer btw VR and HWE
    - Command bus: to control/synchronize HWE operations
  - HVM: High-speed Vector Memory
    - CPU side: DLEN-wide load/store interface with dynamic wait cycles
    - HVM module: accepting multiple accesses to multi-bank SRAM’s
Andes is Driving Innovations in Automotive

with Industry’s 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar

Auto TDDI

Auto MCU

Auto Storage

Subject to change without notice

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Taking RISC-V® Mainstream
AndesCore™ RISC-V Functional Safety Roadmap

**Mainstream Processing**

- **N25F-SE**
  - 5-stage Single-issue
  - ASIL-B Compliant
  - IP: Available now Already Certified

- **D25F-SE**
  - 5-stage Single-issue
  - ASIL-B Compliant
  - IP: June 2023
  - Certified: Q3, 2023

**Mission Critical**

- **D45-SE**
  - 8-stage Dual-issue
  - ASIL-D Compliant
  - ASIL-B Supported
  - IP: Q4, 2023
  - Certified: Q3, 2024

**Low Power & Security**

- **D23-SE**
  - 3-stage Single-issue
  - ASIL-D Compliant
  - ASIL-B Supported
  - IP: Q2, 2024
  - Certified: Q4, 2024

**High Performance**

- **60-Series**
  - 13-stage, OoO 4-issue
  - ASIL-D Compliant (planning)

**Legend**

- Released
- Developing
- Planning

2023

2024

2025 ~'

Taking RISC-V® Mainstream
N25F-SE, D25F-SE 5-Stage, ASIL-B Full Compliant

- **CPU Core**
  - 5-stage, in-order, single-issue architecture
  - RISC-V RV32 GCB[P]* ISA, with Andes Extensions
    - D25F-SE with the RVP (SIMD/DSP) instruction extension
    - RVB bit-manipulation instructions for cryptography, … applications
  - AndeStar™ V5 32-bit architecture

- **Memory Subsystem**
  - Instruction and data caches, up to 32KB each
  - Instruction and data local memories, up to 16MB each

- **Bus Interfaces and System Integration**
  - AXI or AHB bus master port
  - Local memory direct access port

- **Functional Safety**
  - Core trap status bus interface,
  - ECC protection, StackSafe™, PMP …
AndesCore™ N25F-SE Certified by ISO 26262

- “The product has been approved in compliance with ASIL B requirements”
- ISO 26262 Edition 2018, parts:
  - ISO 26262-2:2018
  - ISO 26262-4:2018*
  - ISO 26262-5:2018
  - ISO 26262-8:2018
  - ISO 26262-9:2018
- Certification Body
  - SGS-TÜV Saar GmbH
  - SGS-TÜV Saar GmbH accredited by German accreditation body DAkkS

* Part-4 System/item level integration, validation is not applicable to CPU IP
D45-SE 8-Stage, Dual-Issue, up to ASIL-D

■ CPU Core
  ● 8-stage, in-order, superscalar, dual-issue most instruction pairs
  ● RISC-V RV32 GCBP* support, Andes Extensions
  ● AndeStar™ V5 32-bit architecture

■ Memory Subsystem
  ● Instruction and data cache, up to 64KB
  ● Instruction and data local memory, up to 16MB
  ● MemBoost

■ AXI Bus Interfaces
  ● System port, and flash port (64/128-bit)
  ● LM access port (64/128-bit)
  ● Private, and shared peripheral interface (64-bit)

■ Functional Safety
  ● Lockstep and Split mechanism
  ● Configurable ECC for every memory
  ● Core trap status bus interface
  ● Bus protection, StackSafe™
  ● Certified estimated by or before Q3/2024

*P: draft
D23: Compact Controller for IoT/MCU/ECU

- 3-stage, limited dual-issue (optional)
- ISA extensions:
  - Base: RV32 I/E-MAC + B + Zce
  - Advanced: FD + P + K + CMO
- Privilege modes: M, S, U
- Configurable features
  - Branch prediction: none, static, dynamic
  - Multiplier options:
    - Sequential: 1/2/4/8-bit per cycle
    - Fast: pipelined
  - Andes Custom Extension™ (ACE)
  - Power management: WFI/WFE, PowerBrake
  - Core-Local Interrupt Controller (CLIC)
    - >1000 sources, 255 priority levels
    - Selective vectoring with priority preemption
D23: Compact Controller for IoT/MCU/ECU

- **Memory subsystem:**
  - **Caches:**
    - **Config:**
      - Icache only: ifetch
      - RO-cache (Read-Only): ifetch and load
      - I/D caches: ifetch, load and store
    - Cache sizes: 1KB~32KB
    - Error protection: ECC for I$ and D$
  - **I/D Local Memory (LM):**
    - 0~512MB with ECC
    - Interface: SRAM or AHB-L

- **D23-SE Safety-Enhanced D23** for Automotive designs, ASIL-D compliant & ASIL-B supported

<table>
<thead>
<tr>
<th>RISC-V Code Size Benchmarks</th>
<th>ISA</th>
<th>IMAC</th>
<th>IMAC + V5 (N22)</th>
<th>IMABC + V5 (N25F)</th>
<th>IMABZce + V5 (D23)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SPEC CPU</strong></td>
<td>2,840</td>
<td>2,360</td>
<td>-16.9%</td>
<td>2,346</td>
<td>-17.4%</td>
</tr>
<tr>
<td><strong>CSiBE</strong></td>
<td>1,462</td>
<td>1,204</td>
<td>-17.6%</td>
<td>1,190</td>
<td>-18.6%</td>
</tr>
<tr>
<td><strong>Audio Codec</strong></td>
<td>842</td>
<td>682</td>
<td>-19.0%</td>
<td>671</td>
<td>-20.3%</td>
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<tr>
<td><strong>Embench-IoT</strong></td>
<td>63.6</td>
<td>51.2</td>
<td>-19.5%</td>
<td>48.9</td>
<td>-23.1%</td>
</tr>
</tbody>
</table>
Security System Architecture for D23 (D23-SE)

- Create multiple zones protection by PMP/sPMP
  - REEs (Rich Execution Environment)
  - TEEs (Trusted Execution Environment)
- IOPMP for IO protection
The Rise of

AndesAIRE™ AnDLA™ I350
The First Generation of Andes Deep Learning Accelerator

AndesAIRE™ NN SDK
Unleash the maximum AI/ML performance and synergy of RISC-V CPU and AnDLA™
AndesAIRE™ AnDLA™ I350

- Andes Deep Learning Accelerator (AnDLA™)
  - High performance-efficient deep learning accelerator for edge and end-point inference
  - Scalable and multi-DLA
  - Cooperate with AndesCore™ full series (22/23/25/27/45/65)
- Accelerating for most of NN Applications
  - Image and video
  - Speech/voice and audio
- Target performance
  - Configurable MACs: 32 to 4096 (INT8)
  - Performance: 64 GOPS to 8 TOPS (INT8 @1GHz)
  - Configurable local memory: 16KB to 4MB
  - Leading power efficiency >5 TOPS/W (@28nm)
- Integrated DMA and local memory
Andes AI Total Solutions

**AndesSight™ IDE**
- GCC/LLVM Toolchains
- Build, debug, deploy, profile
- Analysis and tuning
- RTOS & Linux
- Device drivers
- Sample codes
- Simulator
- Documentation

**AndesAIRE™ NN SDK**
- **AndesAIRE™ NN Pilot™**
  - Generated C code template
- **NN inference engines**
  - TensorFlow
  - TensorFlow Lite
  - TVM

**AndesAIRE™ NN Library**
- AndeSoft™ Vector / DSP Library
- AnDLA™ driver

**Linux Host Processor**
- AX45MP(V), AX65

**Compute Acceleration**
- Vector: 27V, 45V
- DSP/SIMD: D25F, D45

**Accelerator**
- AnDLA™ I350

Bus

Taking RISC-V® Mainstream
Andesaire™ - Andes AI Runs Everywhere

Smart Camera

Smart Sensor

Smart Home Appliance

AIoT / tinyML

Robotics

Wearable

Taking RISC-V® Mainstream
Thank You

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