晶心科技股份有限公司

ANDES TECHNOLOGY

投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

公司簡介

http://www.andestech.com

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數超過400人；80%為工程師。
- 獲得TSMC 2015年新的 IP OIP Award 。
- 晉升為RISC-V國際聯盟(前身為RISC-V基金會) 首席會員。 (2020)
- 獲得AI Global Media頒發「2020年最傑出嵌入式處理器IP供應商」。
- EE Awards亞洲金選獎 -「Taiwan 產品獎」,「Asia 企業獎」(2021)
- 2023亞太區 前五百大高成長企業

晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

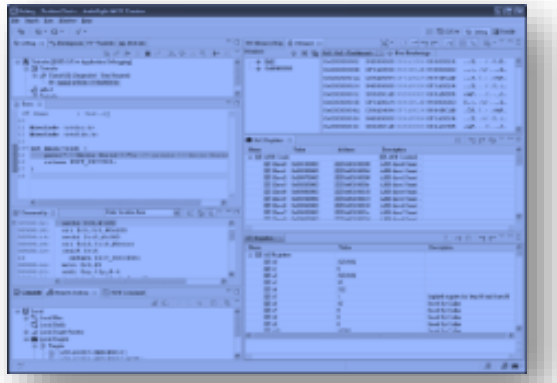
晶心利基

- 智能及環保之電子設備
- 雲端應用,人工智慧及物聯網

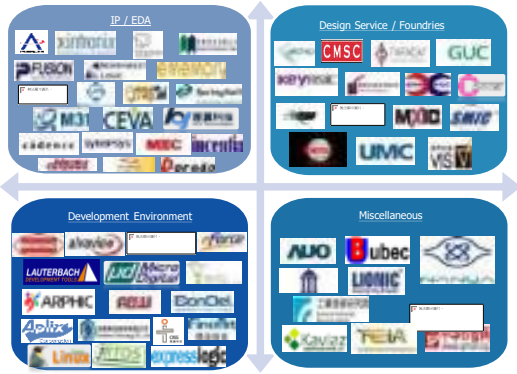
重要里程碑

- **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed

- AndeSight™ IDE:
  - **25,000+** installations



- Eco-system:
  - **500+** partners



- **>13B** Accumulative SoC Shipped

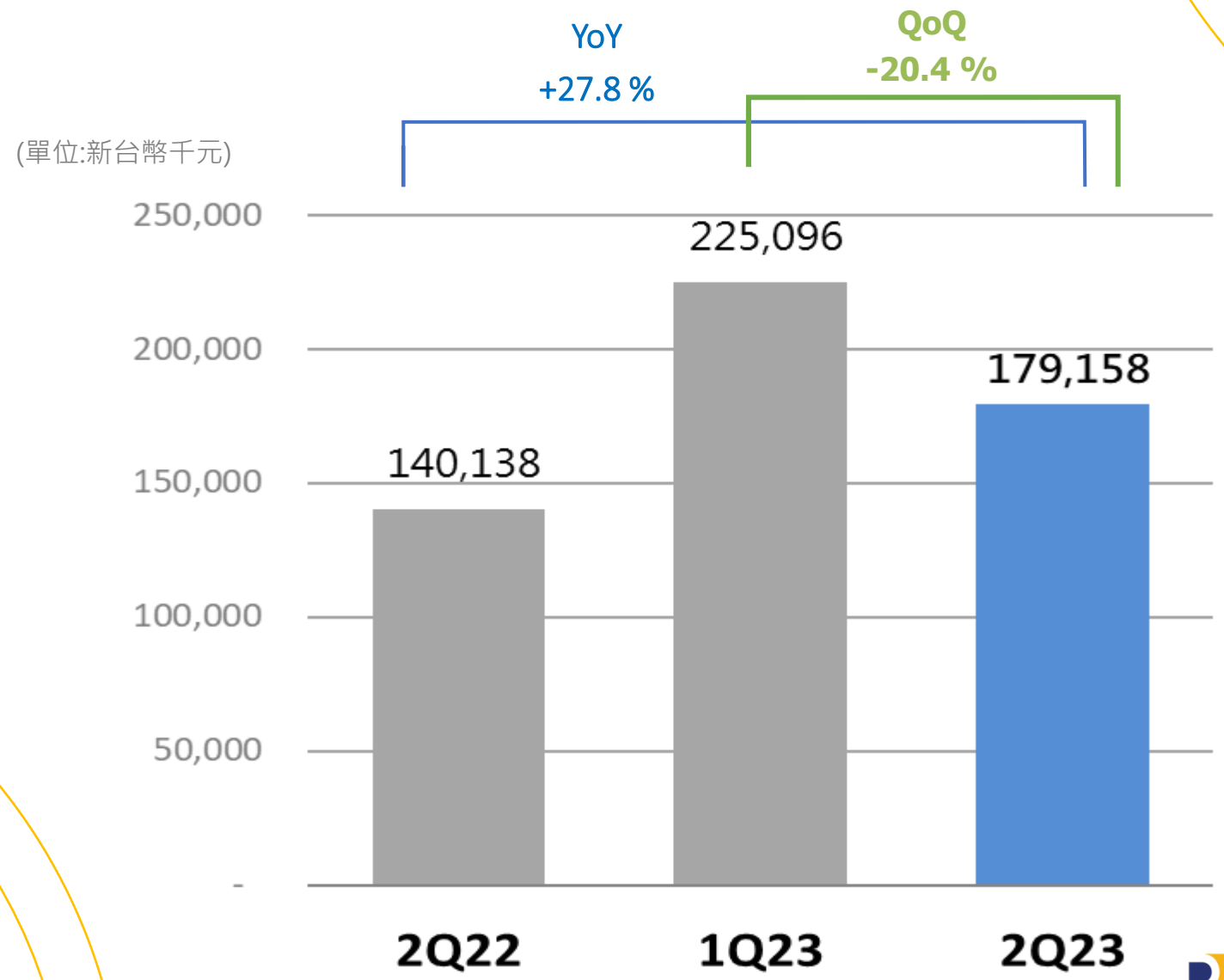
ANDES TECHNOLOGY

RISC-V®

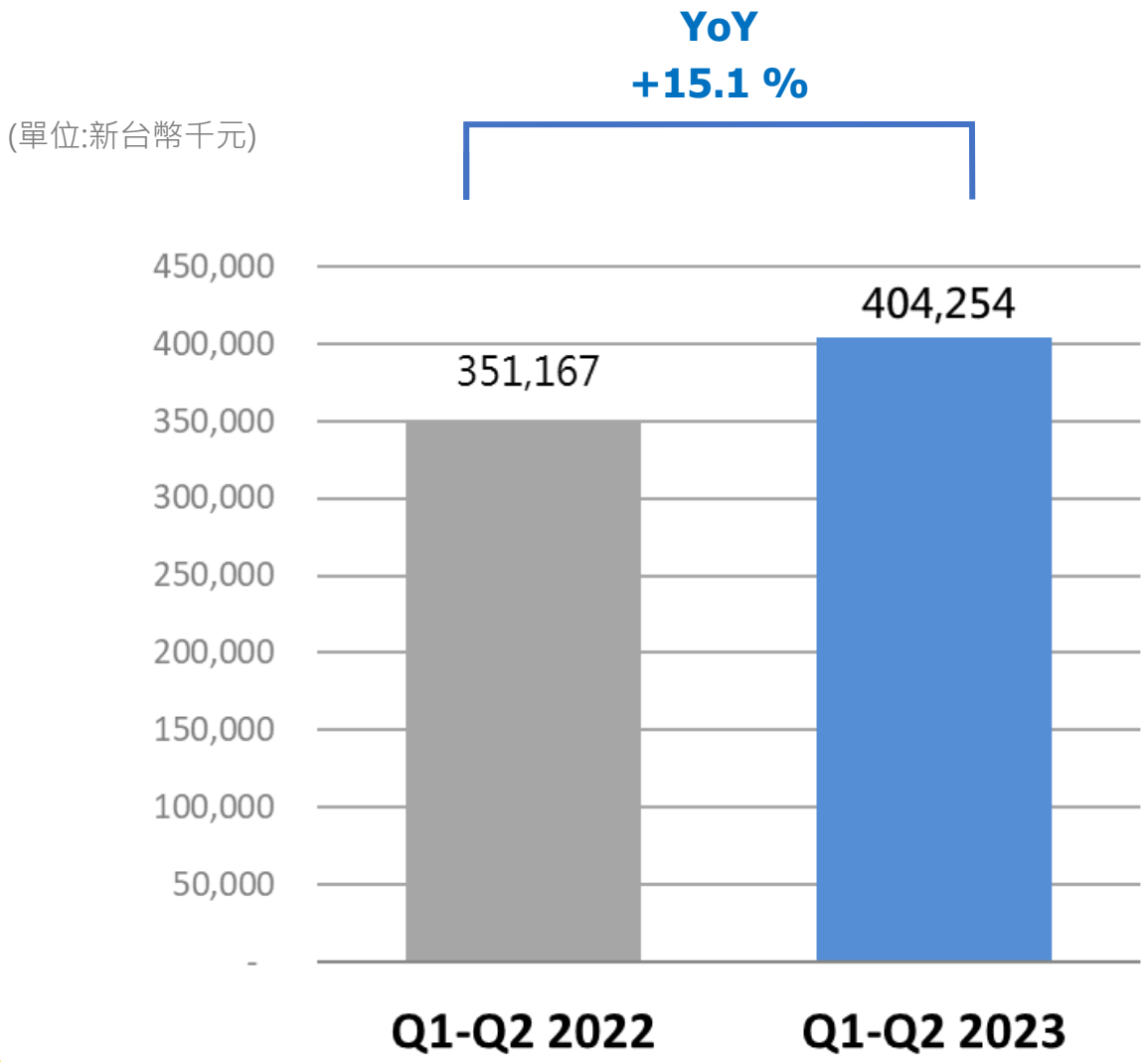
營運成果

http://www.andestech.com

2023年第二季營業收入

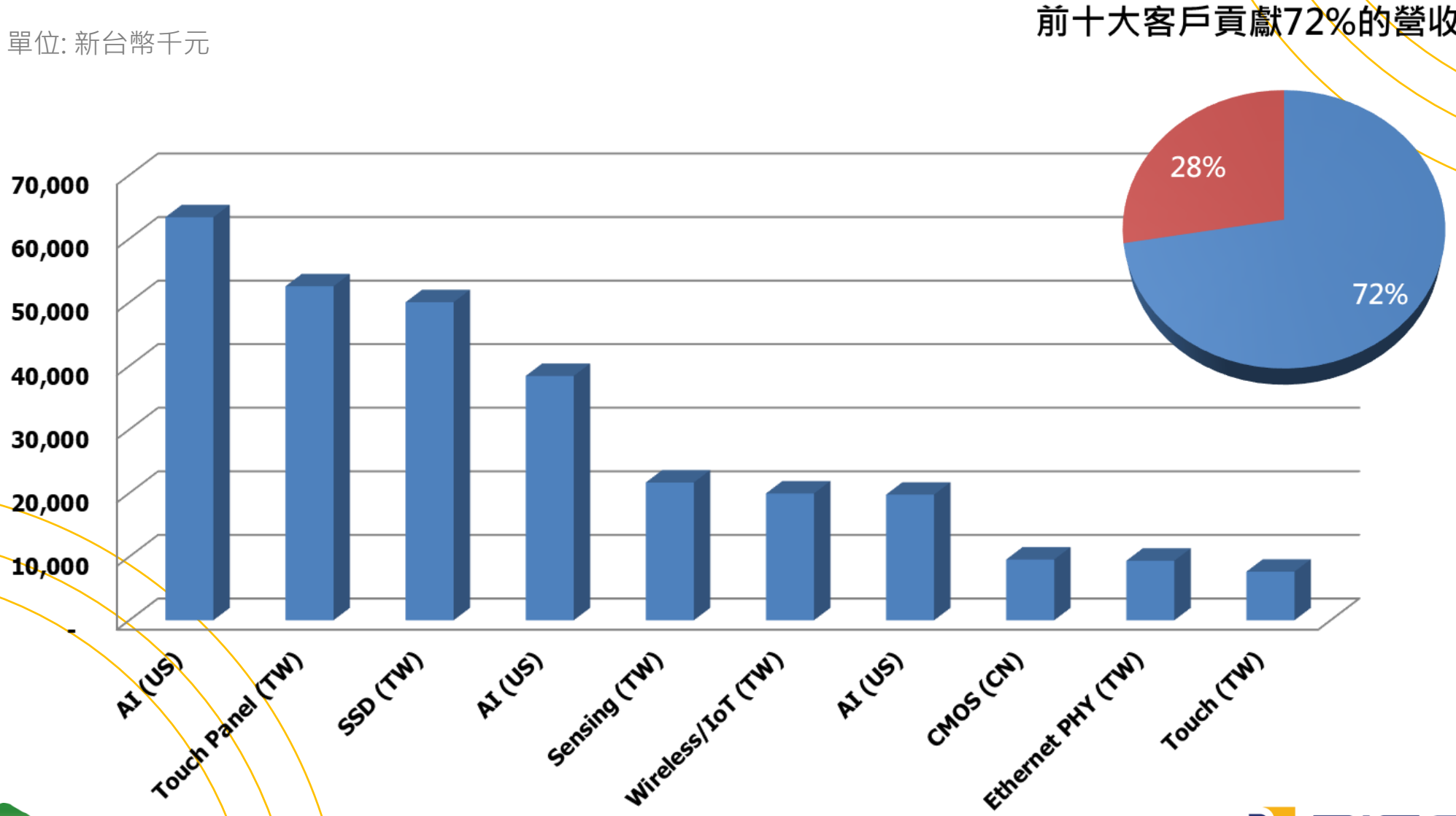


2023年上半年度營業收入

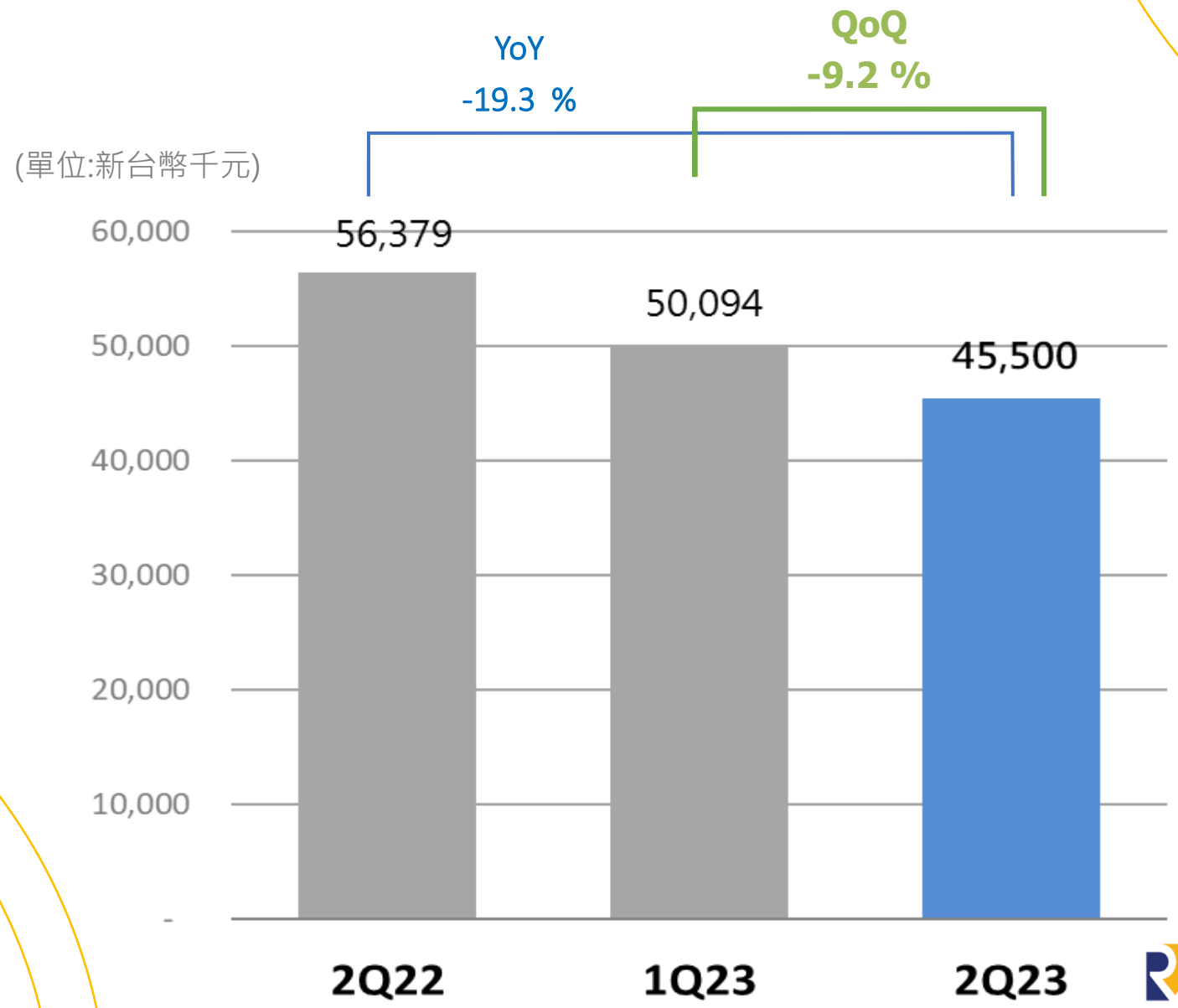


2023年上半年度前十大客戶之應用分析

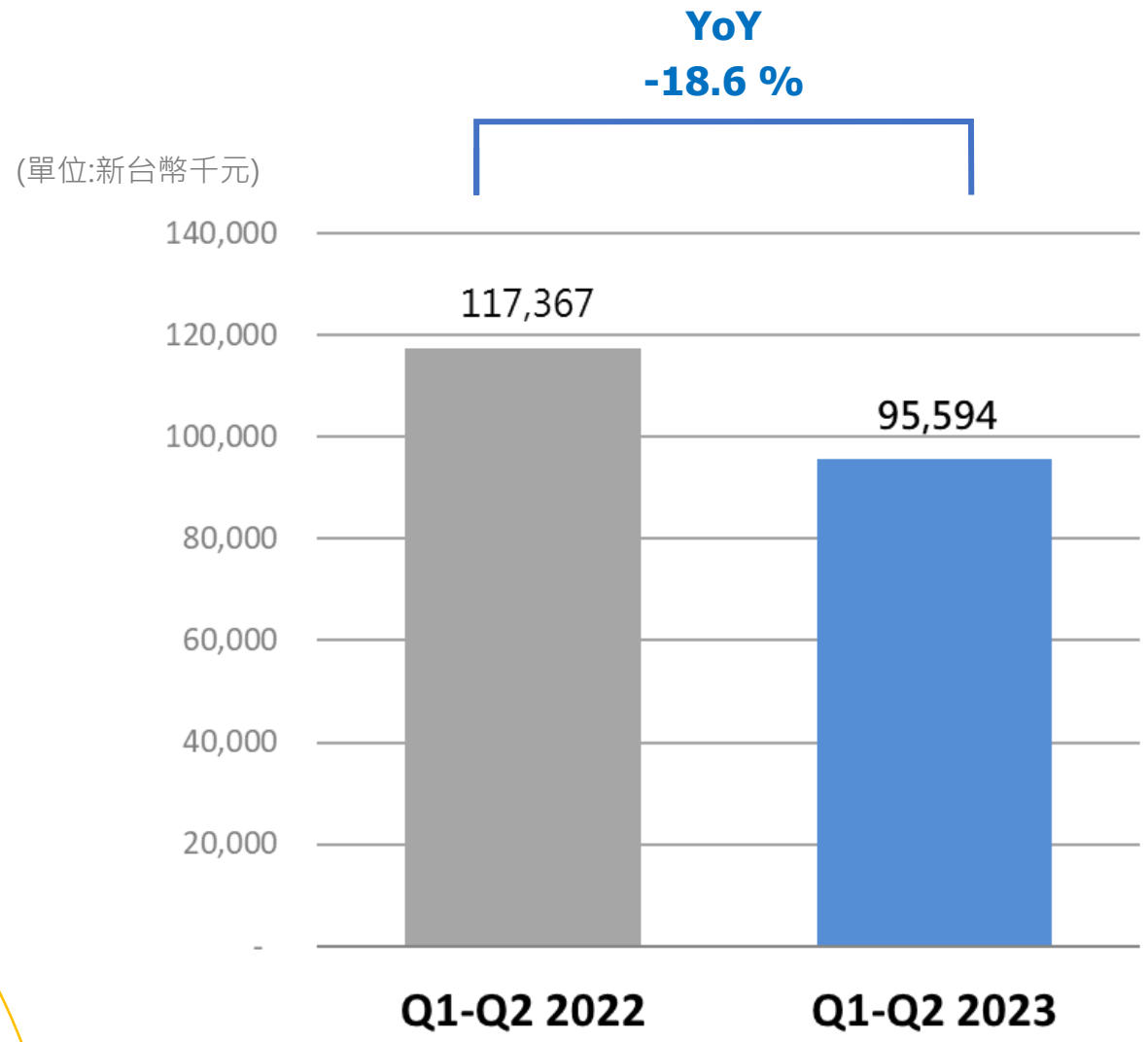
單位: 新台幣千元



2023年第二季權利金收入

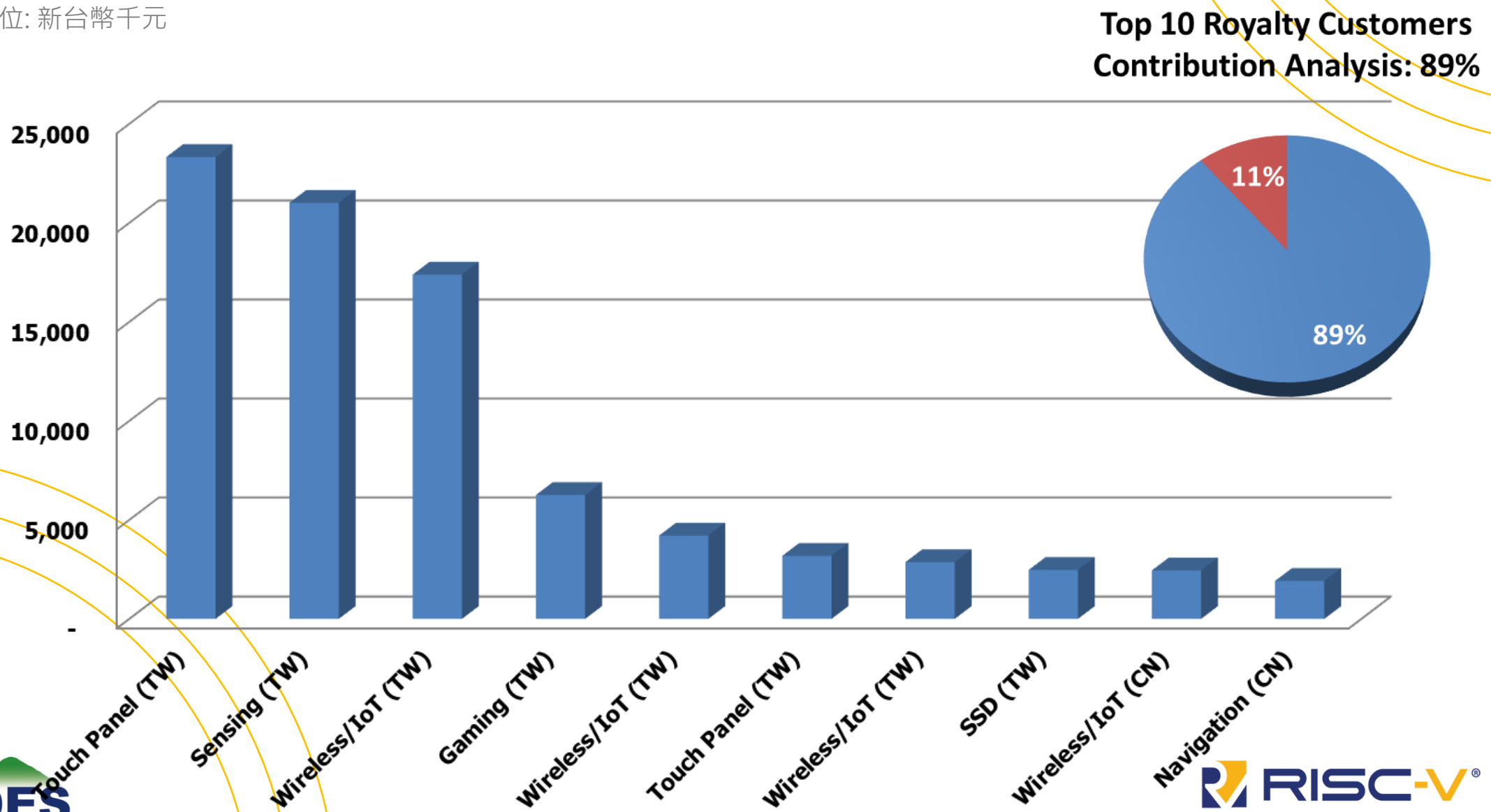


2023年上半年度權利金收入

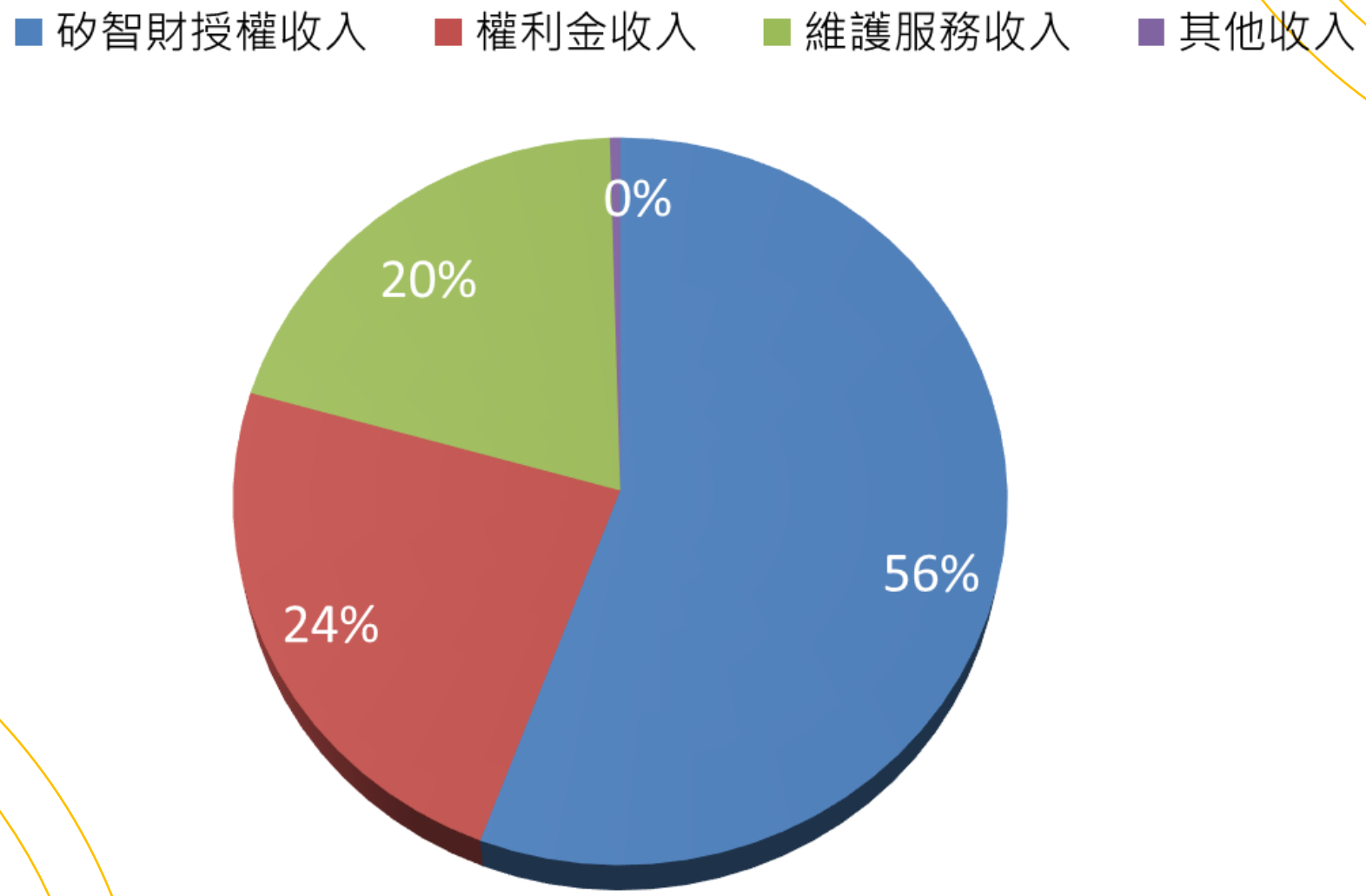


2023年上半年度 權利金應用分析

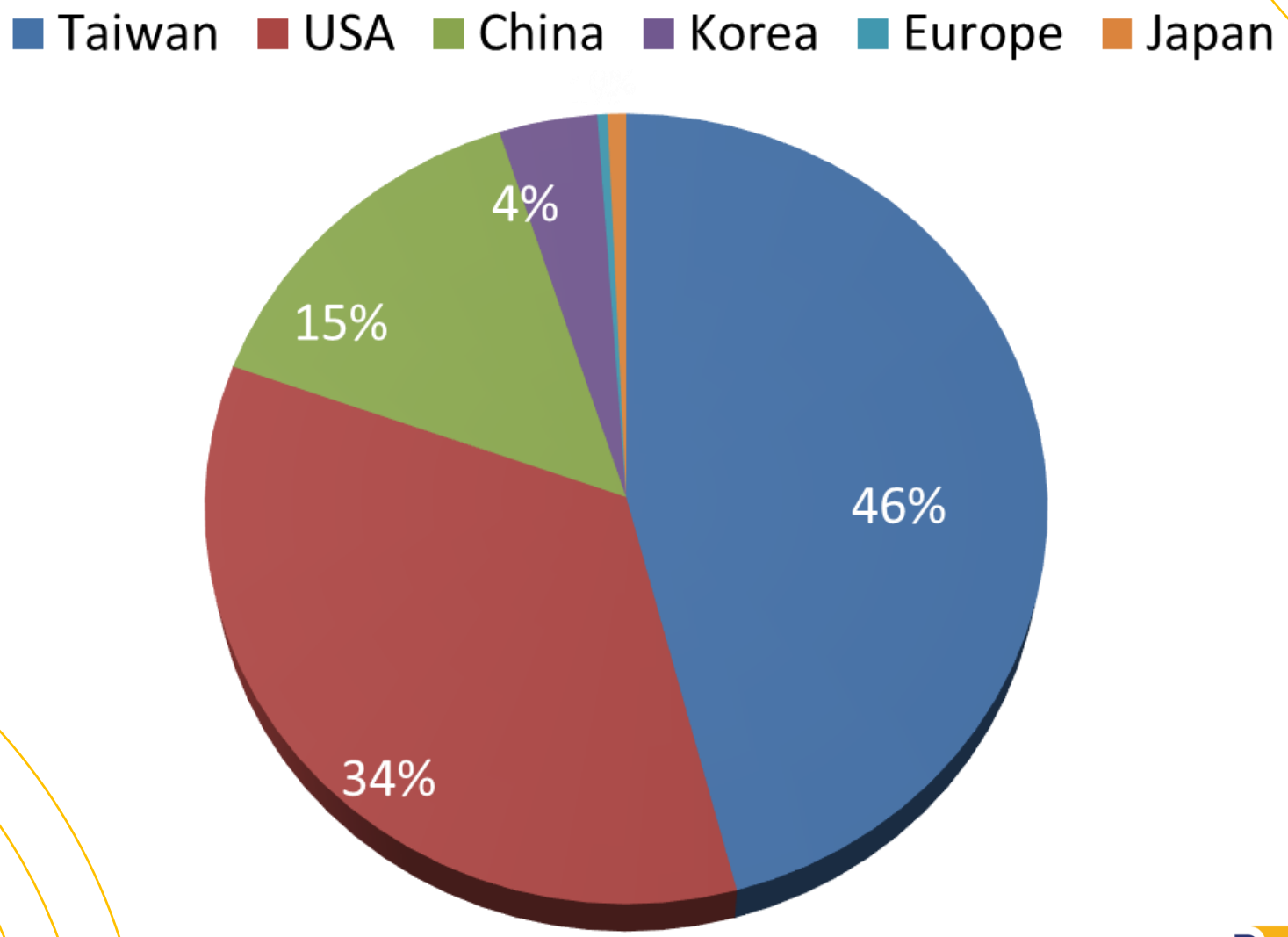
單位: 新台幣千元



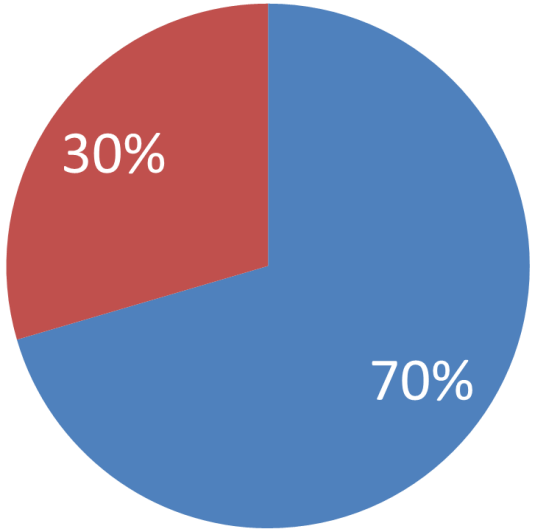
2023年上半年度 銷售分析-收入模式



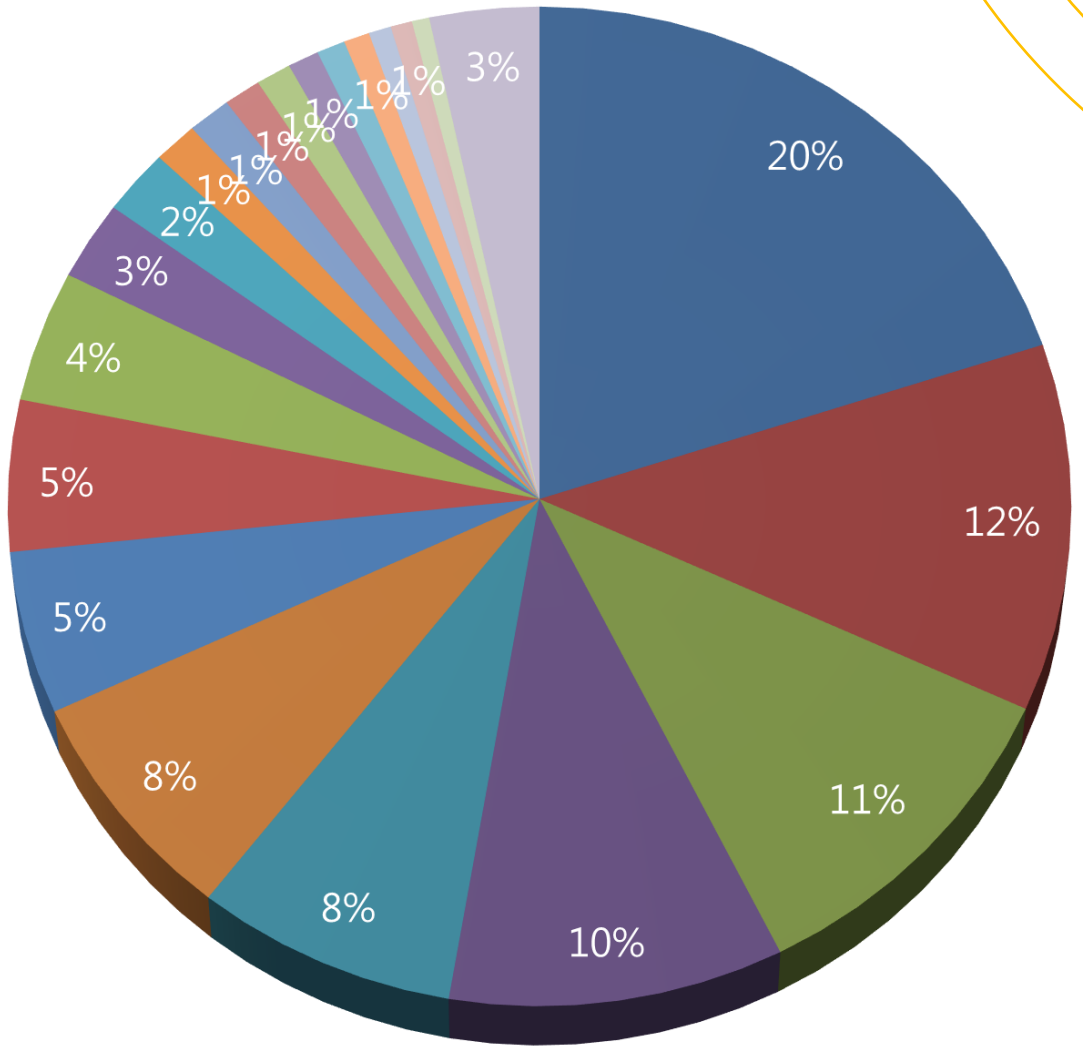
2023年上半年度 銷售分析-地區別



2023年上半年度 銷售分析-產品別



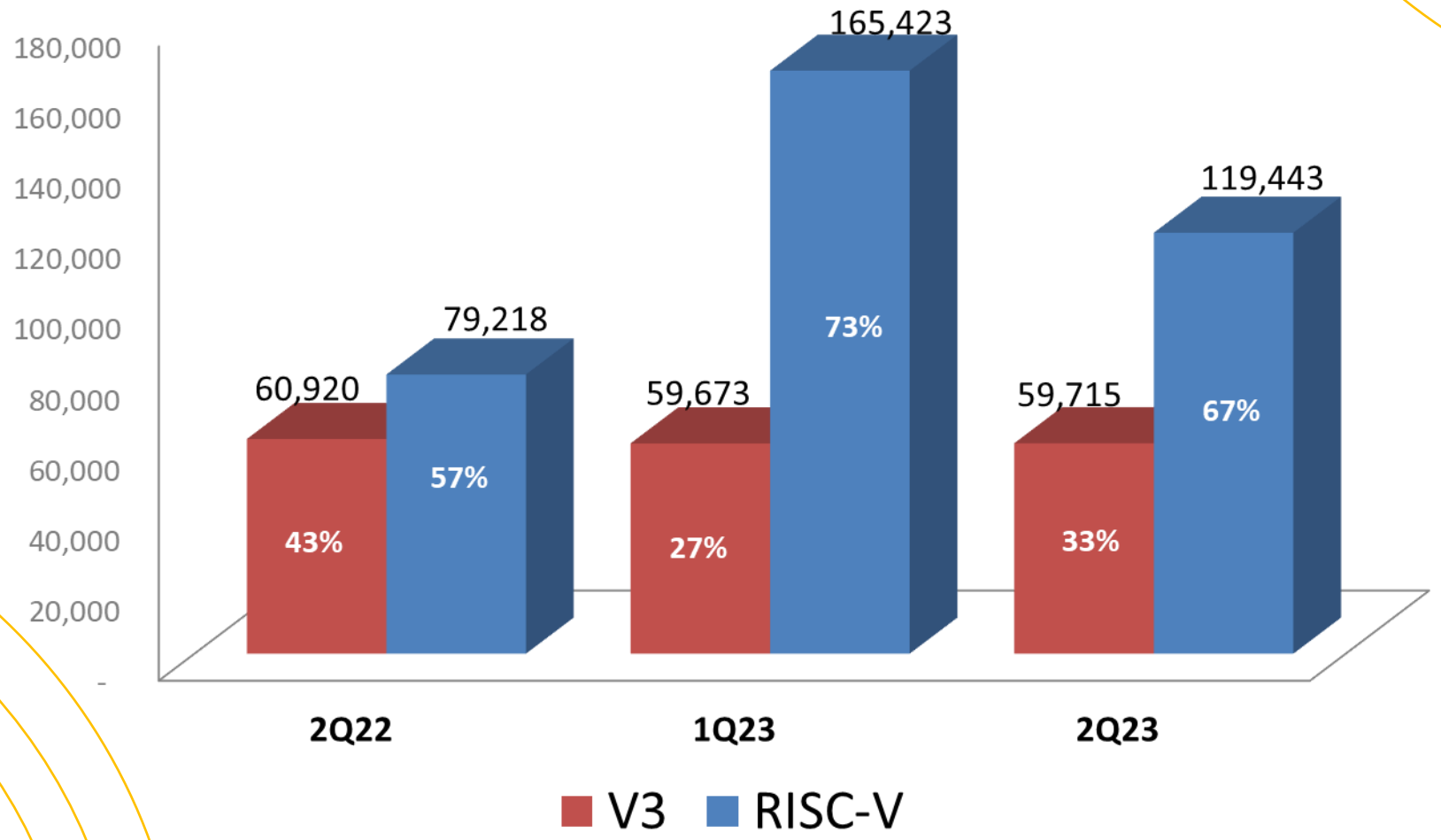
RISC-V
V3



N25
N8
AX45
NX45
ACE
N9
N10
N45
NX27
NX25
N13
N22
A45
E8
LLVM
D25
D10
AE250
Customized IP
N7
A27
OTHERS

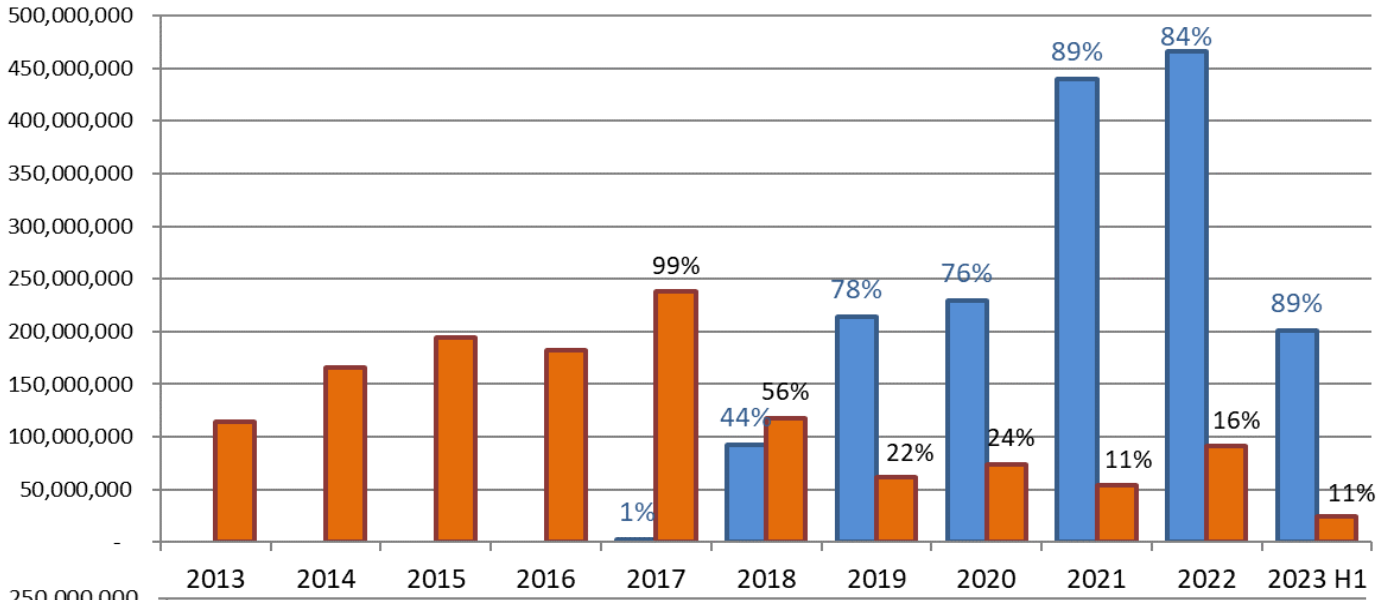
2023年第二季銷售分析- RISC-V

(單位:新台幣千元)

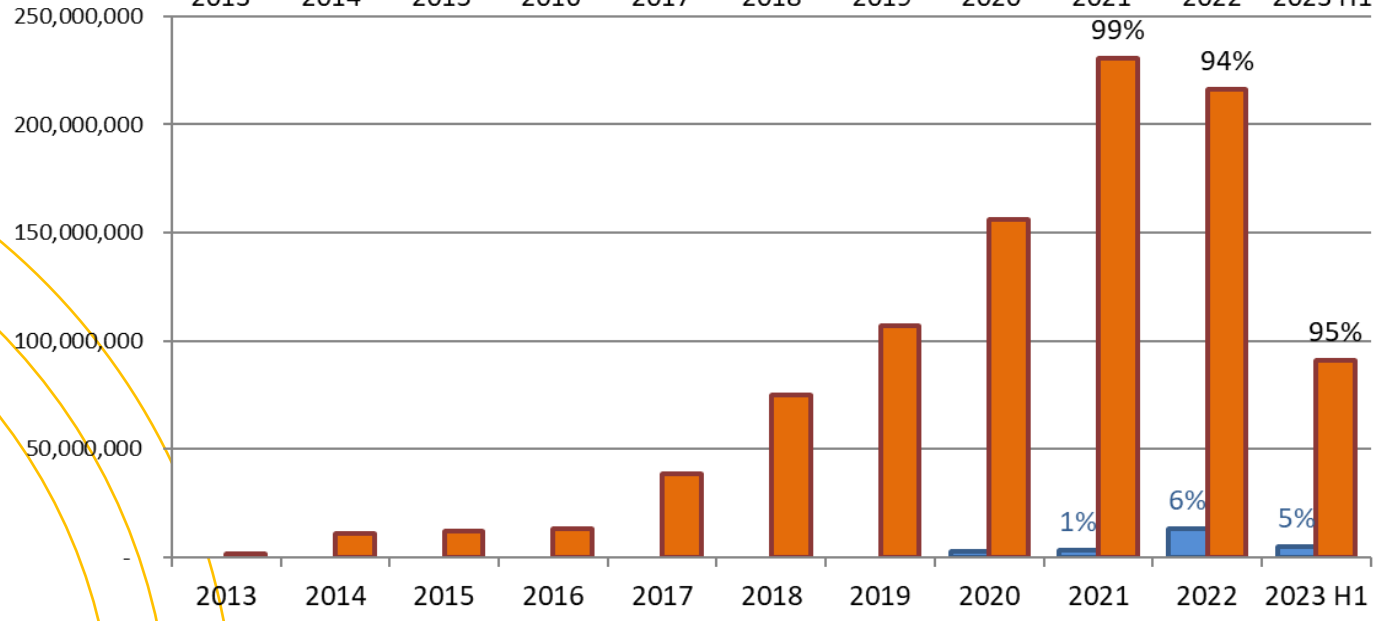


歷年收入分析

(NT$)



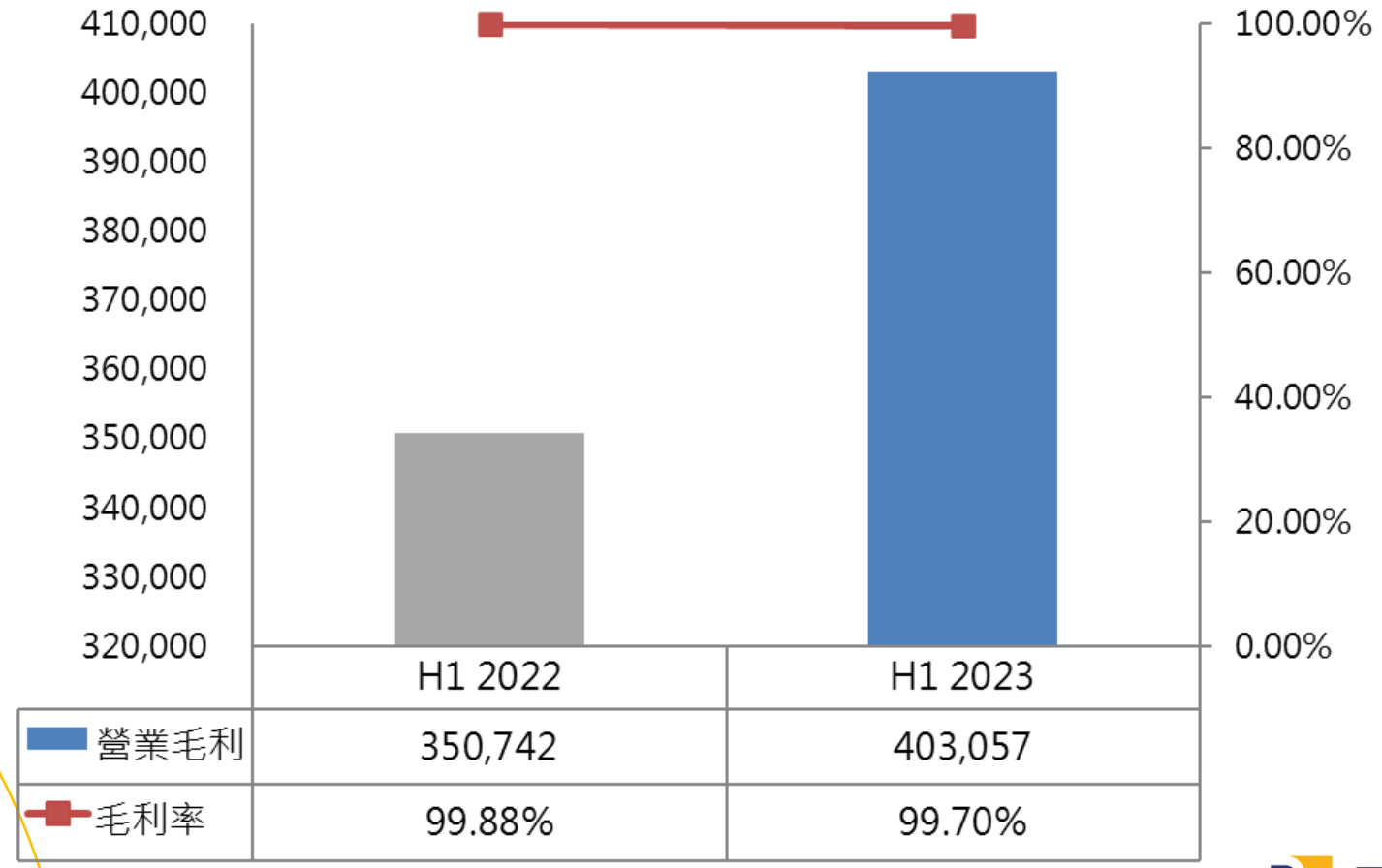
License



Royalty

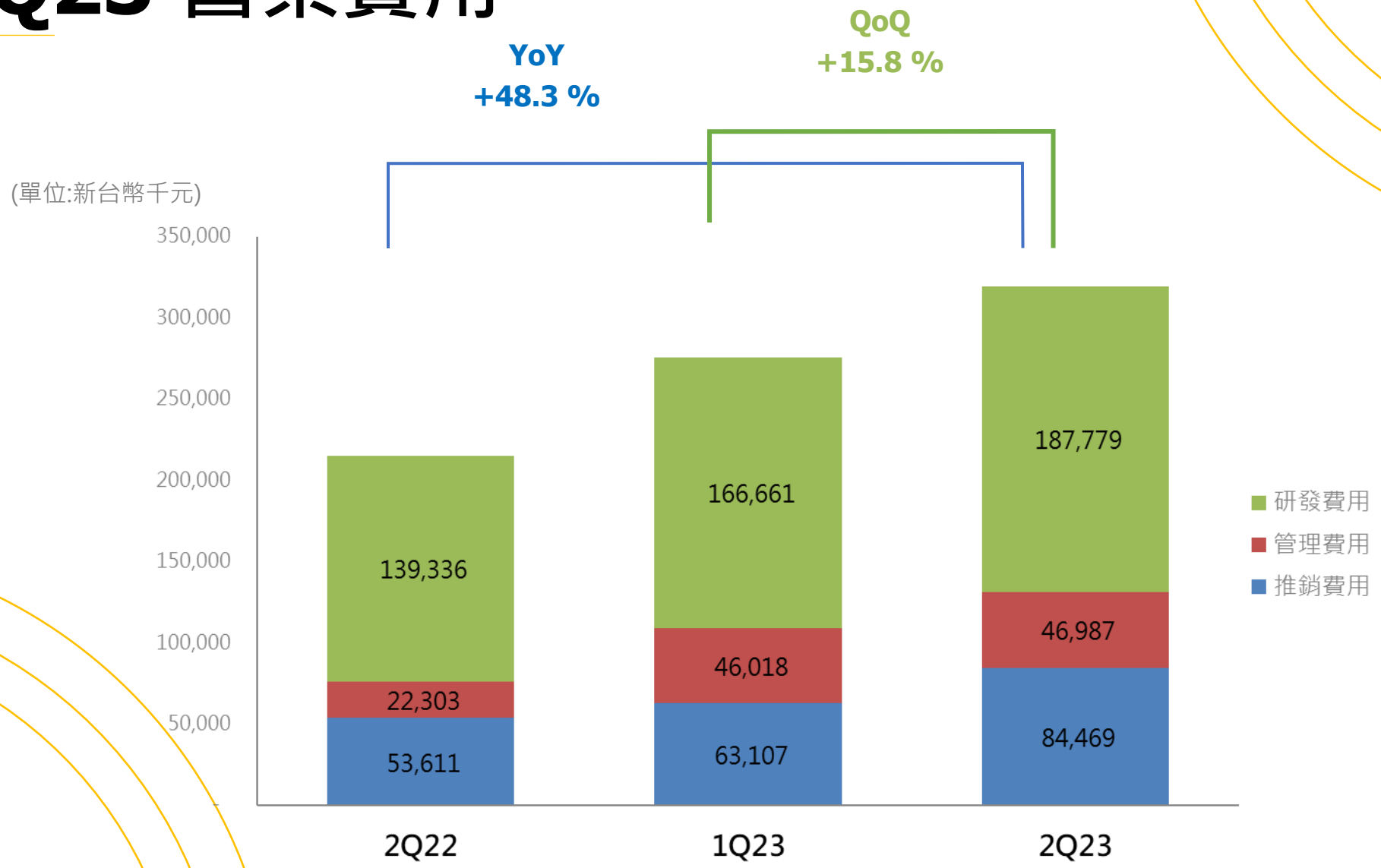
1H23 營業毛利與毛利率

(單位:新台幣千元)

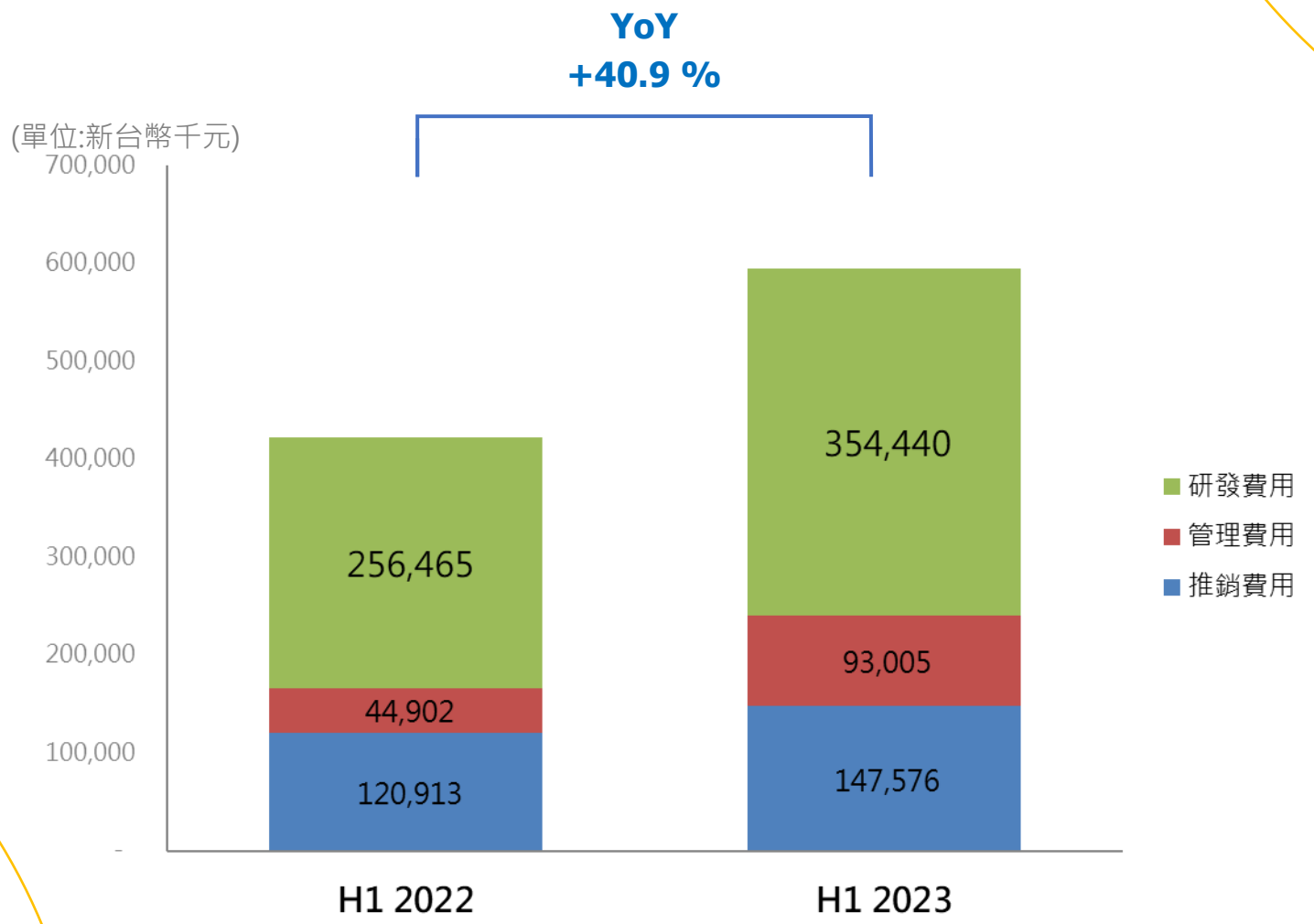


	H1 2022	H1 2023
營業毛利	350,742	403,057
毛利率	99.88%	99.70%

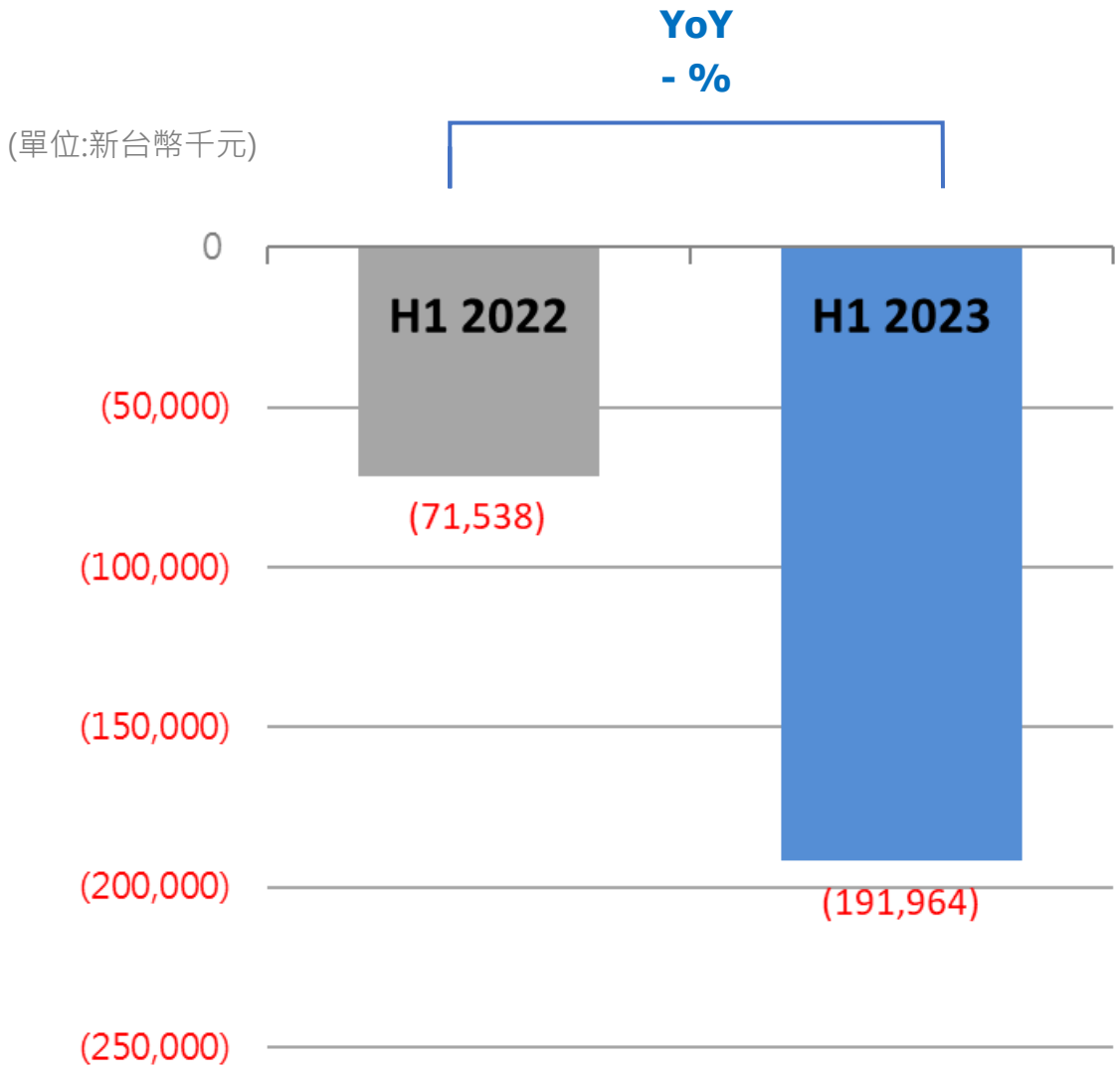
2Q23 營業費用


YoY
+48.3 %
QoQ
+15.8 %
(單位:新台幣千元)
350,000
300,000
250,000
200,000
150,000
100,000
50,000
139,336
22,303
53,611
166,661
46,018
63,107
187,779
46,987
84,469
2Q22
1Q23
2Q23
研發費用
管理費用
推銷費用

1H23 營業費用


YoY
+40.9 %
(單位:新台幣千元)
700,000
600,000
500,000
400,000
300,000
200,000
100,000
-
256,465
44,902
120,913
354,440
93,005
147,576
H1 2022
H1 2023
研發費用
管理費用
推銷費用

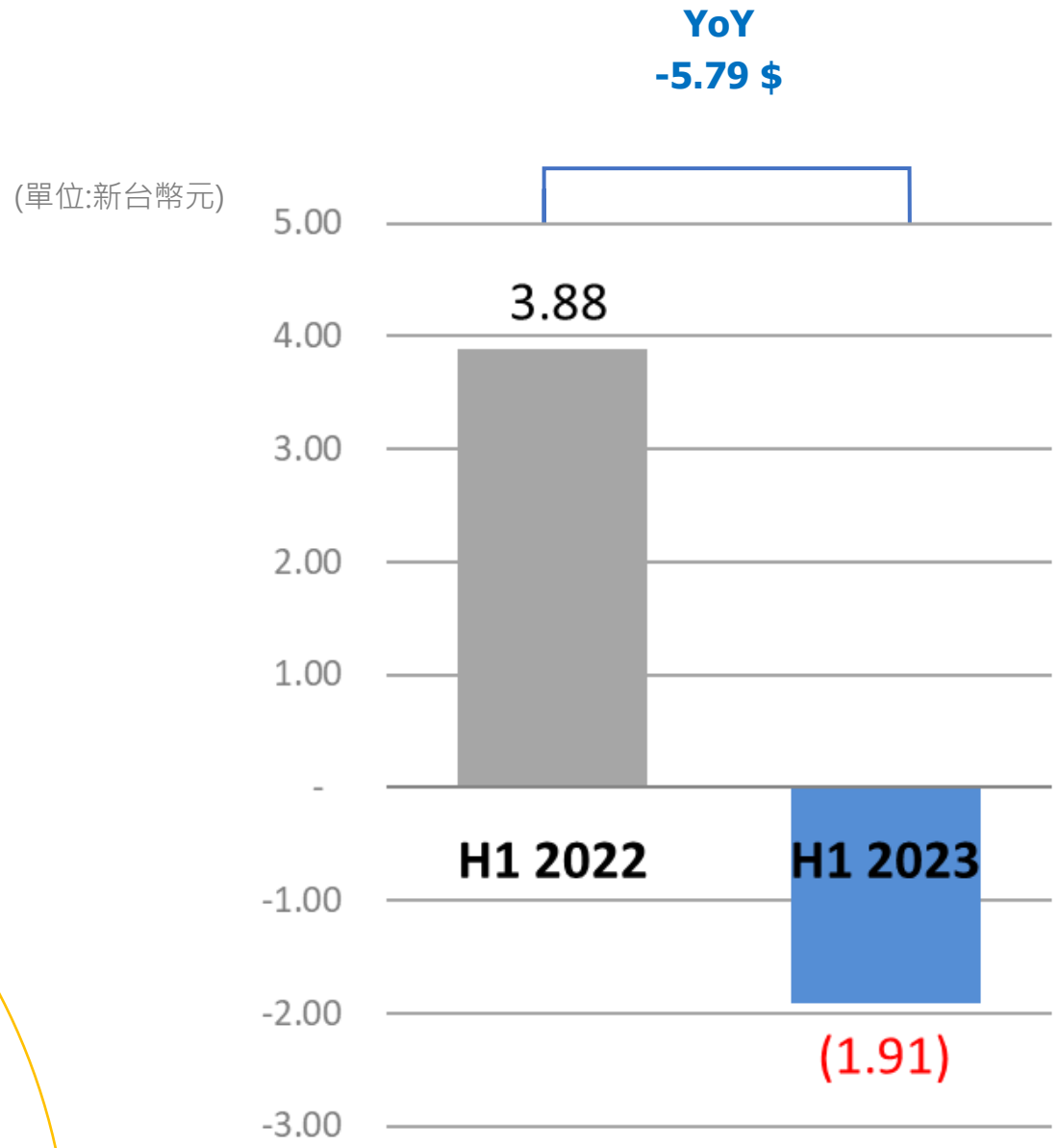
1H23 營業利益


YoY
- %
(單位:新台幣千元)
0
(50,000)
(100,000)
(150,000)
(200,000)
(250,000)
H1 2022
H1 2023
(71,538)
(191,964)

1H23 合併淨利


YoY
- %
(單位:新台幣千元)
250,000
200,000
150,000
100,000
50,000
-
-50,000
-100,000
-150,000
196,317
H1 2022
H1 2023
(96,517)

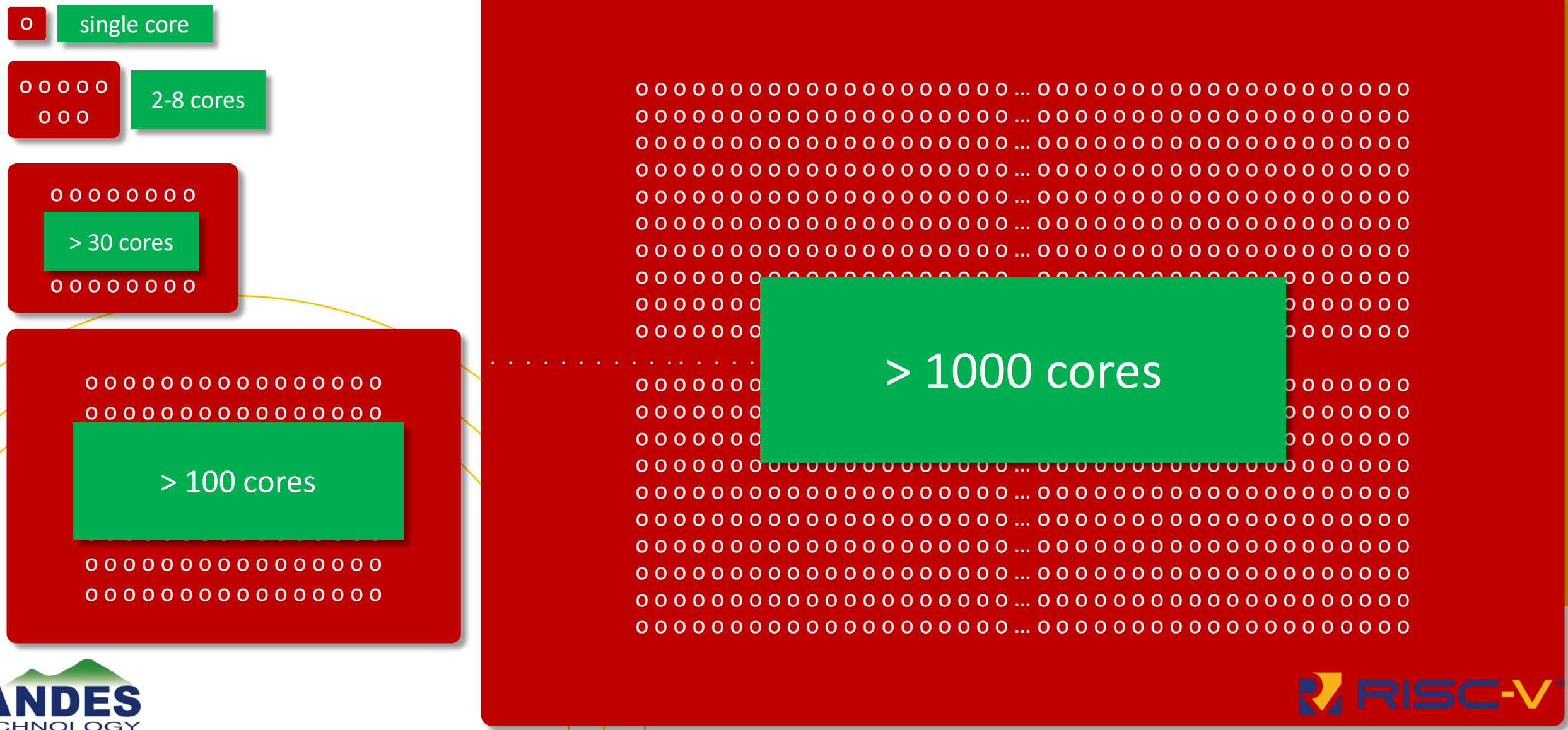
1H23 每股盈餘


YoY
-5.79 $
(單位:新台幣元)
5.00
4.00
3.00
2.00
1.00
-
-1.00
-2.00
-3.00
3.88
H1 2022
H1 2023
(1.91)

產品應用

http://www.andestech.com

晶心RISC-V核心在SoC中被採用的數目



ANDES TECHNOLOGY

RISC-V

Andes RISC-V Powering Rich Applications

Mobile

Performance, code size

N25F, N45

MPU/MCU/AIoT

RENESAS
HPMicro
Kneron
Telink
Internet Company

D25F, D45, AX25MP, AX45MP

Endpoints. Edge. Cloud. Space.

Cloud AI

STREAM COMPUTING
后摩智能 HOUMO.AI
SK telecom
Accelerate, accelerate, accelerate

NX27V, AX25, AX27, AX45MP, AX45MPV

Space

Secure, control, compute, communicate, position

N25F

Storage

Performance, bandwidth, real-time

N25F, N45, AX45MP

5G Networks

picocom
Empowering Wireless

N25F, A25, A45MP, AX45MP

MTIA: Meta Training and Inference Accelerator

- ISCA 2023 paper, “MTIA: First Generation Silicon Targeting Meta’s Recommendation Systems”
- Proc-A/B: Andes AX25-V100, an early version of the popular NX27V
- Custom extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models

Figure 3: High-level architecture of the accelerator

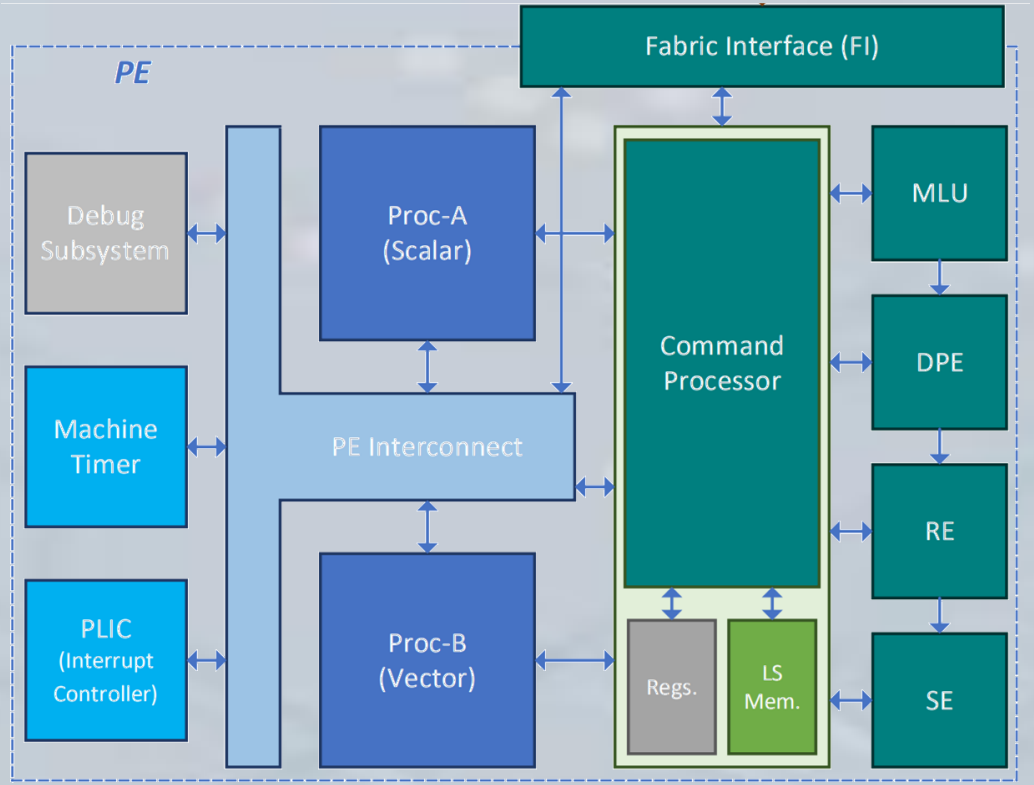


Figure 4: PE’s internal organization

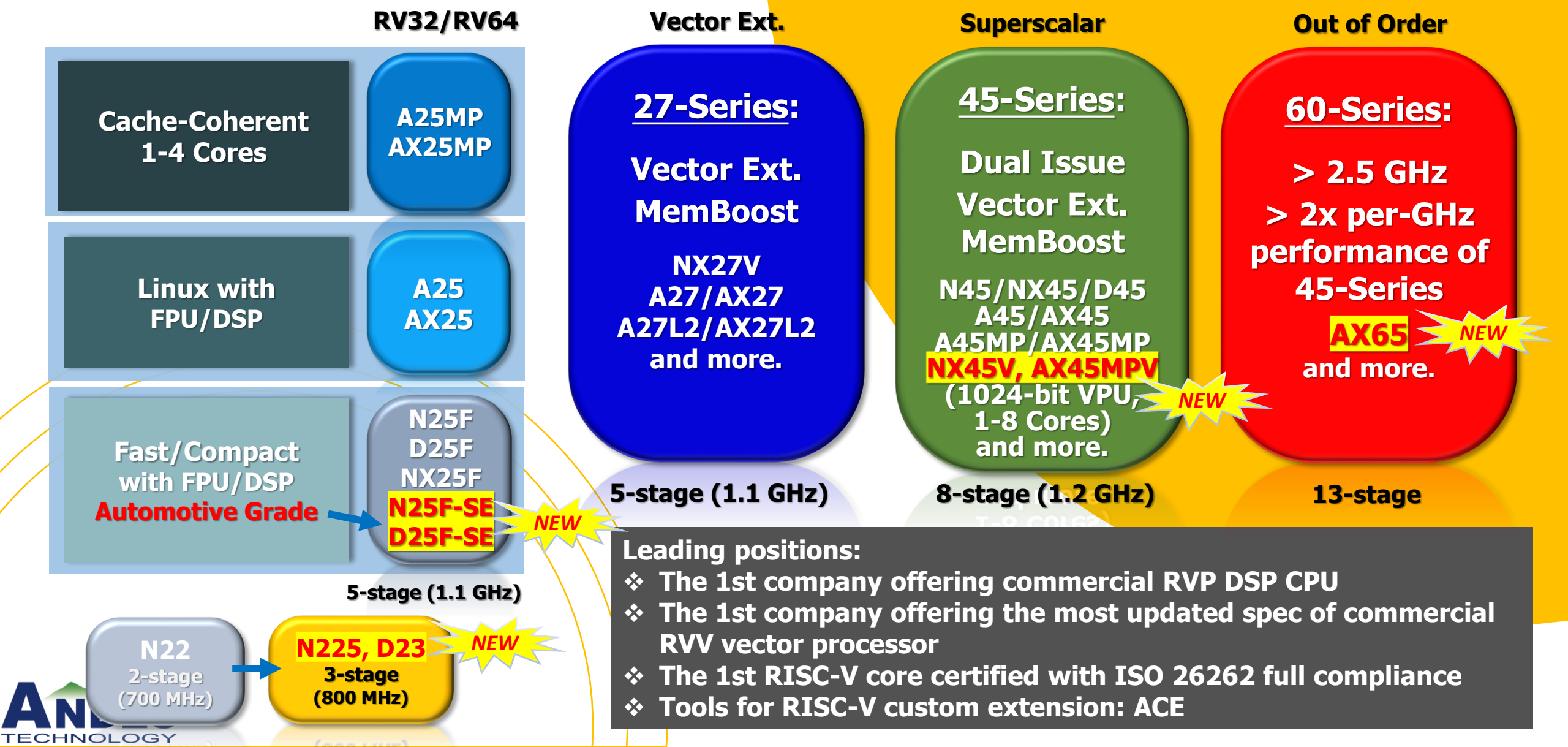
All photos: courtesy of ACM

Powered by Andes NX27V+ACE

New Products and Ecosystems

http://www.andestech.com

晶心RISC-V產品路線圖



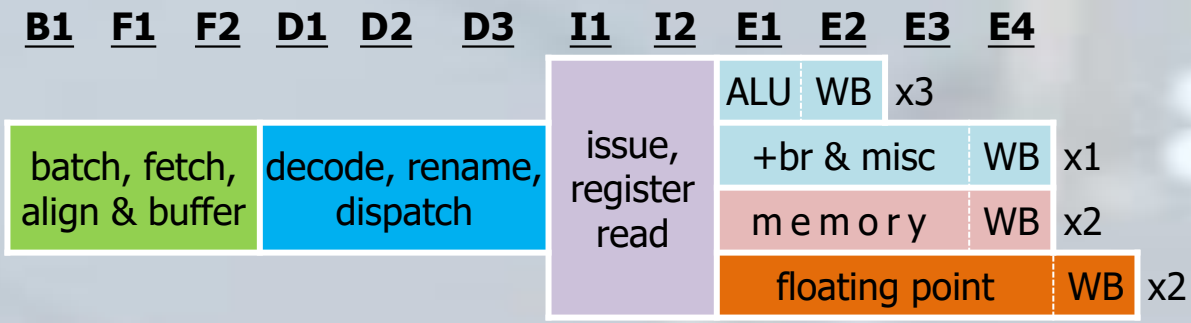
Leading positions:

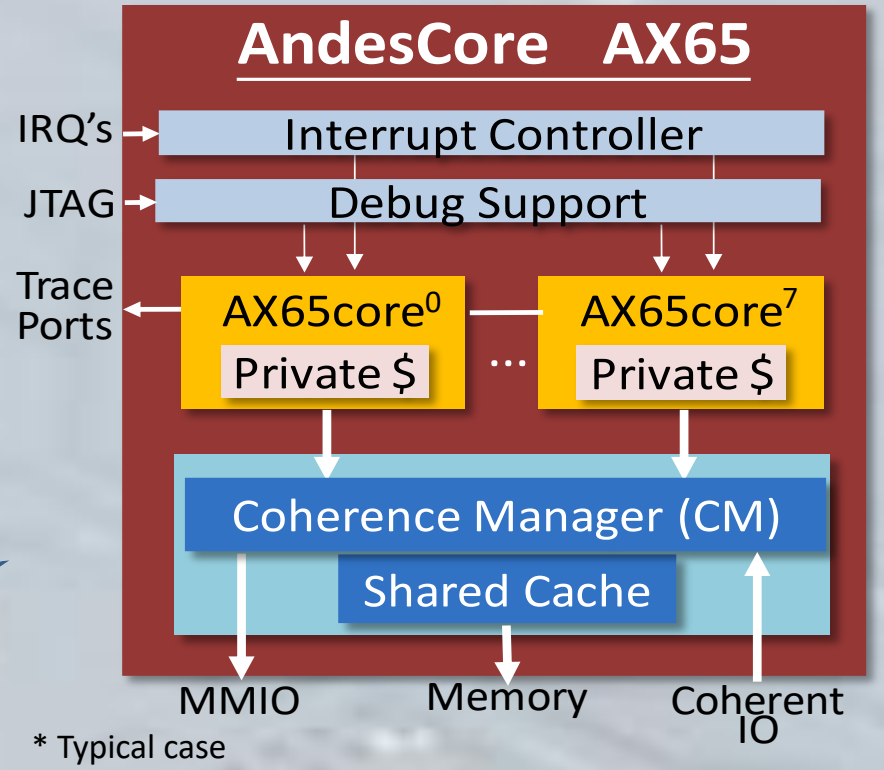
- ❖ The 1st company offering commercial RVP DSP CPU
- ❖ The 1st company offering the most updated spec of commercial RVV vector processor
- ❖ The 1st RISC-V core certified with ISO 26262 full compliance
- ❖ Tools for RISC-V custom extension: ACE

ANDES TECHNOLOGY

AndesCore™ AX65 OOO Application Processor

- 13-stage 4-way 64-bit OOO processor
- RVA22+ profile
- Multicore cluster up to 8 cores
- 8 Execution Pipes: 4 ALU, 2 LD/ST, 2 FP
- 2-Level BTB with TAGE-L Branch Predictor
- Caches:
  - Private I/D caches: 64 KB, 4-way, 4-bank
  - Shared cache: up to 8 MB, 16-way
- 256-bit AXI4 for Memory, MMIO and IOCP
- Performance:
  - 2.4 GHz* @7nm without overdrive
  - Specint2006: 8.25/GHz
  - Specfp2006: 10.2/GHz





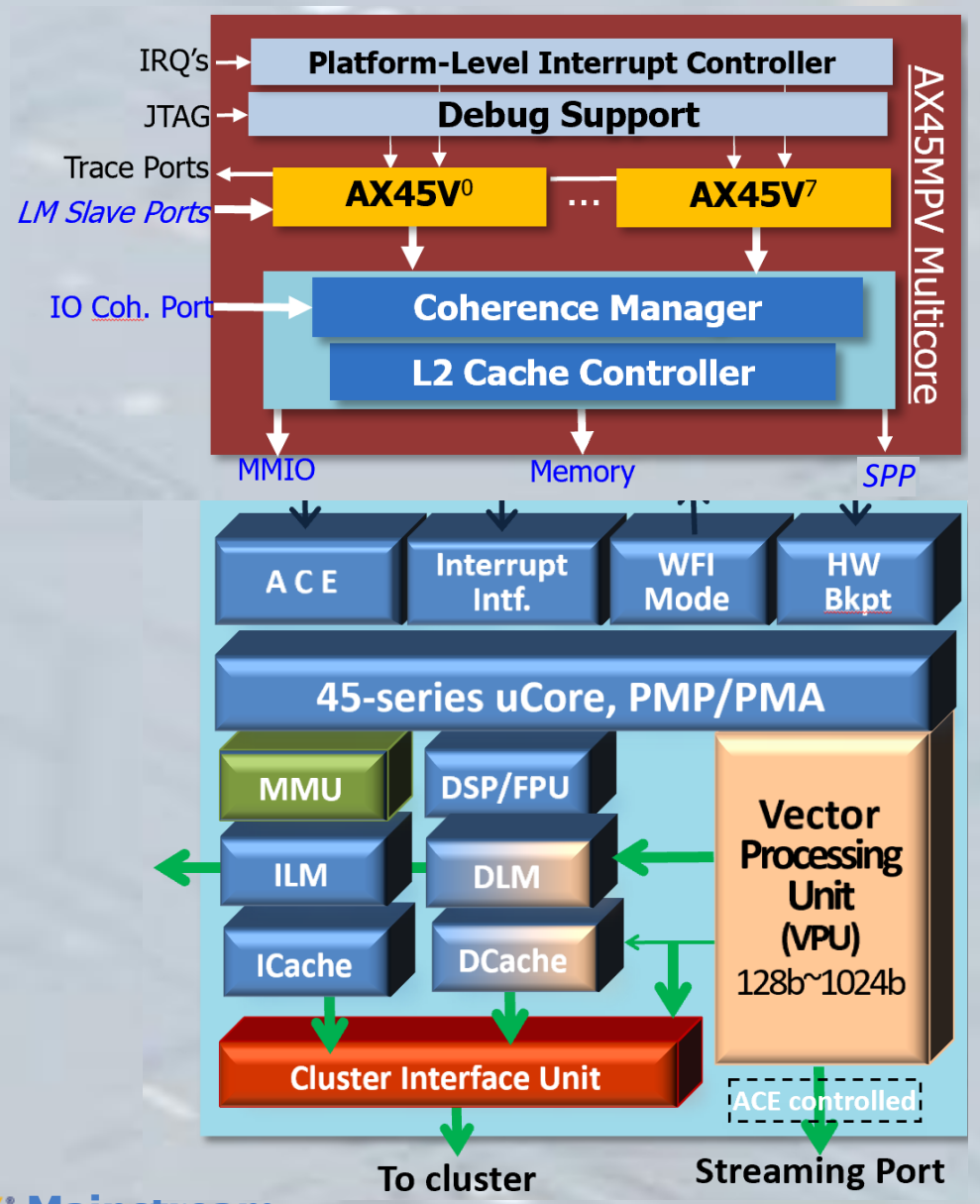
Best spec2k6 with 2-level caches

* Typical case

Roadmap for the AX60 Series

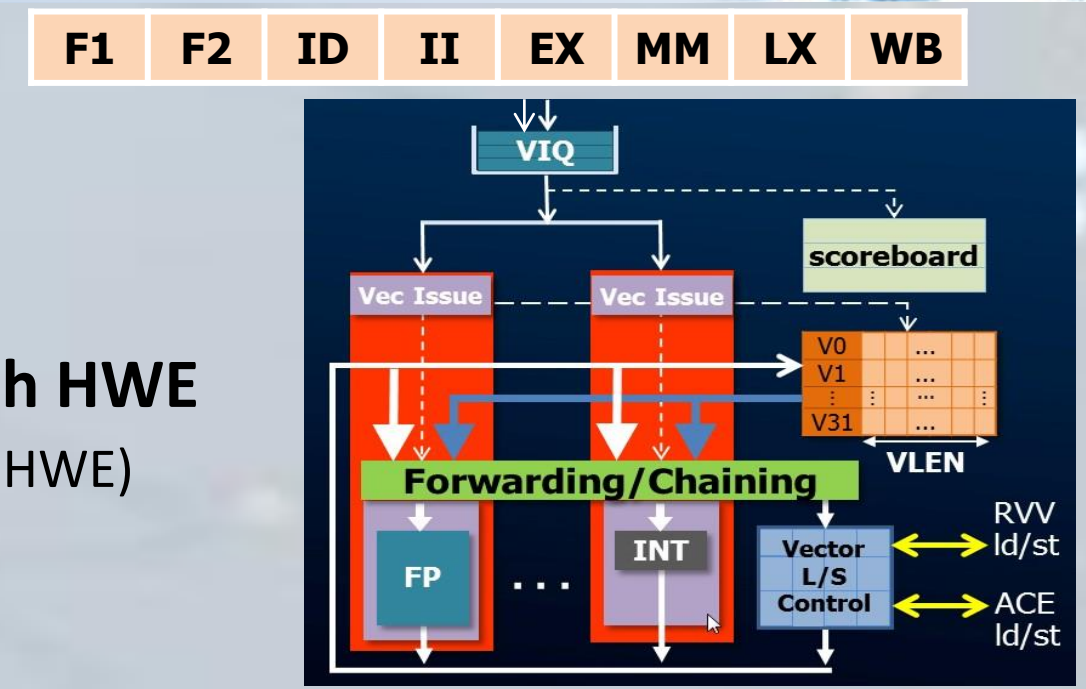
AX45MPV Multicore Cluster

- **At multicore cluster level:**
  - Up to 8 cores
  - CM/L2$ subsystem
    - 128KB to 8MB, 64B line, 16-way
    - Multi-cycle support for high-density SRAMs
    - I/D prefetch, up to 64 outstanding requests
  - AXI Bus Interfaces up to 512 bits
- **Scalar Unit: RV64GCBP**
  - 8-stage In-order dual-issue
  - MMU/SV48, M/S/U modes
  - I/D caches: 8K~64KB; Parity (I$) or ECC (both)
- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, **bf16**
  - VLEN/DLEN: 128~**1024** bits, 1:1 or 2:1 ratio
  - Up to 6 DLEN results per cycle

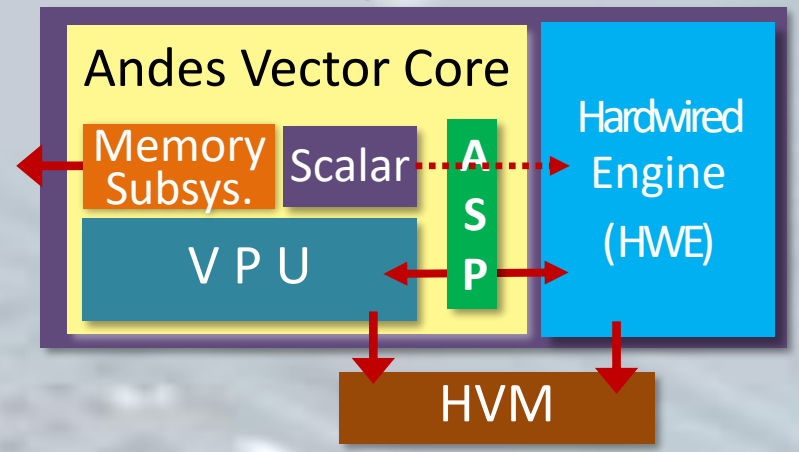


AX45MPV: 1024-bit Vector Processor

- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, **bf16**
  - VLEN/DLEN: 128~**1024** bits, 1:1 or 2:1 ratio
  - Up to 6 DLEN results per cycle
- **Efficient support needed for tight coupling with HWE**
  1. Data exchange performance (from/to shared memory in HWE)
  2. Efficient control to the HWE
- **2 solutions offered in AX45MPV:**
  - Andes Streaming Port™ (ASP) thru ACE
    - Data bus: data transfer btw VR and HWE
    - Command bus: to control/synchronize HWE operations
  - HVM: High-speed Vector Memory
    - CPU side: DLEN-wide load/store interface with dynamic wait cycles
    - HVM module: accepting multiple accesses to multi-bank SRAM's



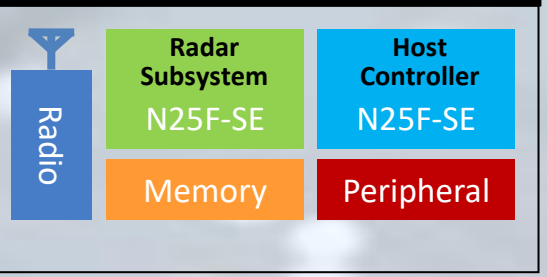
Processing Element (PE)



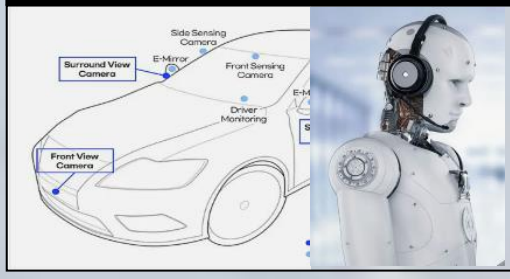
Andes is *Driving* Innovations in Automotive

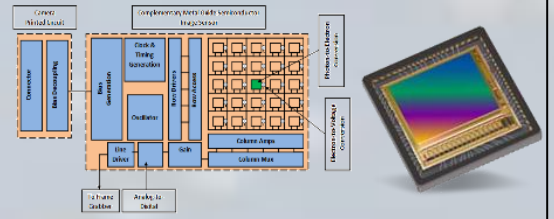
with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar

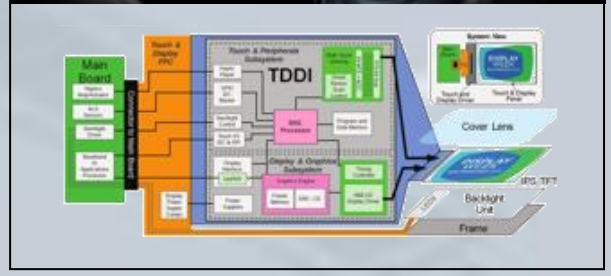


CMOS Sensor



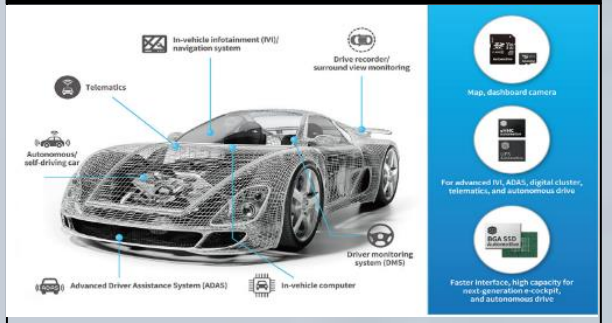


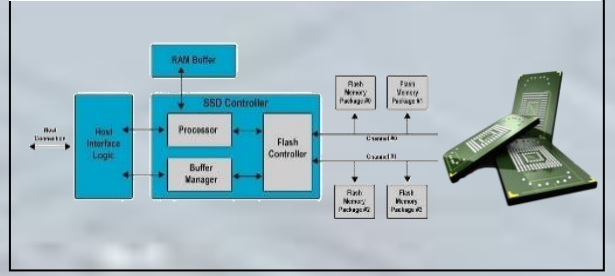
Auto TDDI



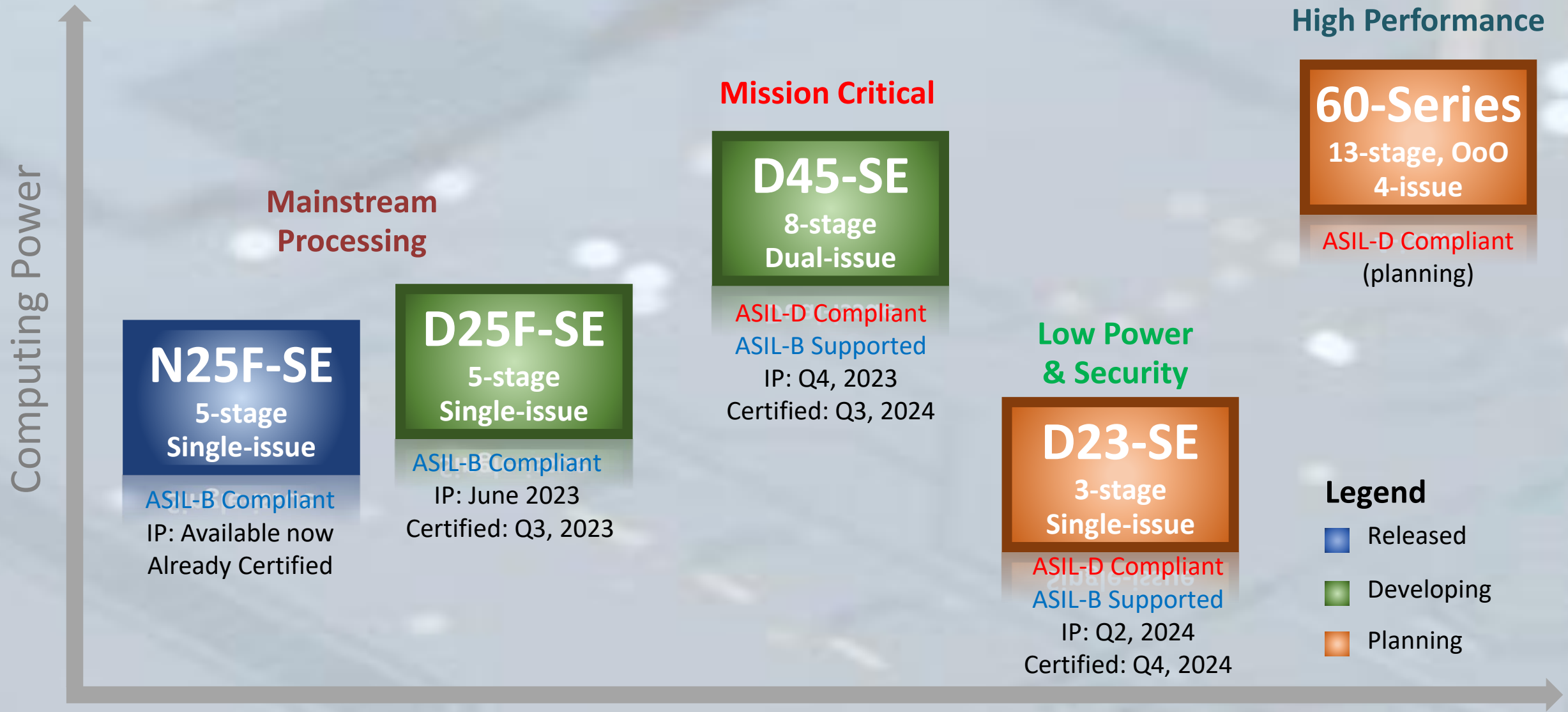
Auto MCU

Auto Storage



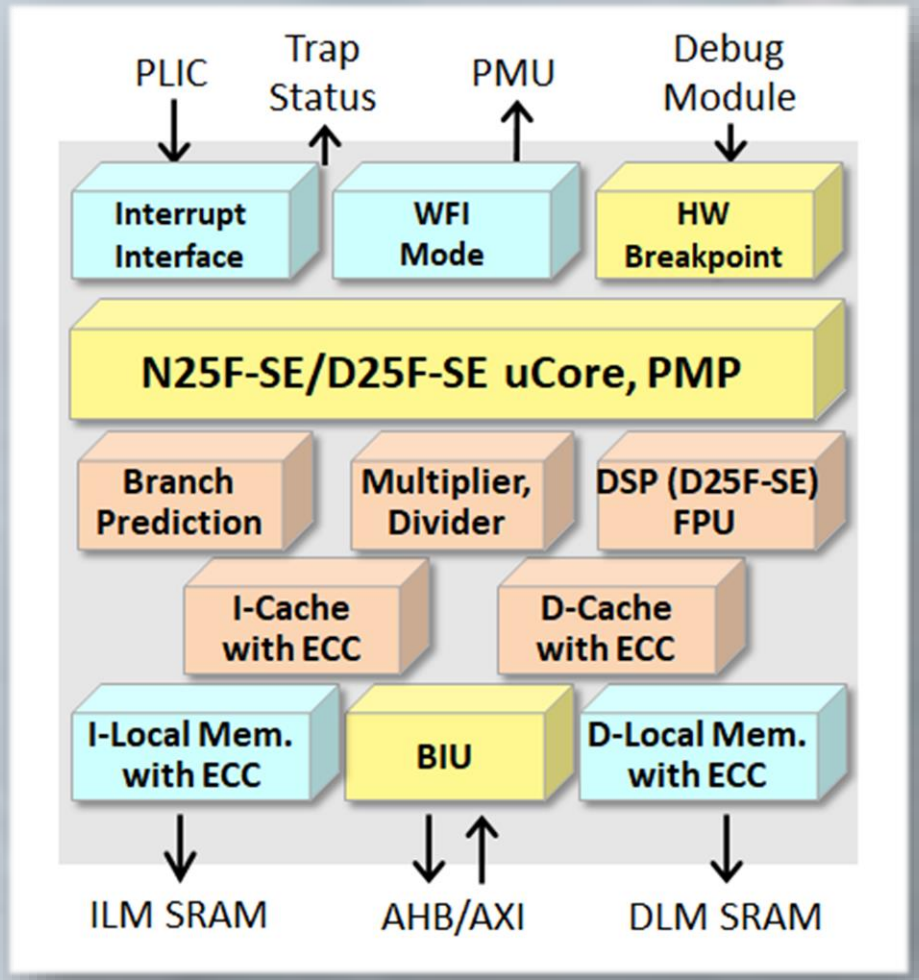


AndesCore™ RISC-V Functional Safety Roadmap



N25F-SE, D25F-SE 5-Stage, ASIL-B Full Compliant

- **CPU Core**
  - 5-stage, in-order, single-issue architecture
  - RISC-V RV32 GCB[P]* ISA, with Andes Extensions
    - D25F-SE with the RVP (SIMD/DSP) instruction extension
    - RVB bit-manipulation instructions for cryptography, … applications
  - AndeStar™ V5 32-bit architecture
- **Memory Subsystem**
  - Instruction and data caches, up to 32KB each
  - Instruction and data local memories, up to 16MB each
- **Bus Interfaces and System Integration**
  - AXI or AHB bus master port
  - Local memory direct access port
- **Functional Safety**
  - Core trap status bus interface,
  - ECC protection, StackSafe™, PMP …
  - N25F-SE, ASIL-B certified. D25F-SE, ASIL-B certified at Q3/2023



AndesCore™ N25F-SE Certified by ISO 26262

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID	LICENSED TEST MARK	Report No.
S280	SGS TÜV SAAR ASIL B COMPLIANT Functional Safety ISO 26262	S2800001

Tested according to ISO 26262:2018 (Parts 2, 4 partly, 5, 8, 9)

Certified Product(s) CPU IP "N25F-SE"
Version: R320

Technical Data/Parameter The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance with **ASIL B** requirements.

Specific Requirements The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval.
The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

Munich, October 28th, 2022

Marcus Rau

The validation status is documented via SGS Certification Database.

The test mark regulation is an integral part of this certificate.

SGS-TÜV Saar GmbH, Hofmannstr. 50, D-81379 München, Deutschland / Germany.
Website: www.sgs-tuv-saar.com/fs
E-Mail: fs@sgs.com

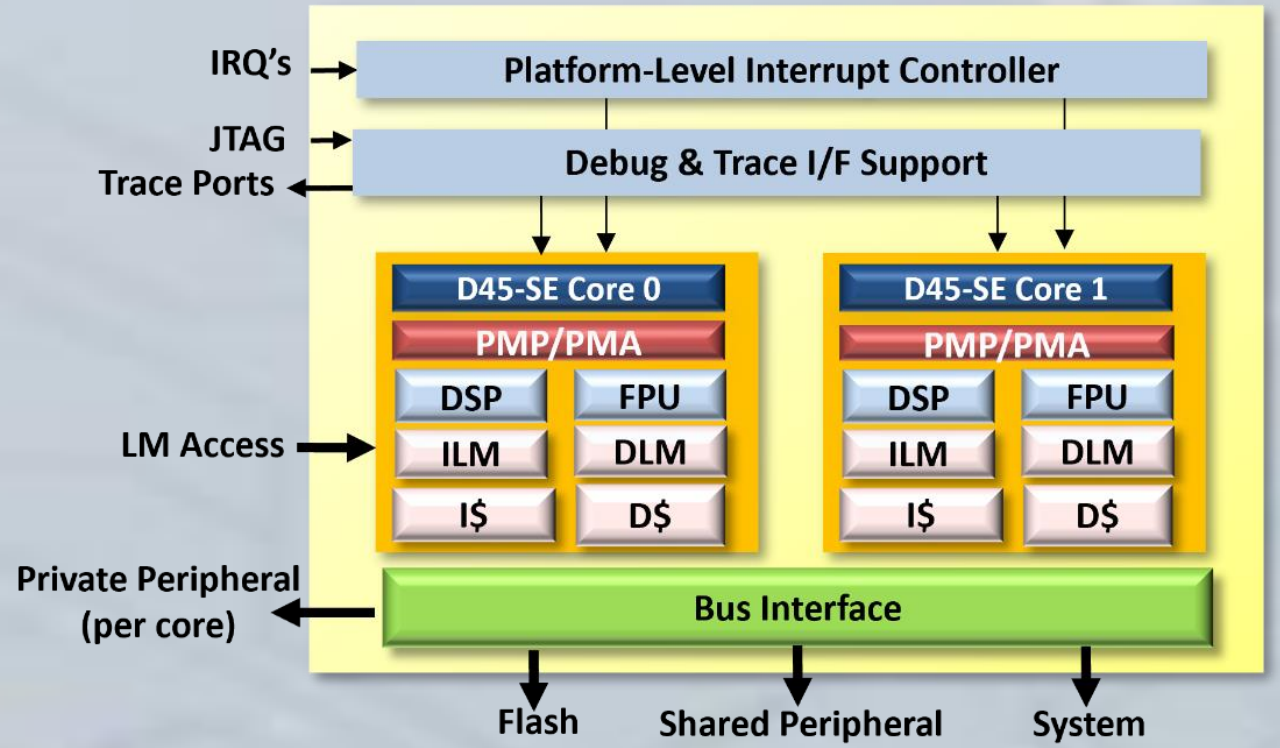
CERTIFICATE

- **"The product has been approved in compliance with ASIL B requirements"**
- **ISO 26262 Edition 2018, parts:**
  - ISO 26262-2:2018
  - ISO 26262-4:2018*
  - ISO 26262-5:2018
  - ISO 26262-8:2018
  - ISO 26262-9:2018
- **Certification Body**
  - SGS-TÜV Saar GmbH
  - SGS-TÜV Saar GmbH accredited by German accreditation body DAkkS

* Part-4 System/item level integration, validation is not applicable to CPU IP

D45-SE 8-Stage, Dual-Issue, up to ASIL-D

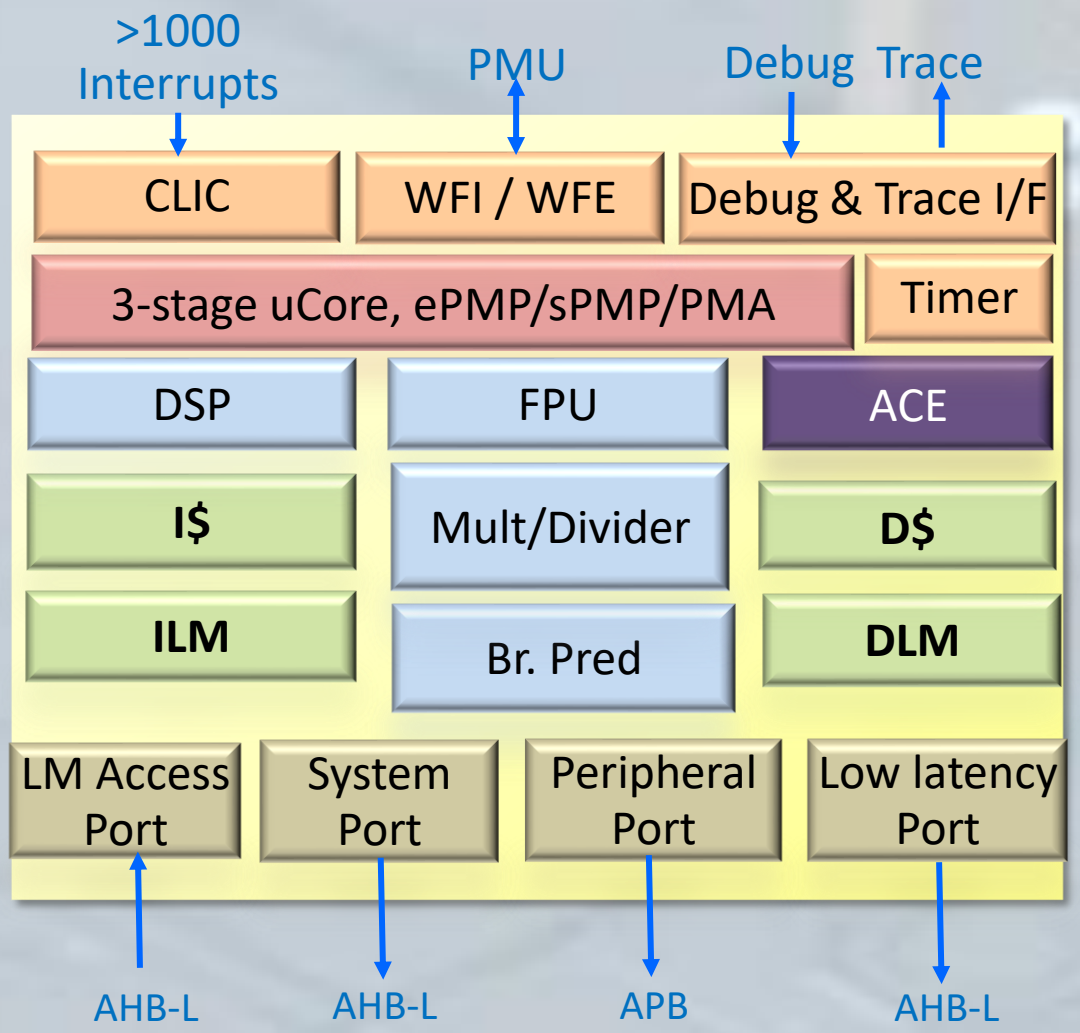
- **CPU Core**
  - 8-stage, in-order, superscalar, dual-issue most instruction pairs
  - RISC-V RV32 GCBP* support, Andes Extensions
  - AndeStar™ V5 32-bit architecture
- **Memory Subsystem**
  - Instruction and data cache, up to 64KB
  - Instruction and data local memory, up to 16MB
  - MemBoost
- **AXI Bus Interfaces**
  - System port, and flash port (64/128-bit)
  - LM access port (64/128-bit)
  - Private, and shared peripheral interface (64-bit)
- **Functional Safety**
  - Lockstep and Split mechanism
  - Configurable ECC for every memory
  - Core trap status bus interface
  - Bus protection, StackSafe™
  - Certified estimated by or before Q3/2024



*P: draft

D23: Compact Controller for IoT/MCU/ECU

- **3-stage, limited dual-issue (optional)**
- **ISA extensions:**
  - Base: RV32 I/E-MAC + B + Zce
  - Advanced: FD + P + K + CMO
- **Privilege modes: M, S, U**
- **Configurable features**
  - Branch prediction: none, static, dynamic
  - Multiplier options:
    Sequential: 1/2/4/8-bit per cycle
    Fast: pipelined
  - Andes Custom Extension™ (ACE)
  - Power management: WFI/WFE, PowerBrake
  - Core-Local Interrupt Controller (CLIC)
    >1000 sources, 255 priority levels
    Selective vectoring with priority preemption



D23: Compact Controller for IoT/MCU/ECU

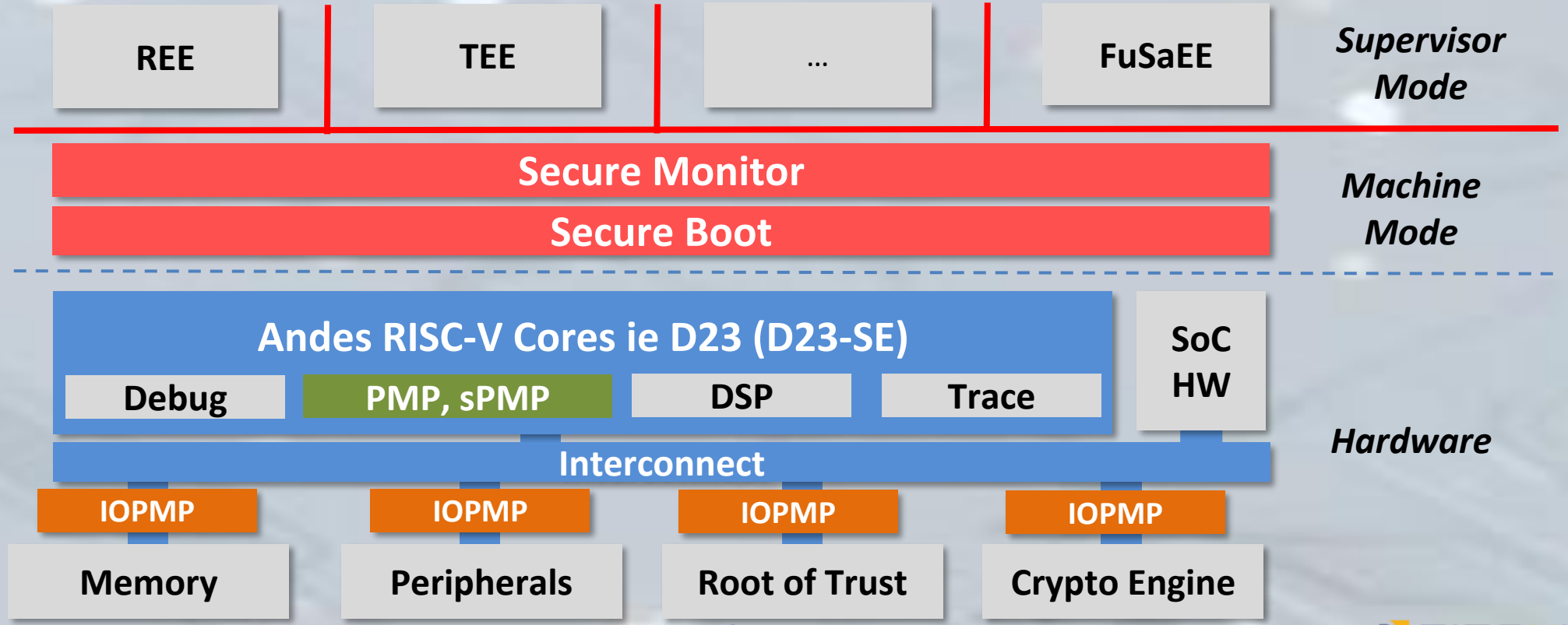
- **Memory subsystem:**
  - Caches:
    - Config:
      - Icache only: ifetch
      - RO-cache (Read-Only): ifetch and load
      - I/D caches: ifetch, load and store
    - Cache sizes: 1KB~32KB
    - Error protection: ECC for I$ and D$
  - I/D Local Memory (LM):
    - 0~512MB with ECC
    - Interface: SRAM or AHB-L

RISC-V Code Size Benchmarks							
ISA	IMAC	IMAC + V5 (N22)		IMABC + V5 (N25F)		**IMABZce + V5 (D23)**	
SPEC CPU	2,840	2,360	-16.9%	2,346	-17.4%	**2,247**	**20.9%**
CSiBE	1,462	1,204	-17.6%	1,190	-18.6%	**1,144**	**21.8%**
Audio Codec	842	682	-19.0%	671	-20.3%	**656**	**22.1%**
Embench-IoT	63.6	51.2	-19.5%	48.9	-23.1%	**48.4**	**23.9%**

- D23-SE Safety-Enhanced D23 for Automotive designs, ASIL-D compliant & ASIL-B supported

Security System Architecture for D23 (D23-SE)

- Create multiple zones protection by PMP/sPMP
  - REEs (Rich Execution Environment)
  - TEEs (Trusted Execution Environment)
- IOPMP for IO protection



The Rise of

AndesAIRE™ AnDLA™ I350

The First Generation of Andes Deep Learning Accelerator

AndesAIRE™ NN SDK

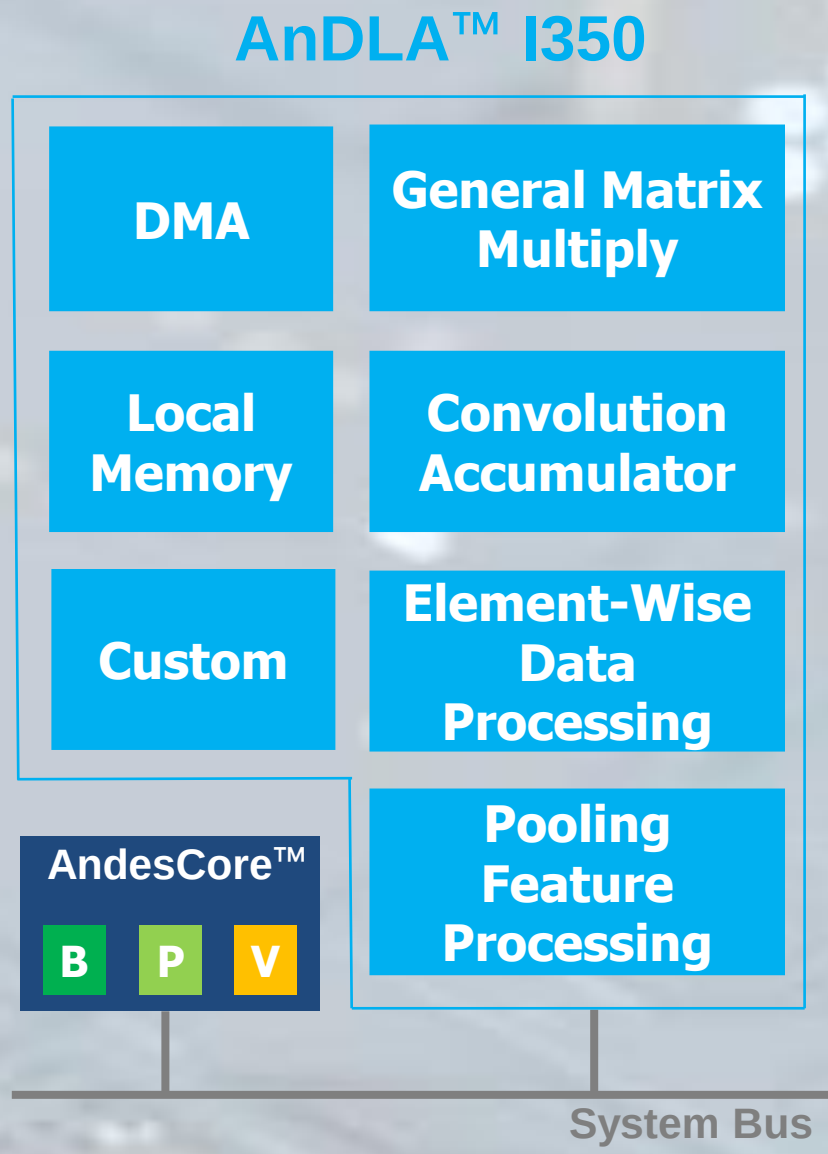
Unleash the maximum AI/ML performance
and synergy of RISC-V CPU and AnDLA™

AndesAIRE™

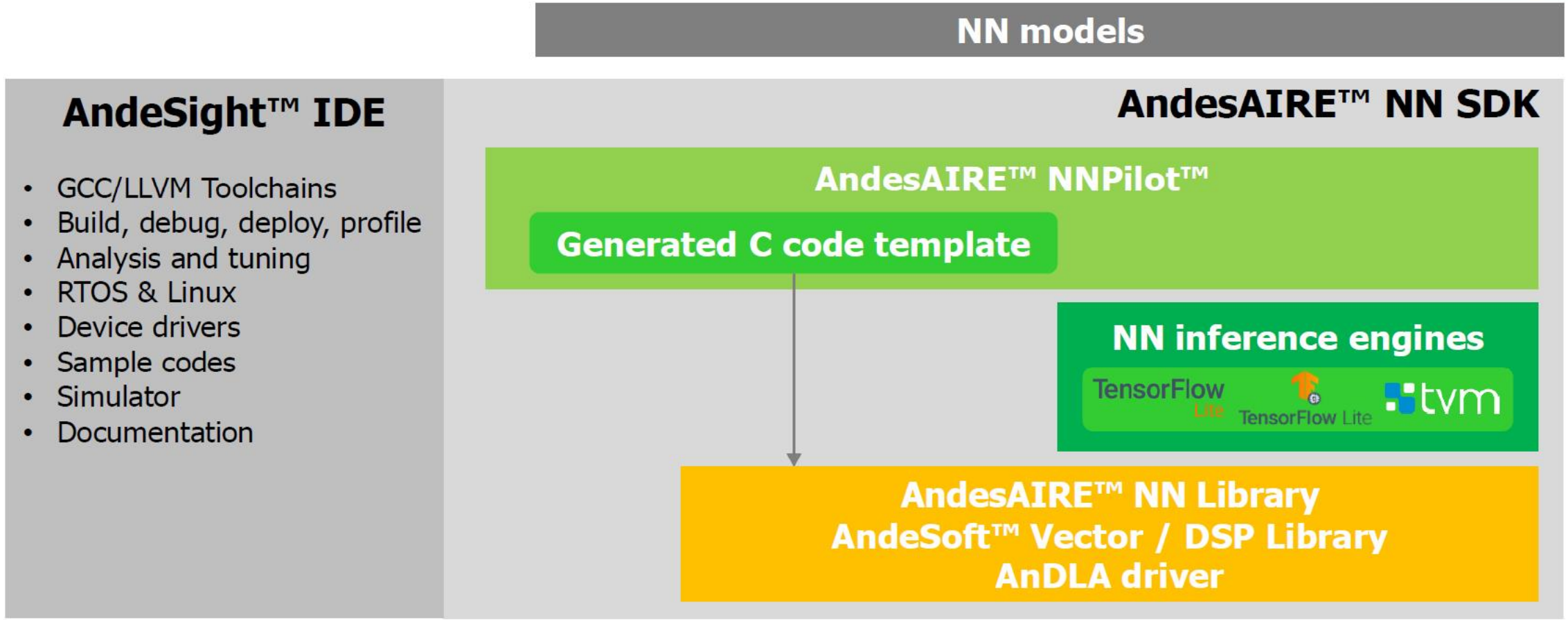
Andes AI Runs Everywhere

AndesAIRE™ AnDLA™ I350

- Andes Deep Learning Accelerator (AnDLA™)
  - High performance-efficient deep learning accelerator for edge and end-point inference
  - Scalable and multi-DLA
  - Cooperate with AndesCore™ full series (22/23/25/27/45/65)
- Accelerating for most of NN Applications
  - Image and video
  - Speech/voice and audio
- Target performance
  - Configurable MACs: 32 to 4096 (INT8)
  - Performance: 64 GOPS to 8 TOPS (INT8 @1GHz)
  - Configurable local memory: 16KB to 4MB
  - Leading power efficiency >5 TOPS/W (@28nm)
- Integrated DMA and local memory



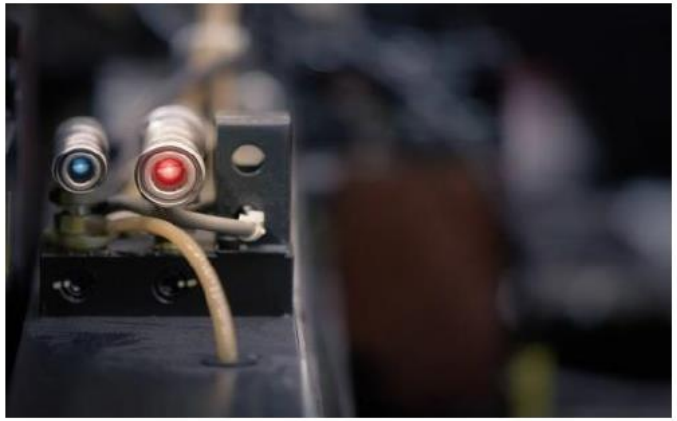
Andes AI Total Solutions



AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera

Smart Sensor



Smart Home Appliance

AIoT / tinyML

Robotics

Wearable

Taking RISC-V® Mainstream

Thank You

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