



# Andes Technology Corp. Investor Conference Report



# Safe Harbor Notice

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Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

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# Company Overview

<http://www.andestech.com> 

## Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 400 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)
- EE Awards - “Taiwan-Product Award” & “Asia-Company Award” (2021)
- Top 500 High-Growth Companies Asia-Pacific 2023

## Andes Mission

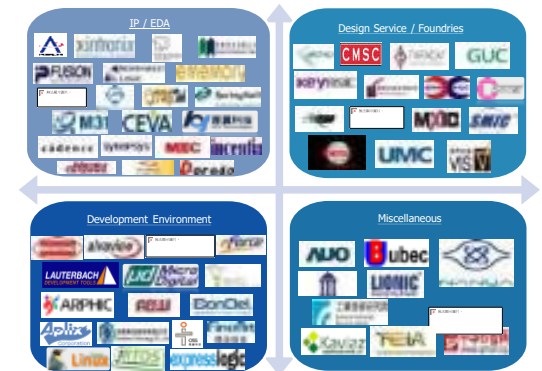
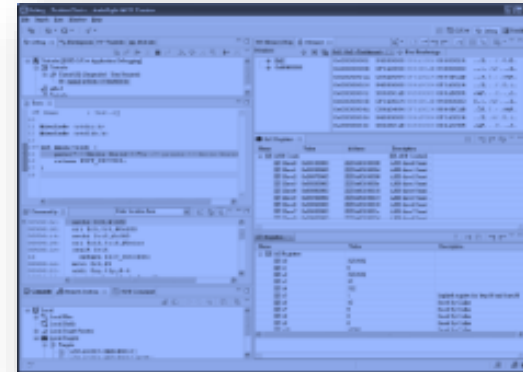
- Innovate performance-efficient processor solution for low-power SoC

## Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

# Business Status Overview

- ❖ **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed
- ❖ AndeSight™ IDE:
  - **~25,000** installations
- ❖ Eco-system:
  - **500+** partners
- ❖ **12B+** Accumulative SoC Shipped





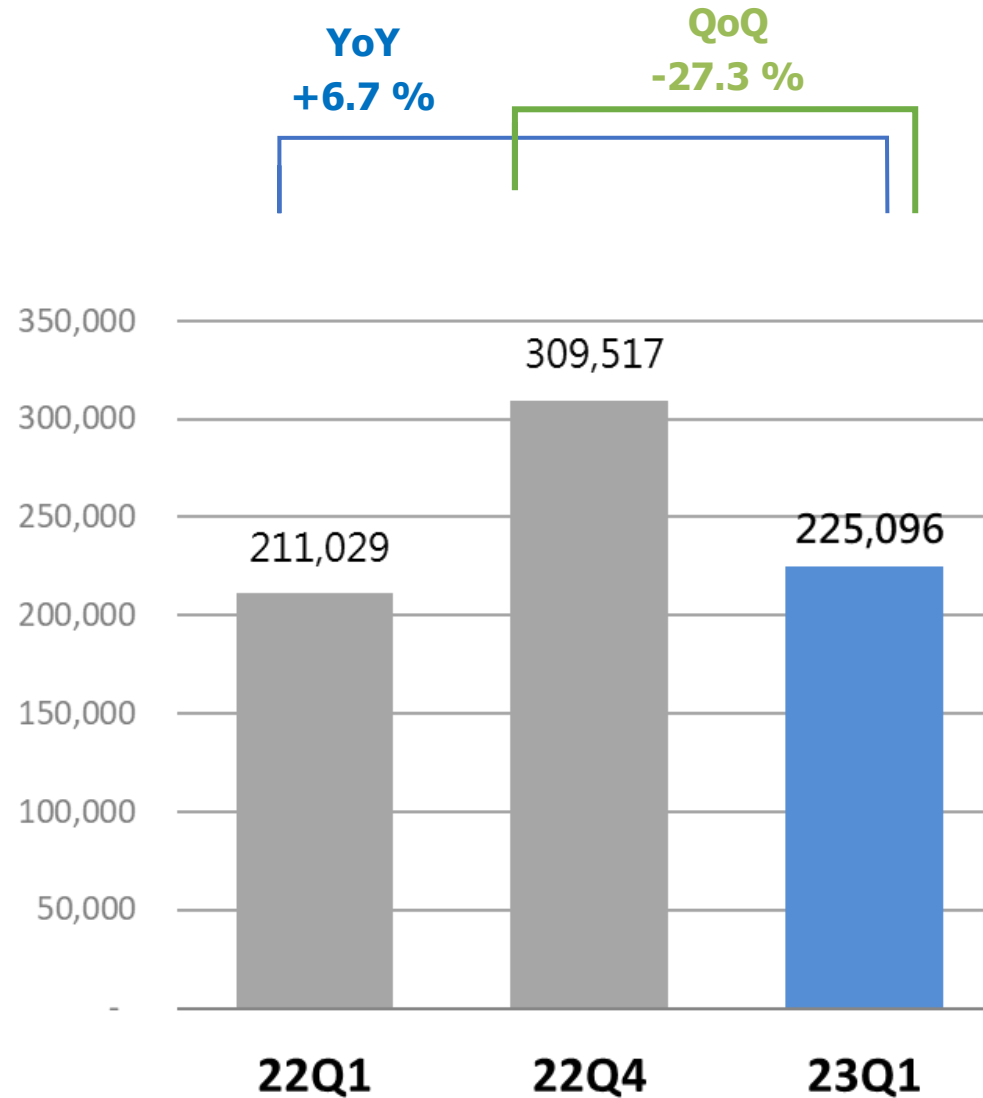
# Operation Results

<http://www.andestech.com>



# 1Q23 Revenue Analysis

(NT\$ thousands)

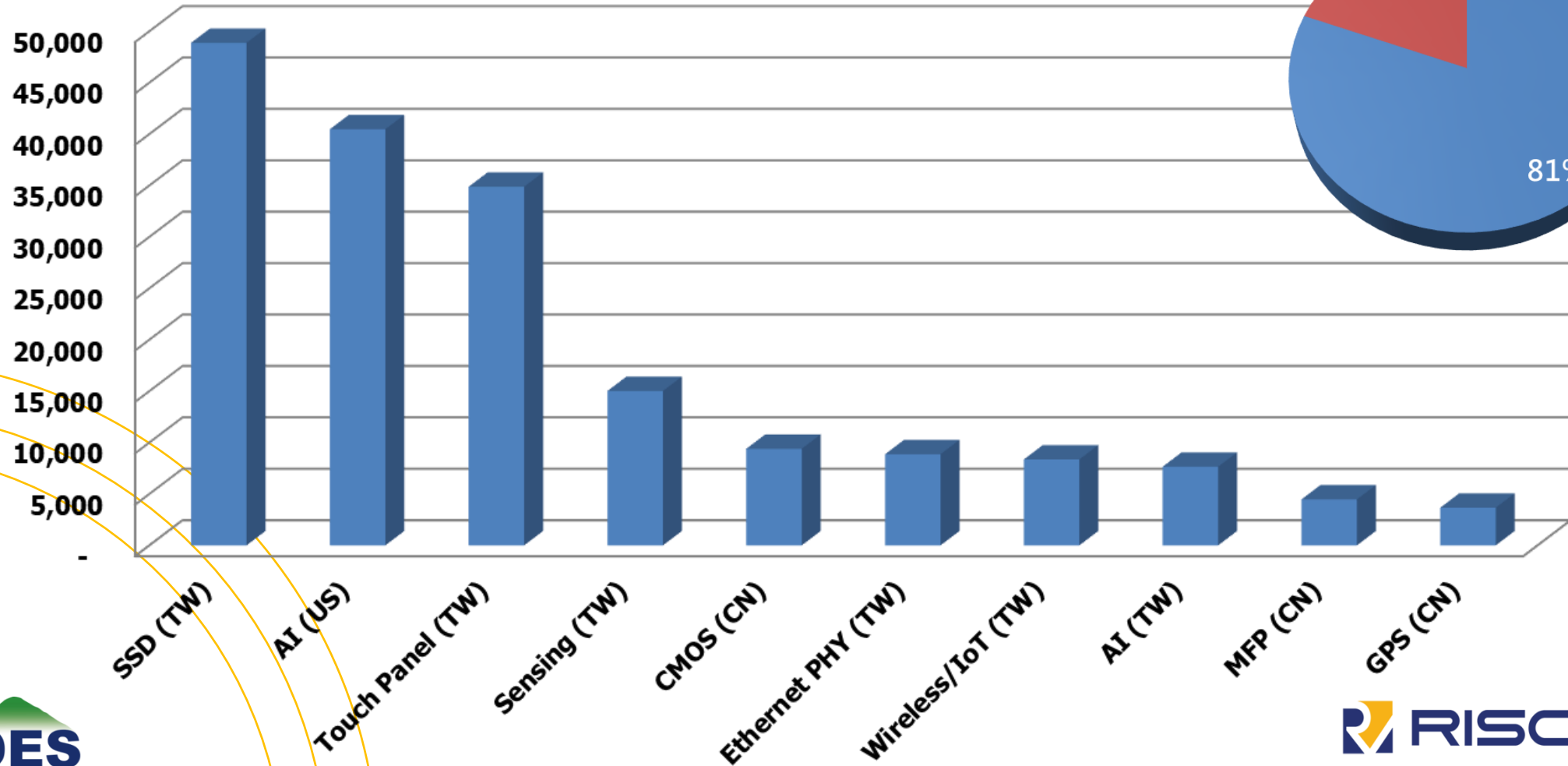




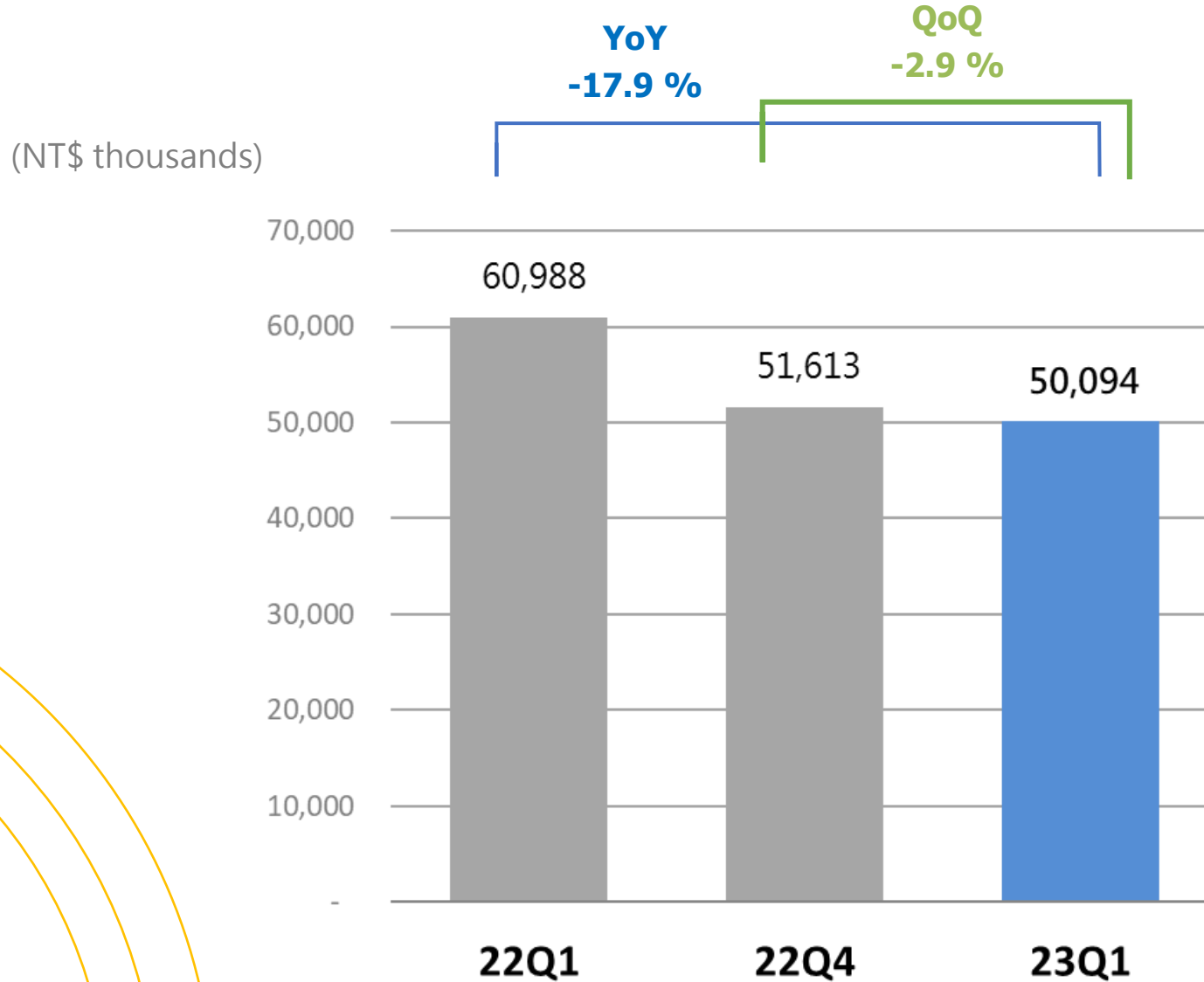
# 1Q23 Top 10 Customers Analysis by Revenue

(NT\$ thousands)

Top 10 Customer Contributed 81% Revenue



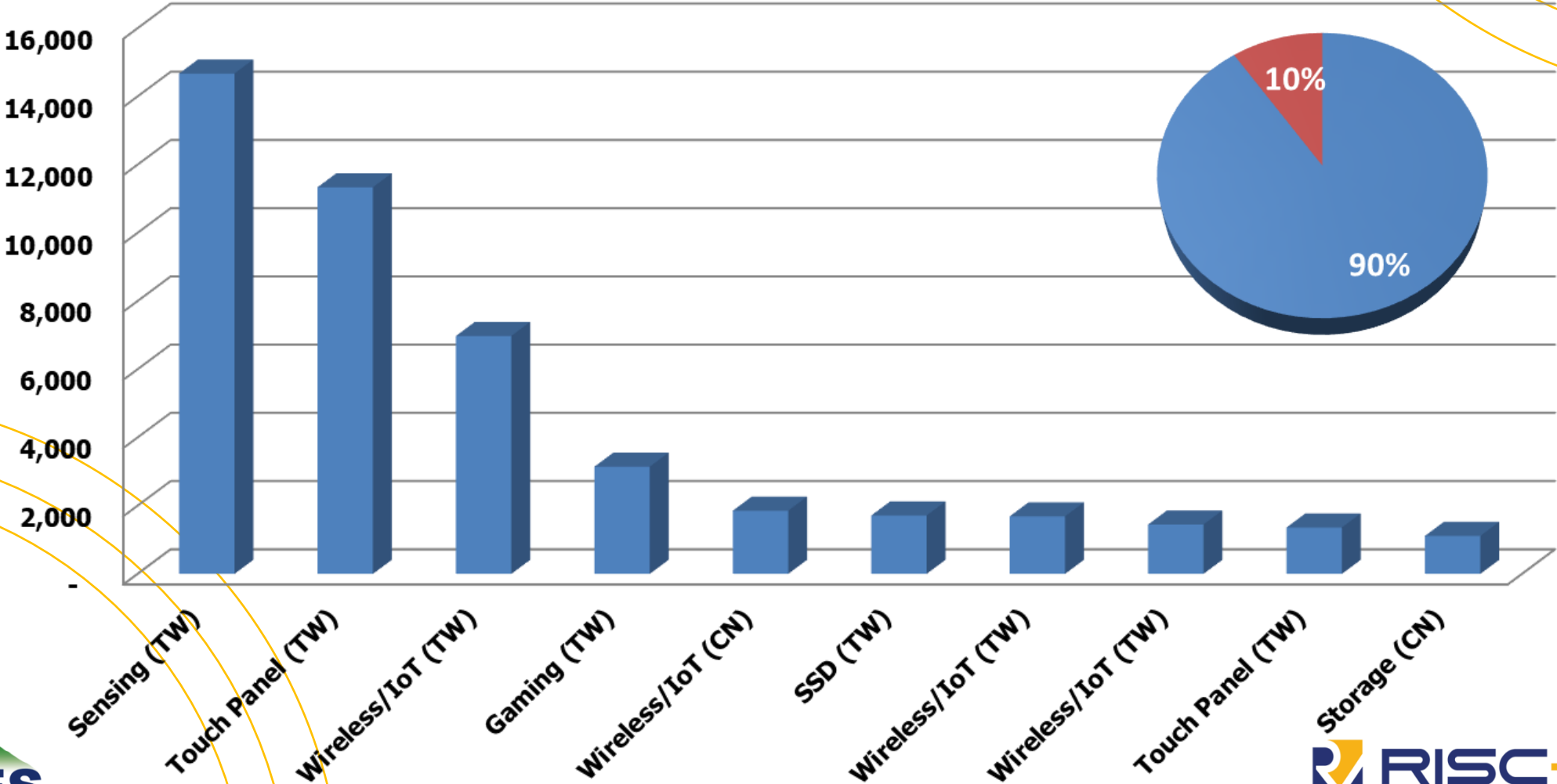
# 1Q23 Royalty Analysis



# 1Q23 Top 10 Royalty Contributors Analysis by Application

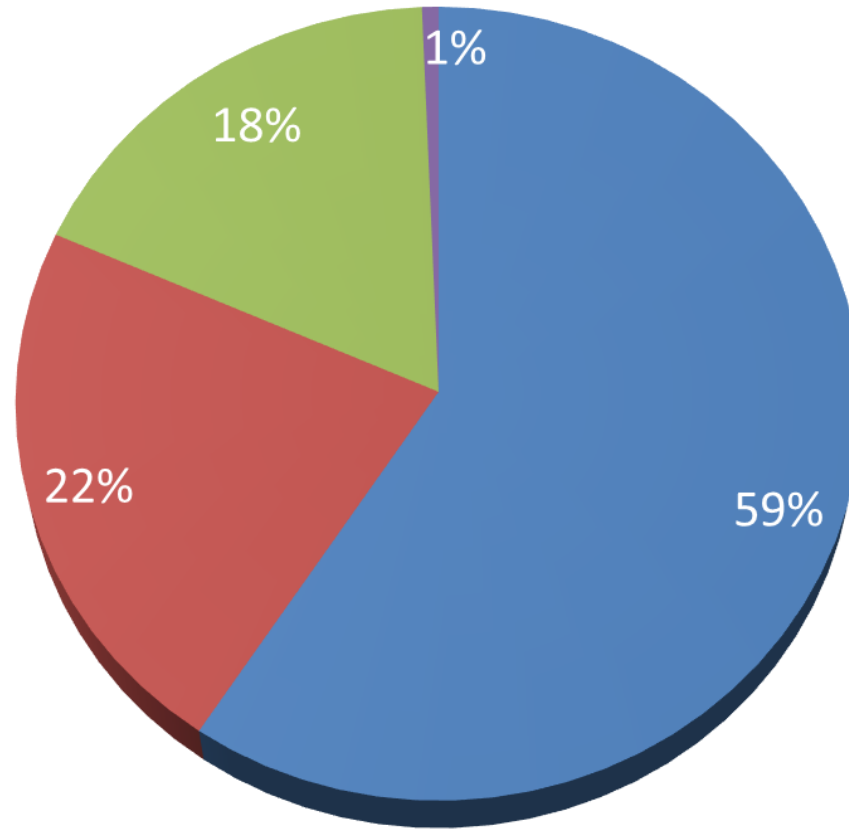
(NT\$ thousands)

Top 10 Royalty Customers  
Contribution Analysis: 90%



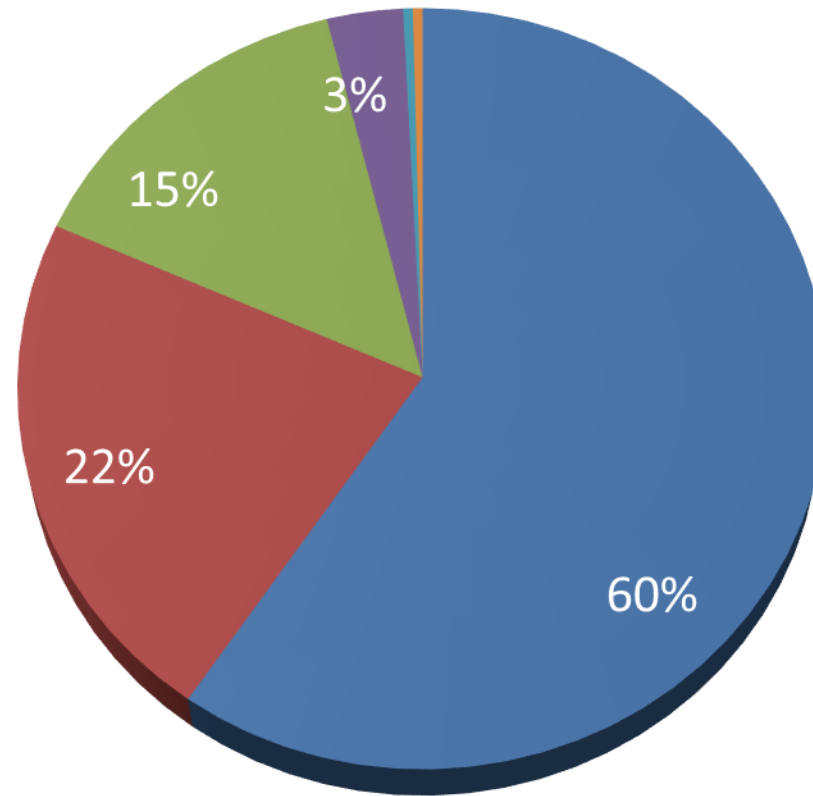
# 1Q23 Revenue Analysis by Payment Model

■ License Fee ■ Running Royalty ■ Maintenance ■ Others

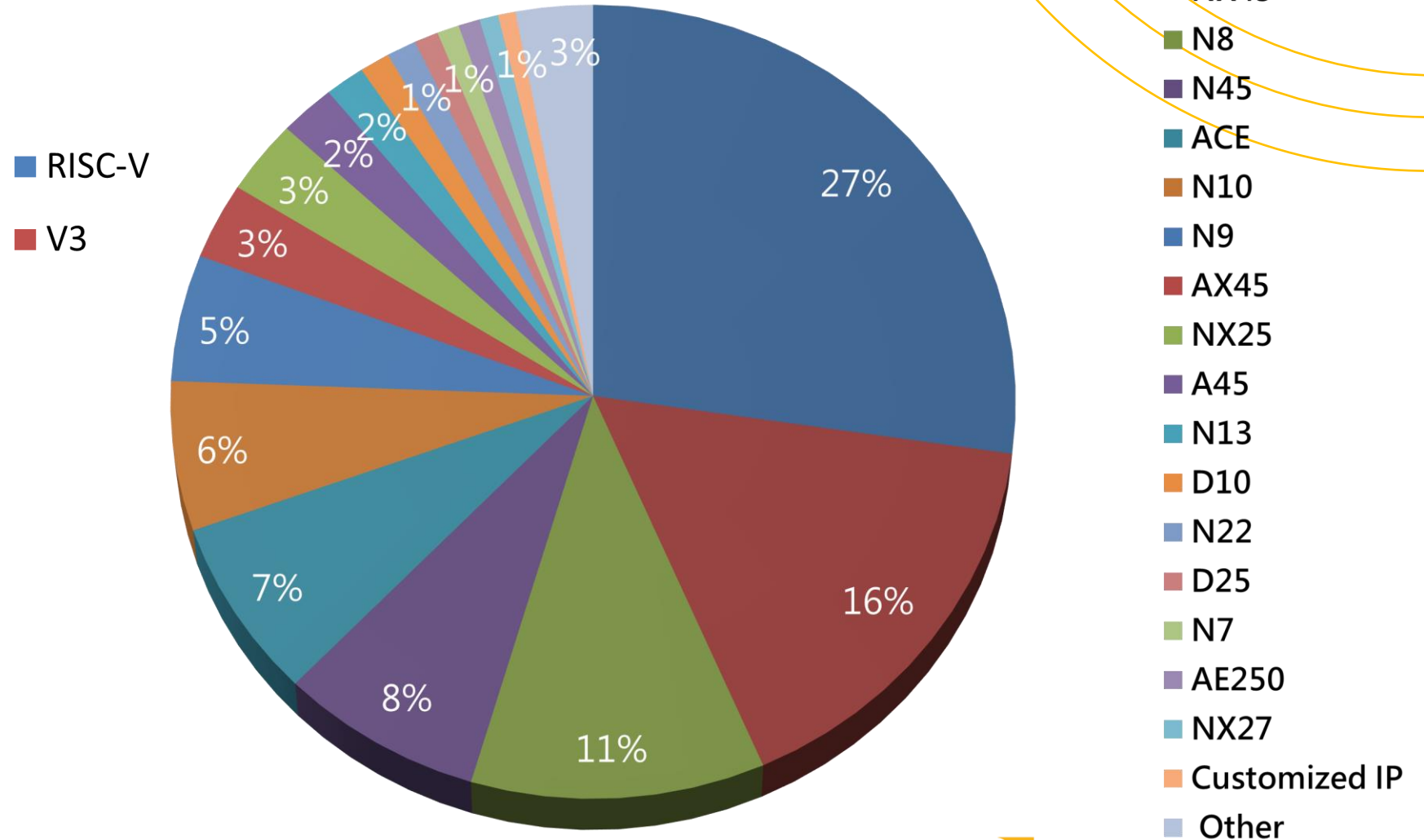
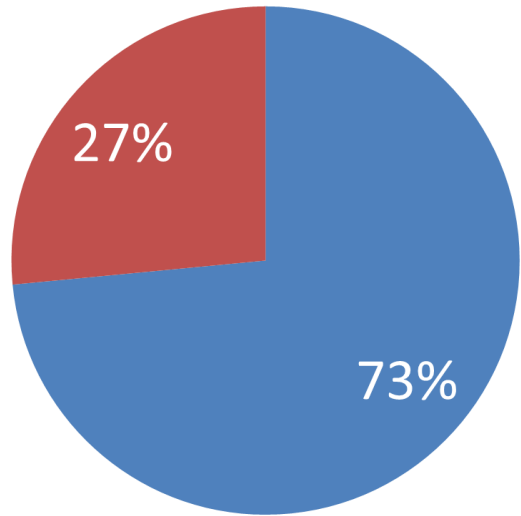


# 1Q23 Revenue Analysis by Region

■ Taiwan ■ USA ■ China ■ Korea ■ Europe ■ Japan

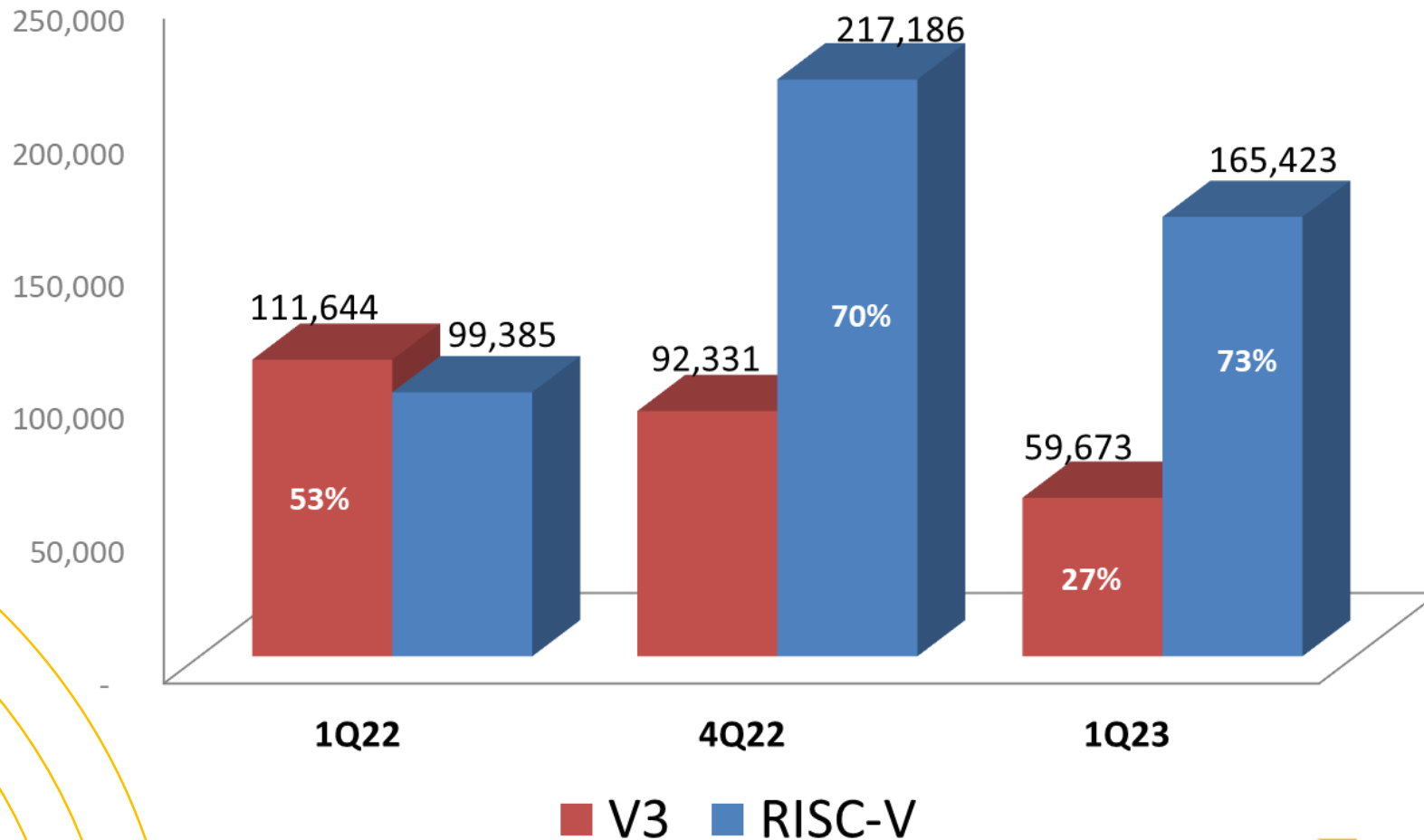


# 1Q23 Revenue Analysis by Product



# 1Q23 Revenue Analysis - RISC-V

(NT\$ thousands)





# Product Applications

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<http://www.andestech.com>





# V5 Adoptions: From MCU to Datacenters

## ❖ Edge to Cloud

- ADAS
- AIoT
- Blockchain
- FPGA
- MCU
- Multimedia
- Security
- Wireless (BT/WiFi)
- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

## ❖ 40nm to 3nm

## ❖ Many in AI





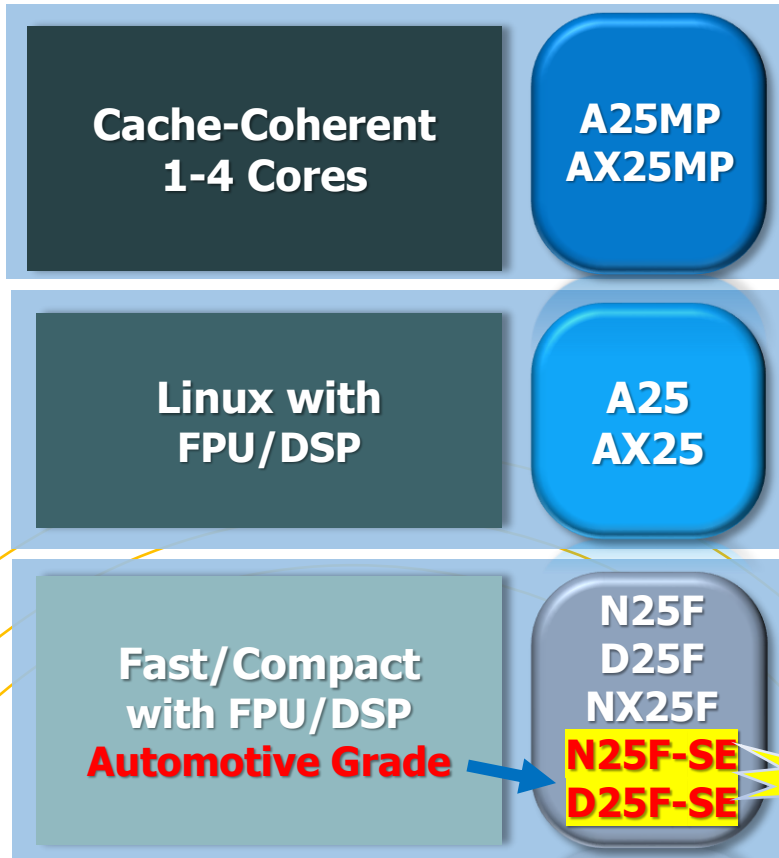


# New Products and Ecosystems

<http://www.andestech.com> 

# Andes RISC-V Product Roadmap

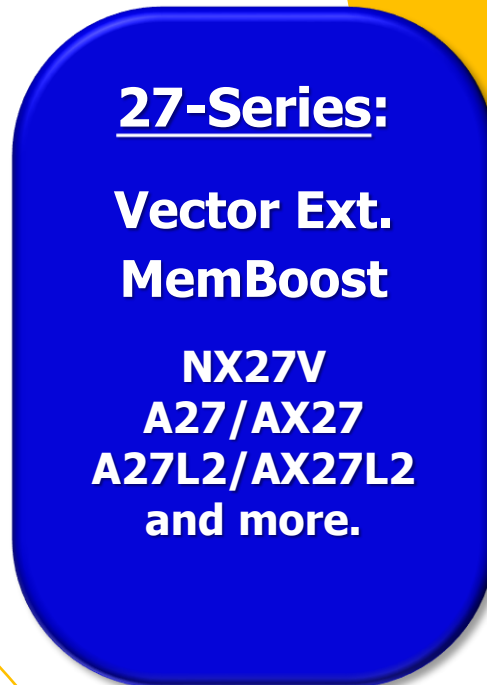
RV32/RV64



5-stage (1.1 GHz)

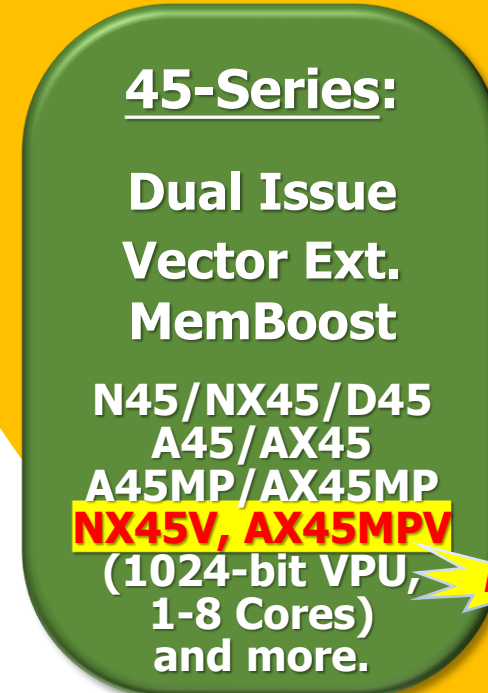


Vector Ext.



5-stage (1.1 GHz)

Superscalar



8-stage (1.2 GHz)

Out of Order



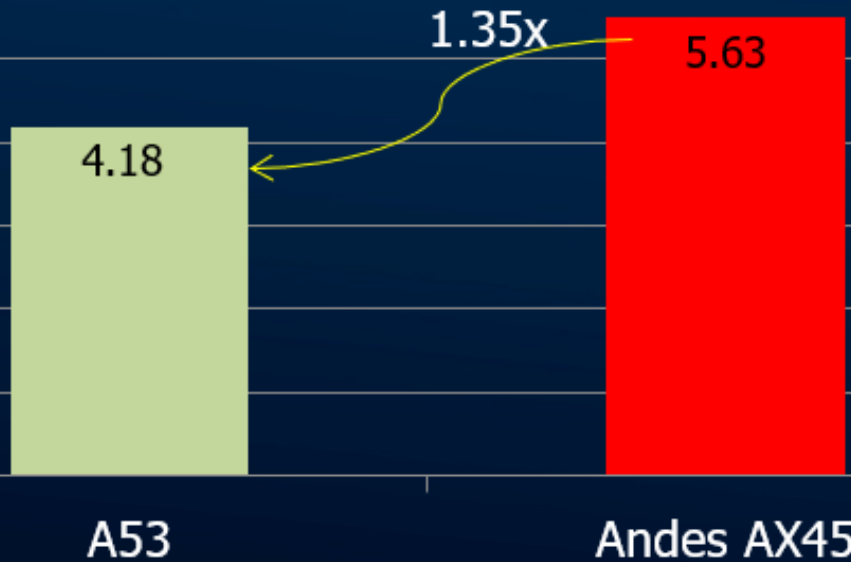
13-stage

Leading positions:

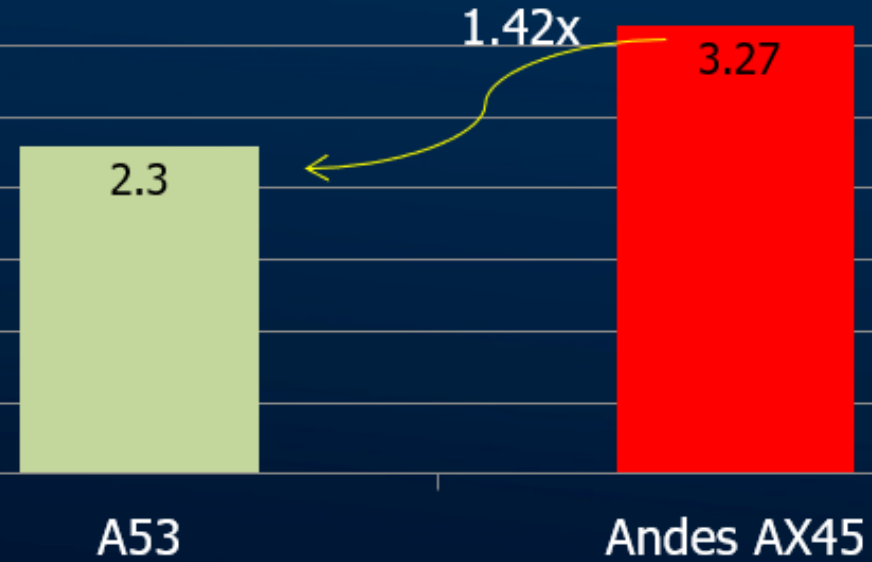
- ❖ The 1st company offering commercial RVP DSP CPU
- ❖ The 1st company offering the most updated spec of commercial RVV vector processor
- ❖ The 1st RISC-V core certified with ISO 26262 full compliance
- ❖ Tools for RISC-V custom extension: ACE

# AX45 Can Do More (vs. 64bit A-series)

Coremark/MHz



Dhrystone/MHz



## ■ A53

- 8-stage In-Order Dual Issue
- **Widely adopted by industries in many applications**

## ■ AX45

- 8-stage In-Order Dual Issue
- **Performance is better!**
  - Coremark/MHz: 1.35x
  - Dhrystone/MHz: 1.42x

# Target Applications for 27, 45, 60-Series

■ AI/Deep Learning

■ AR/VR

■ 5G



■ Video Surveillance

■ ADAS



■ Networking



■ V2X (Vehicle to Everything)



■ IVI (In-Vehicle-Infotainment)



■ Storage



*Metaverse, HPC and more...*

# The Andes AX60 Processor Series



## ■ A new generation of AndesCore™

- Advanced Performance 13-stage Out-of-Order Superscalar Multicore
- Latest RISC-V Architecture
- Supported by Andes Long-term Roadmap
  - AX65 as the first member of the AX60 series
  - More products based on the AX60 micro-architecture planned, including for automotive functional safety

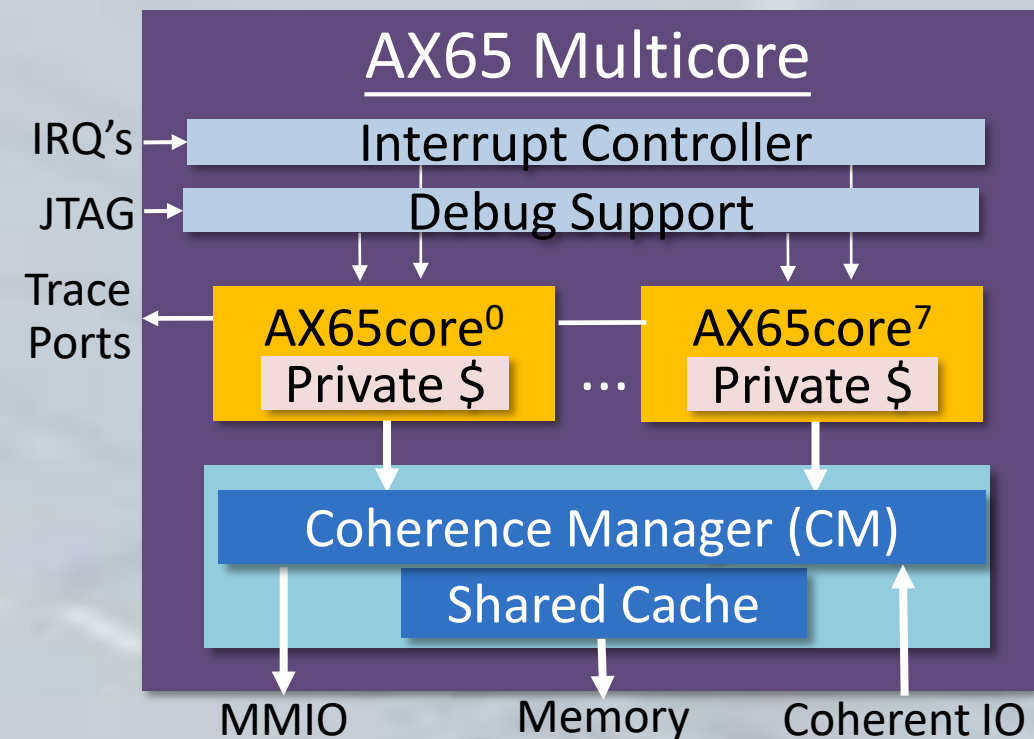
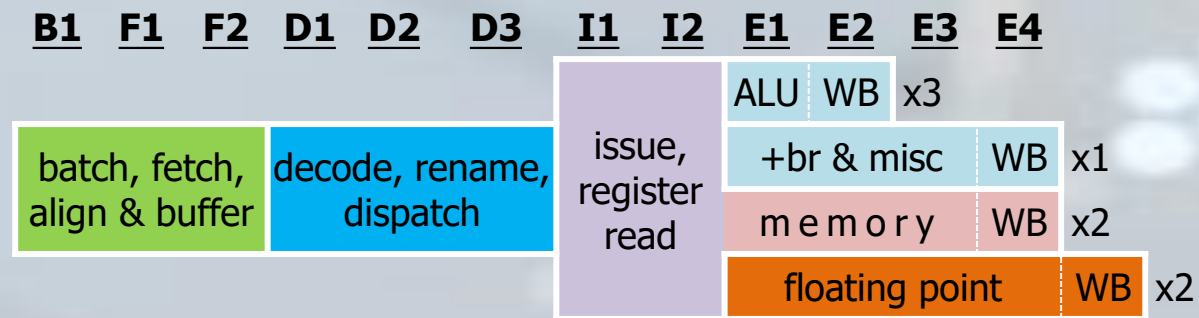
## ■ AndesCore™ AX65

- Offering performance surpassing CA72
- > 2.5 GHz, > 2x per-GHz performance of AX45MP
- Engaging with early customers

# AndesCore AX65: 1<sup>st</sup> Member of AX60-Series



- 64-bit, RV64GCBK
- 8-core Multiprocessor
- 13-stage OoO Pipeline
- 128-entry Reorder Buffer (ROB)
- 4-wide Frontend Decoder
- 8 Execution Pipeline engines
- 2-level Branch Target Buffer (BTB)
- TAGE-L Branch Predictor
- 1024-entry 4-way L2 TLBs
- 64 KB, 4-way Private I/D Caches
- 8 MB, 16-way Shared Cache
- 256-bit AXI4, MMIO and IOCP Buses





# Andes is *Driving* Innovations in Automotive



with Industry's 1<sup>st</sup> RISC-V ISO 26262 Fully Compliant Core, N25F-SE

## In-Cabin Radar



Radio


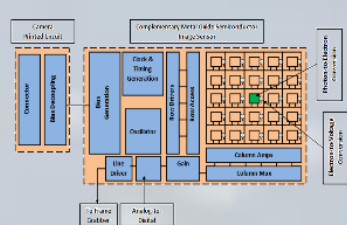
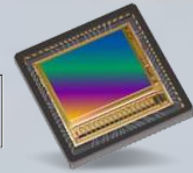
**Radar Subsystem**  
N25F-SE

**Host Controller**  
N25F-SE

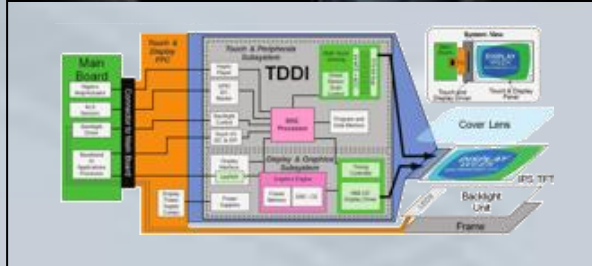
Memory

Peripheral


## CMOS Sensor

## Auto TDDI



## Auto MCU

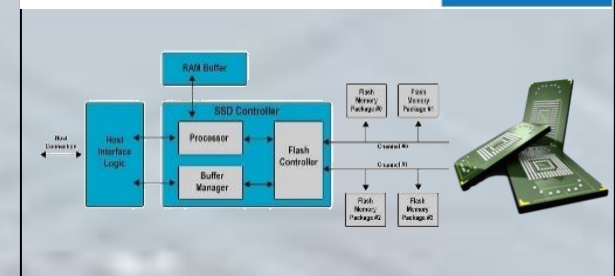



器件	数量	物料号	备注
MCU	1	RISC-V CPU 0	
MCU	1	RISC-V CPU 1	
MCU	1	RISC-V CPU 2	
MCU	1	RISC-V CPU 3	
MCU	1	RISC-V CPU 4	
MCU	1	RISC-V CPU 5	
MCU	1	RISC-V CPU 6	
MCU	1	RISC-V CPU 7	
MCU	1	RISC-V CPU 8	
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MCU	1	RISC-V CPU 10	
MCU	1	RISC-V CPU 11	
MCU	1	RISC-V CPU 12	
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MCU	1	RISC-V CPU 87	
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MCU	1	RISC-V CPU 90	
MCU	1	RISC-V CPU 91	
MCU	1	RISC-V CPU 92	
MCU	1	RISC-V CPU 93	
MCU	1	RISC-V CPU 94	
MCU	1	RISC-V CPU 95	
MCU	1	RISC-V CPU 96	
MCU	1	RISC-V CPU 97	
MCU	1	RISC-V CPU 98	
MCU	1	RISC-V CPU 99	
MCU	1	RISC-V CPU 100	

## Auto Storage

For advanced IVI, ADAS, digital cluster, telematics, and autonomous drive

Factor interface, high capacity for next generation cockpit, and autonomous drive



# Thank You

<http://www.andestech.com>

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# N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor



- ISO 26262 Certification for Development Process: ASIL-D
  - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- ISO-9001 QMS achieved and maintained since 2010
- ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE
  - ISO 26262-2,4,5,8,9
  - Covers all the sections applicable to CPU core