



Andes Technology Corp. Investor Conference Report



Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

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Company Overview

<http://www.andestech.com> 

Andes Highlights

- **Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.**
- **Well-established high technology IPO company**
- **Over 400 people; 80% are engineers.**
- **TSMC OIP Award “Partner of the Year” for New IP (2015)**
- **Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)**
- **AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)**
- **EE Awards - “Taiwan-Product Award” & “Asia-Company Award” (2021)**
- **Top 500 High-Growth Companies Asia-Pacific (2023)**

Andes Mission

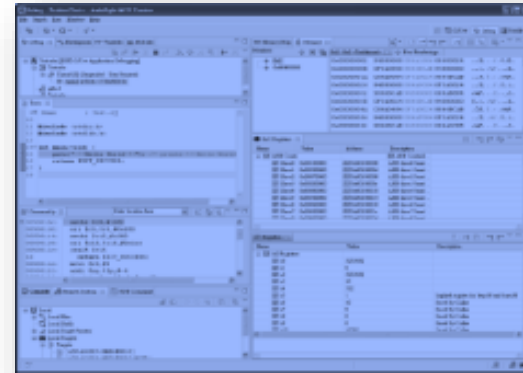
- **Innovate performance-efficient processor solution for low-power SoC**

Emerging Opportunities

- **Smart and Green electronic devices**
- **Cloud Computing and Internet of Things and Machine Learning**

Business Status Overview

- ❖ **300+** commercial licensees
 - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
 - **600+** license agreements signed
- ❖ AndeSight™ IDE:
 - **25,000+** installations
- ❖ Eco-system:
 - **500+** partners
- ❖ **12B+** Accumulative SoC Shipped





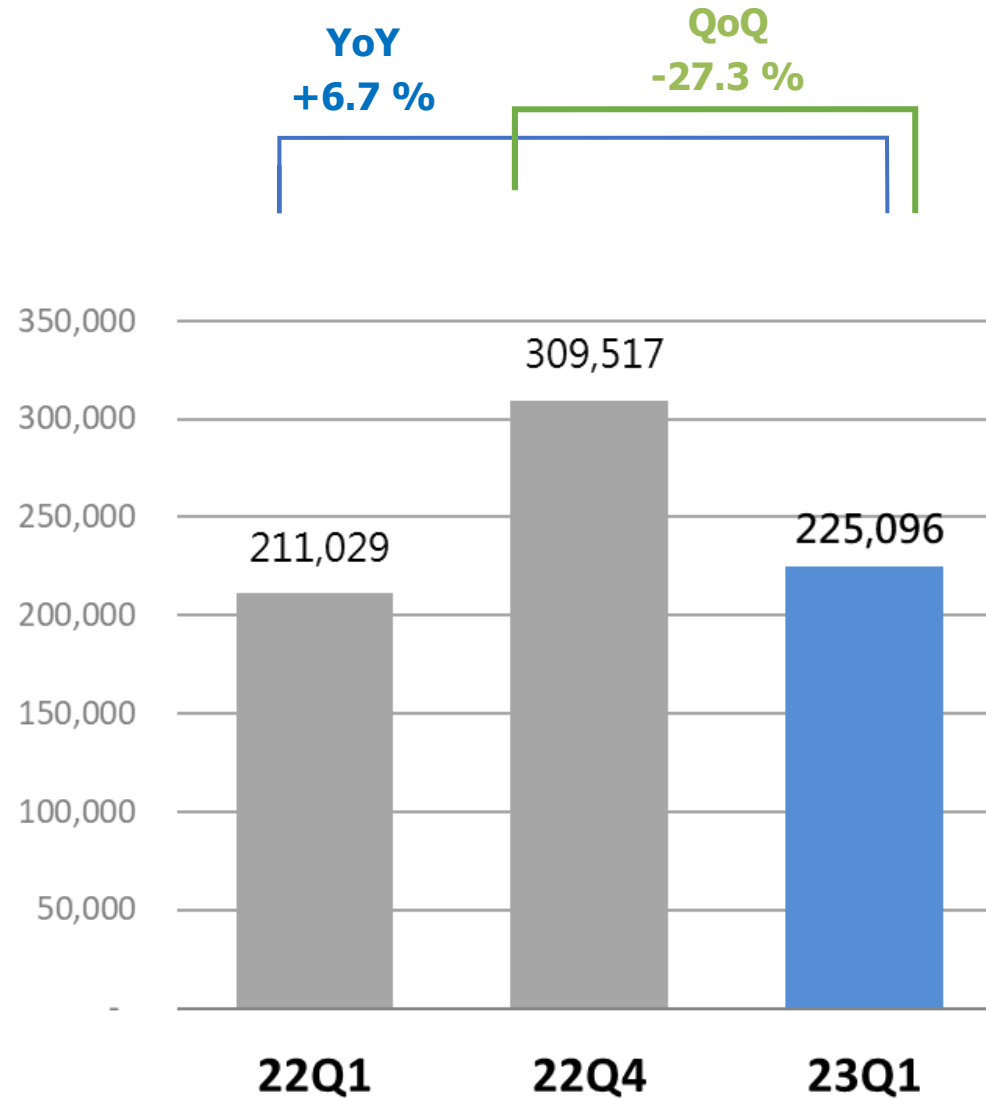
Operation Results

<http://www.andestech.com>



1Q23 Revenue Analysis

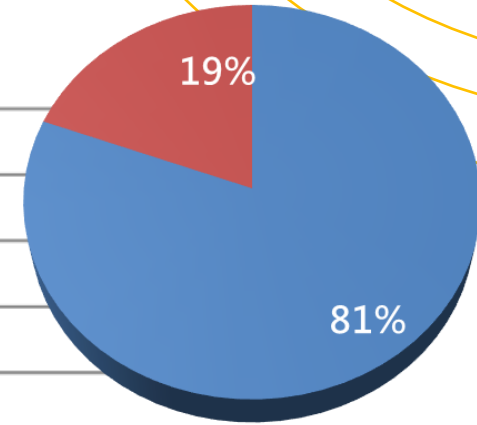
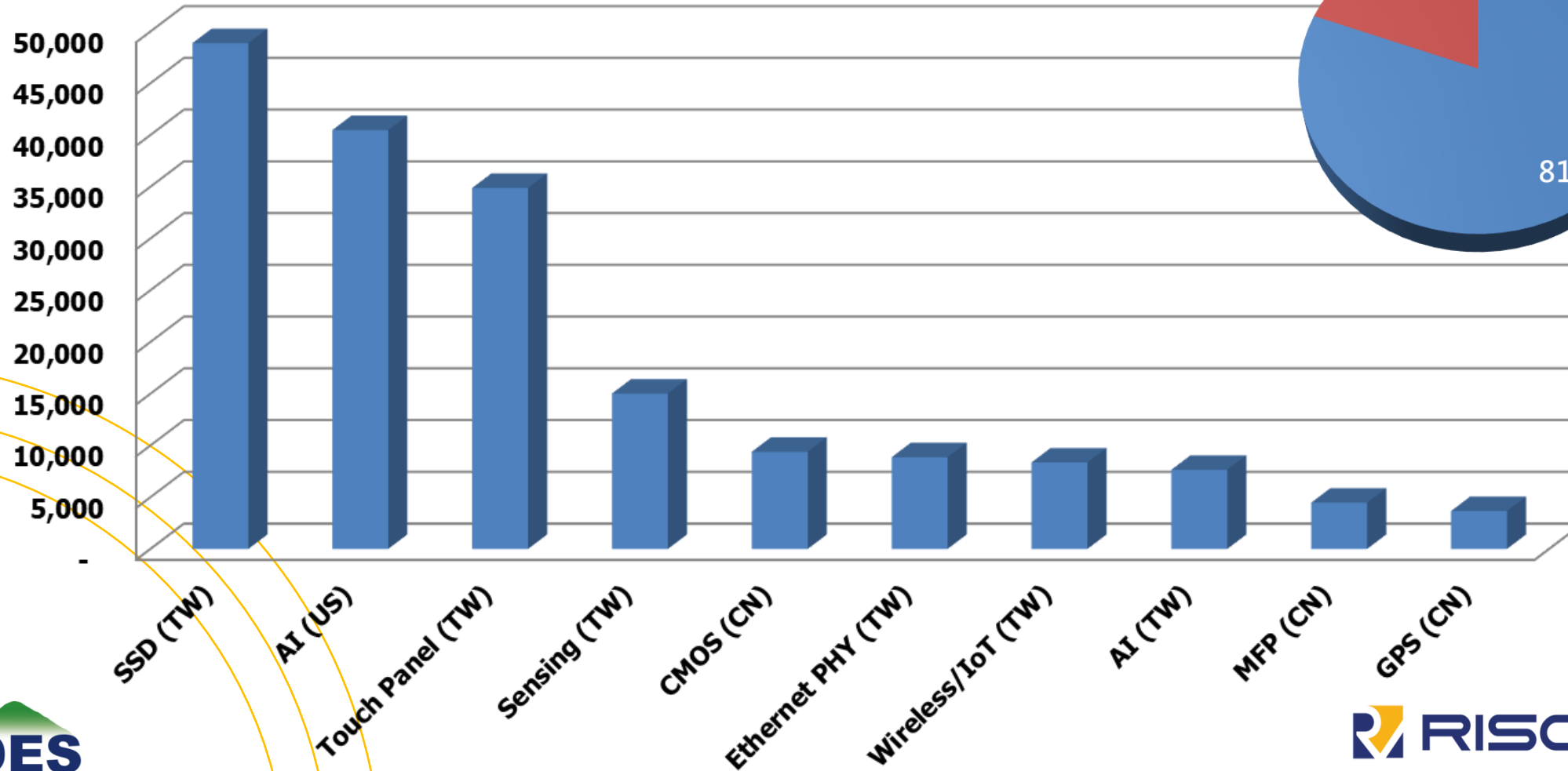
(NT\$ thousands)



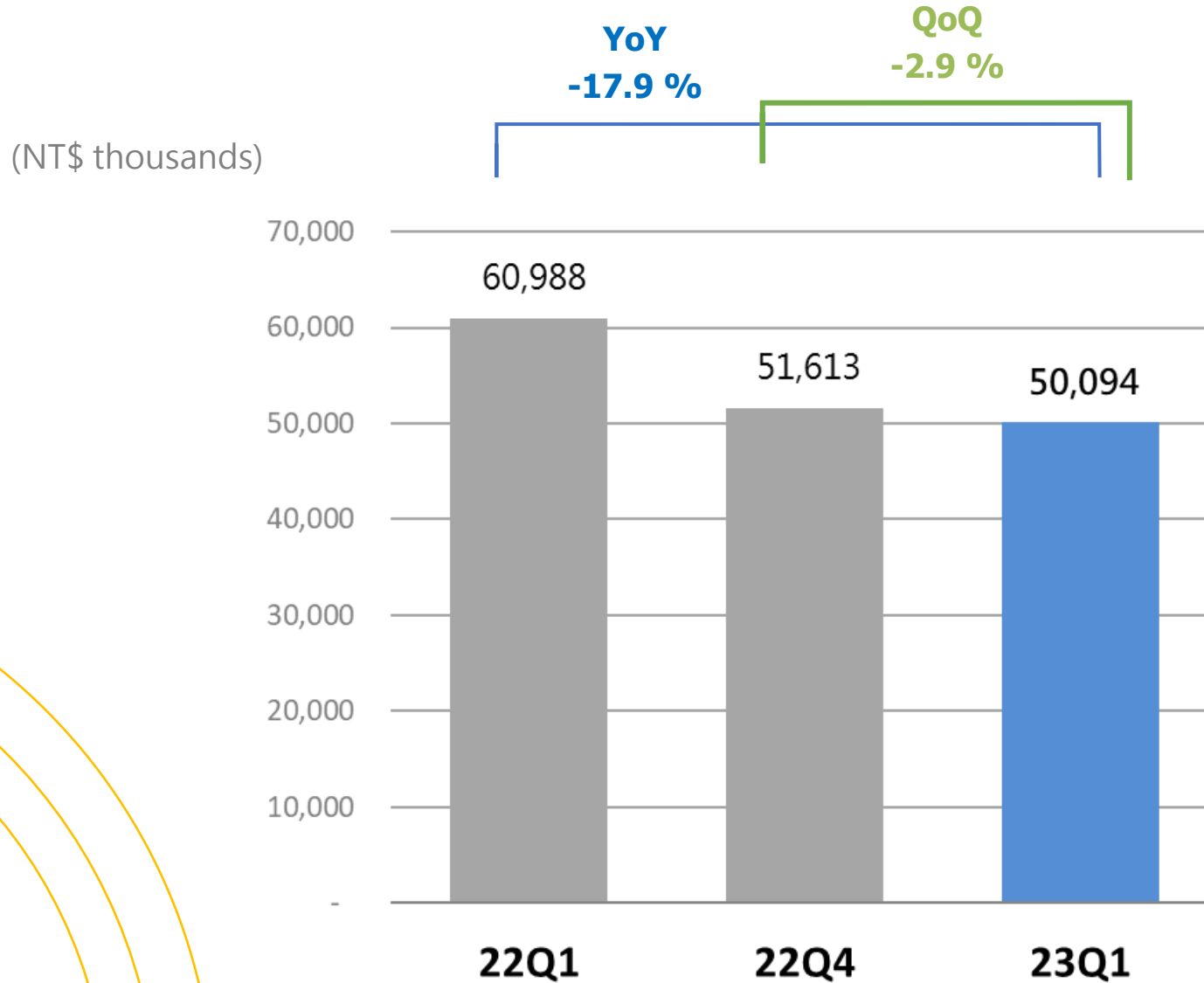
1Q23 Top 10 Customers Analysis by Revenue

(NT\$ thousands)

Top 10 Customer Contributed 81% Revenue



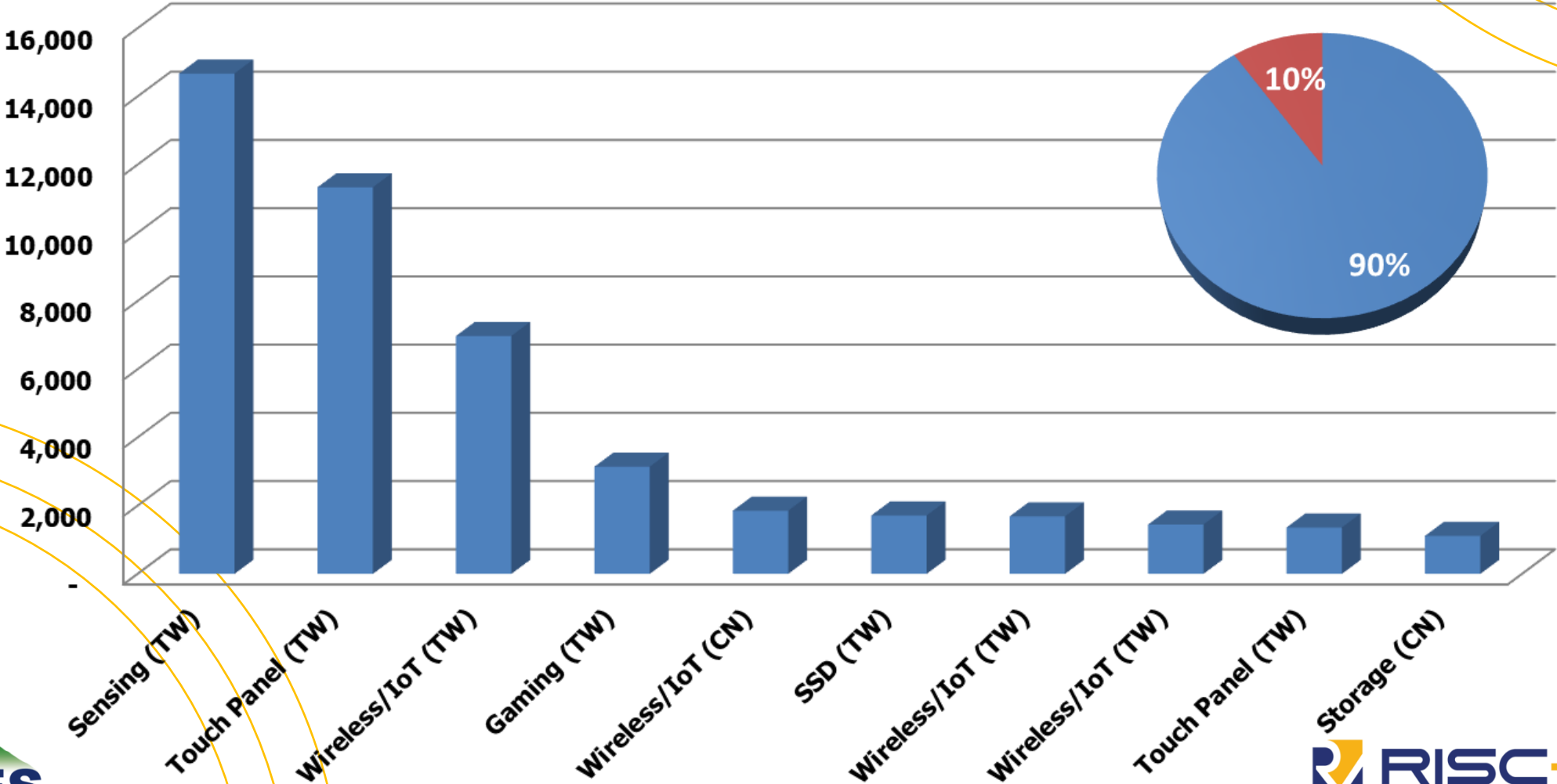
1Q23 Royalty Analysis



1Q23 Top 10 Royalty Contributors Analysis by Application

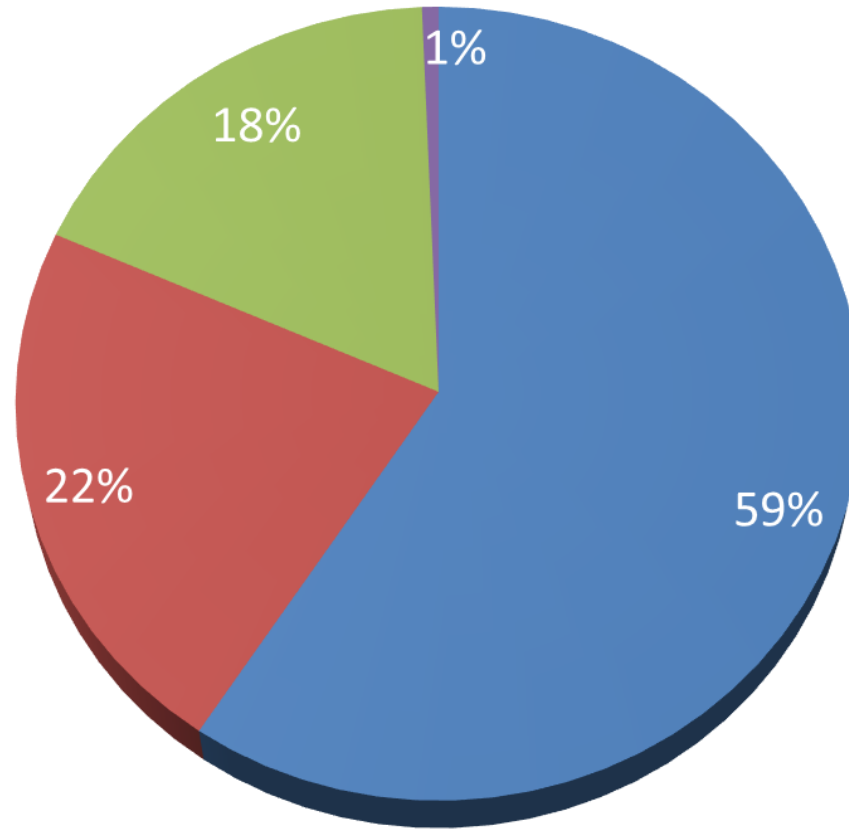
(NT\$ thousands)

Top 10 Royalty Customers
Contribution Analysis: 90%



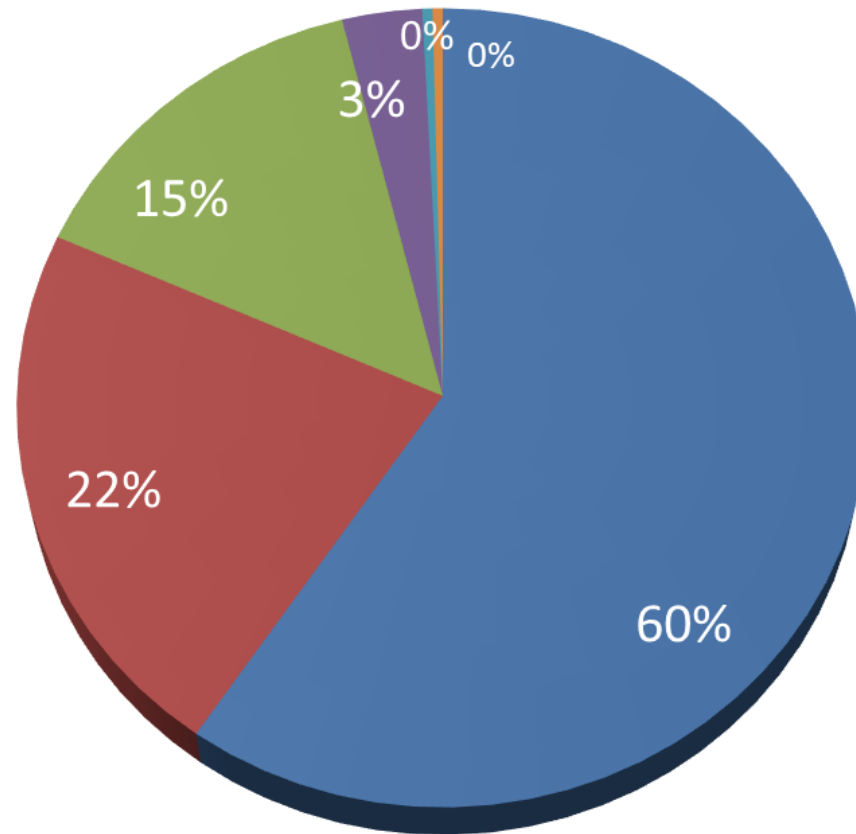
1Q23 Revenue Analysis by Payment Model

■ License Fee ■ Running Royalty ■ Maintenance ■ Others

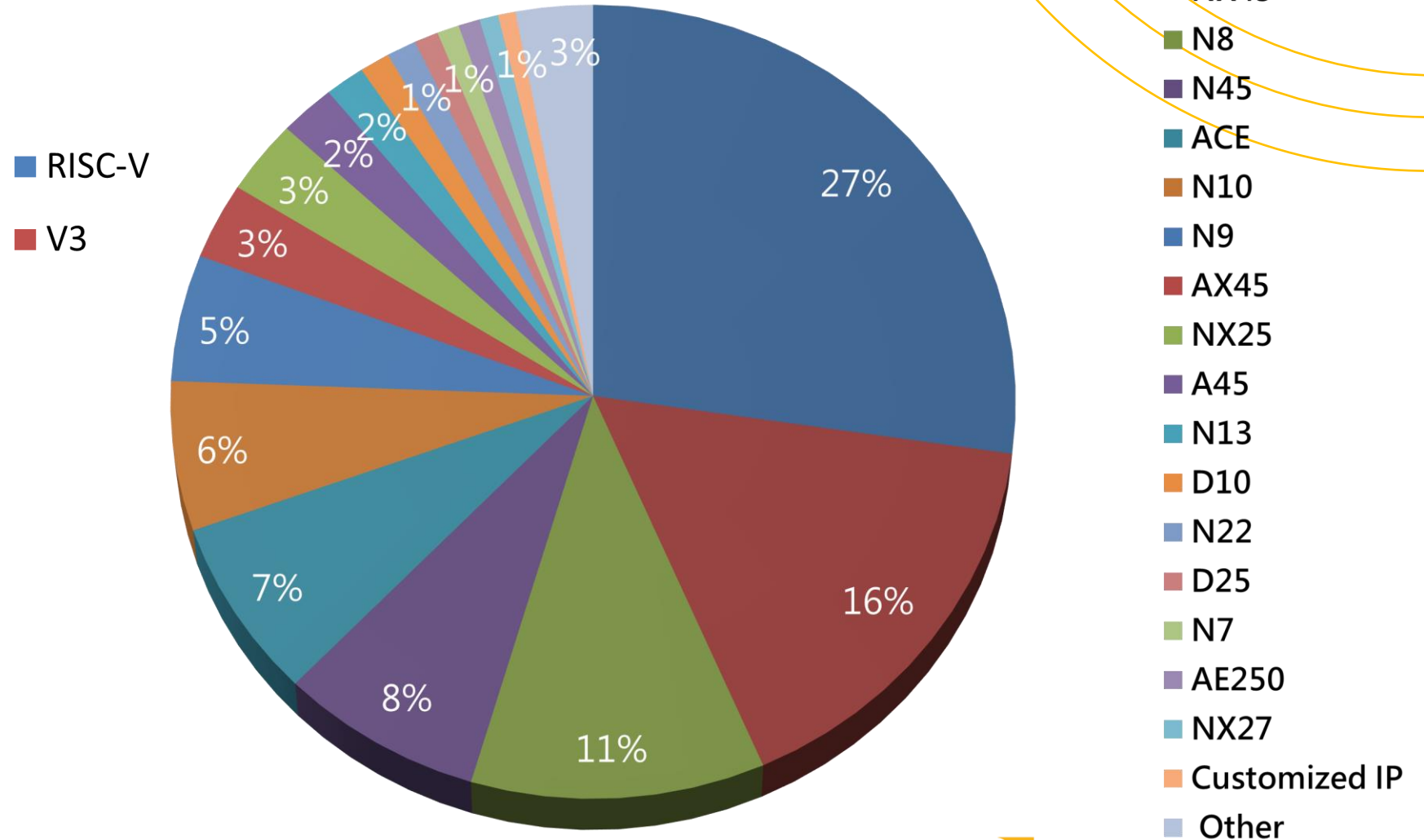
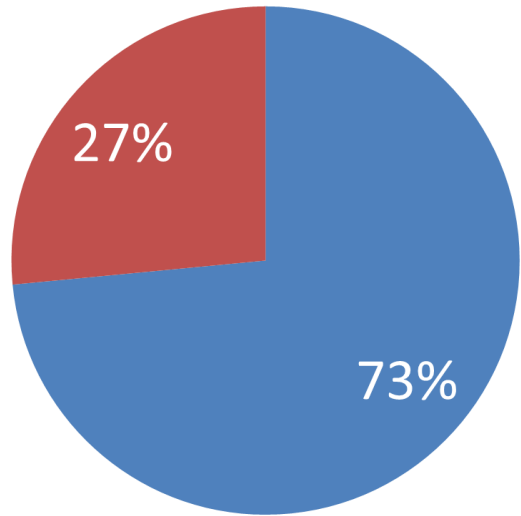


1Q23 Revenue Analysis by Region

■ Taiwan ■ USA ■ China ■ Korea ■ Europe ■ Japan

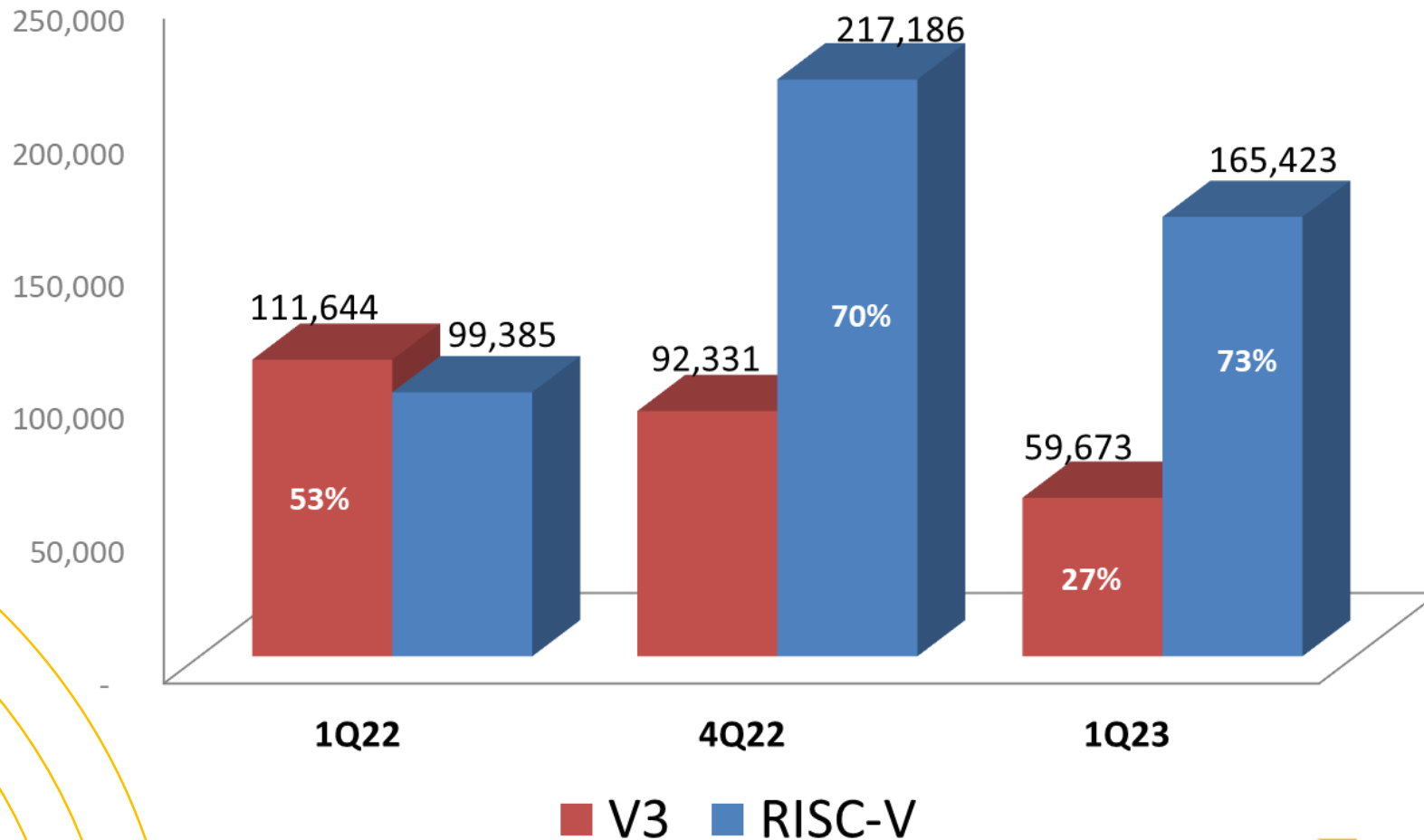


1Q23 Revenue Analysis by Product



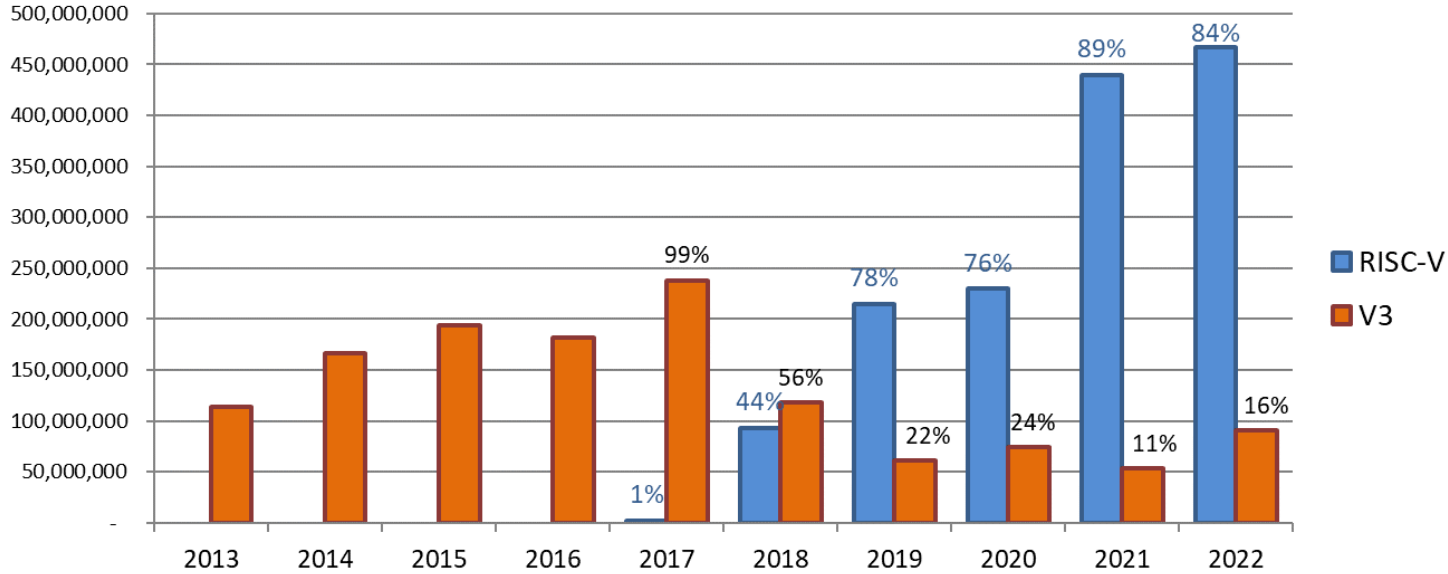
1Q23 Revenue Analysis - RISC-V

(NT\$ thousands)

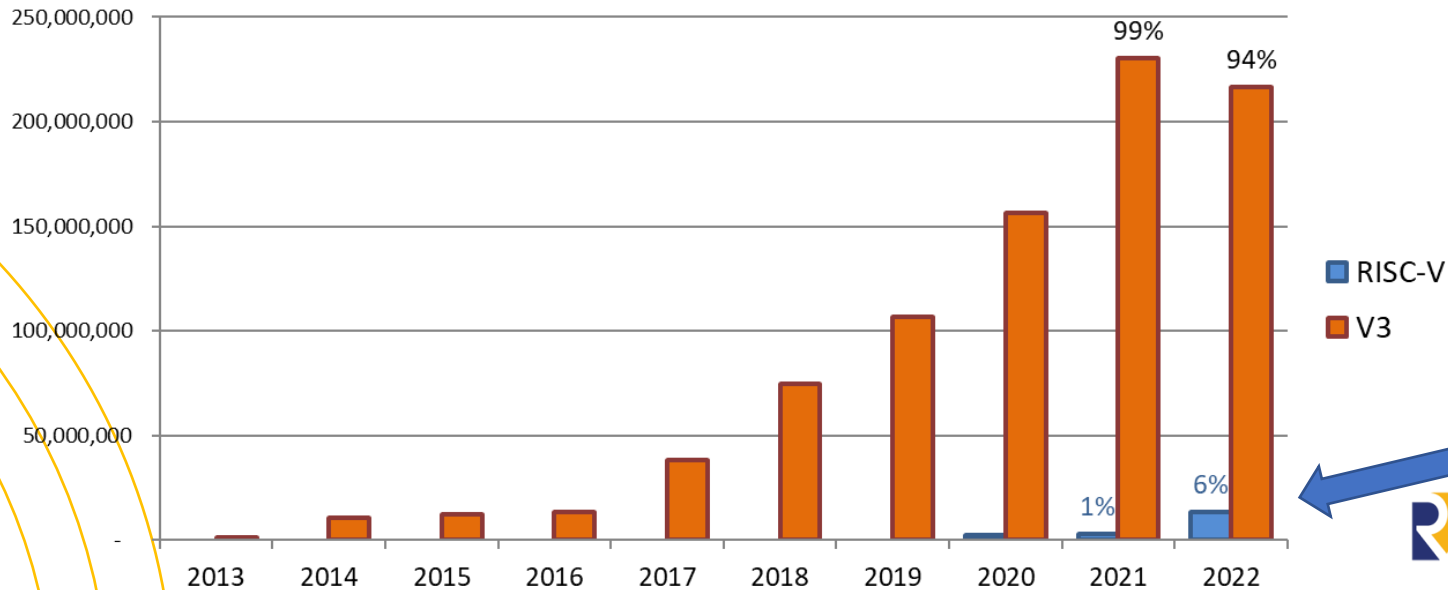


Historical Revenue Analysis

(NT\$)



License



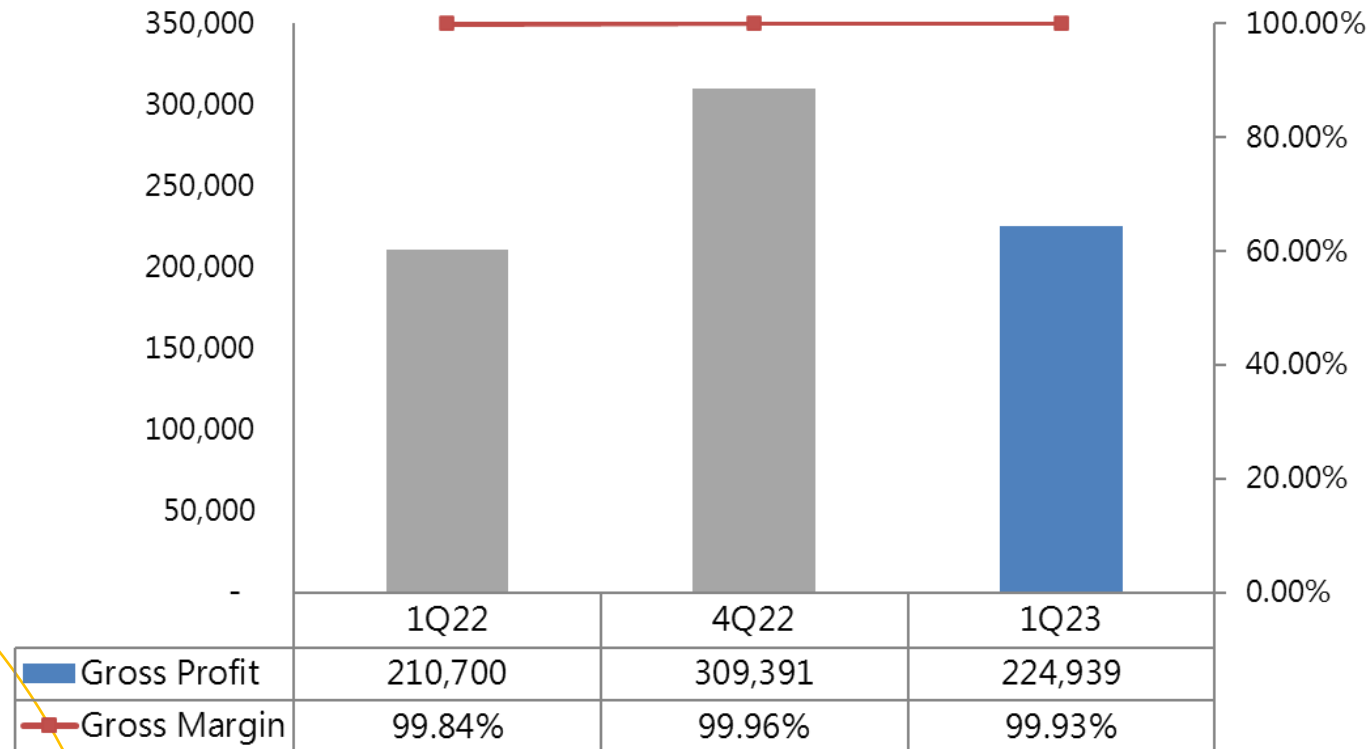
Royalty

RISC-V 2022: 6%

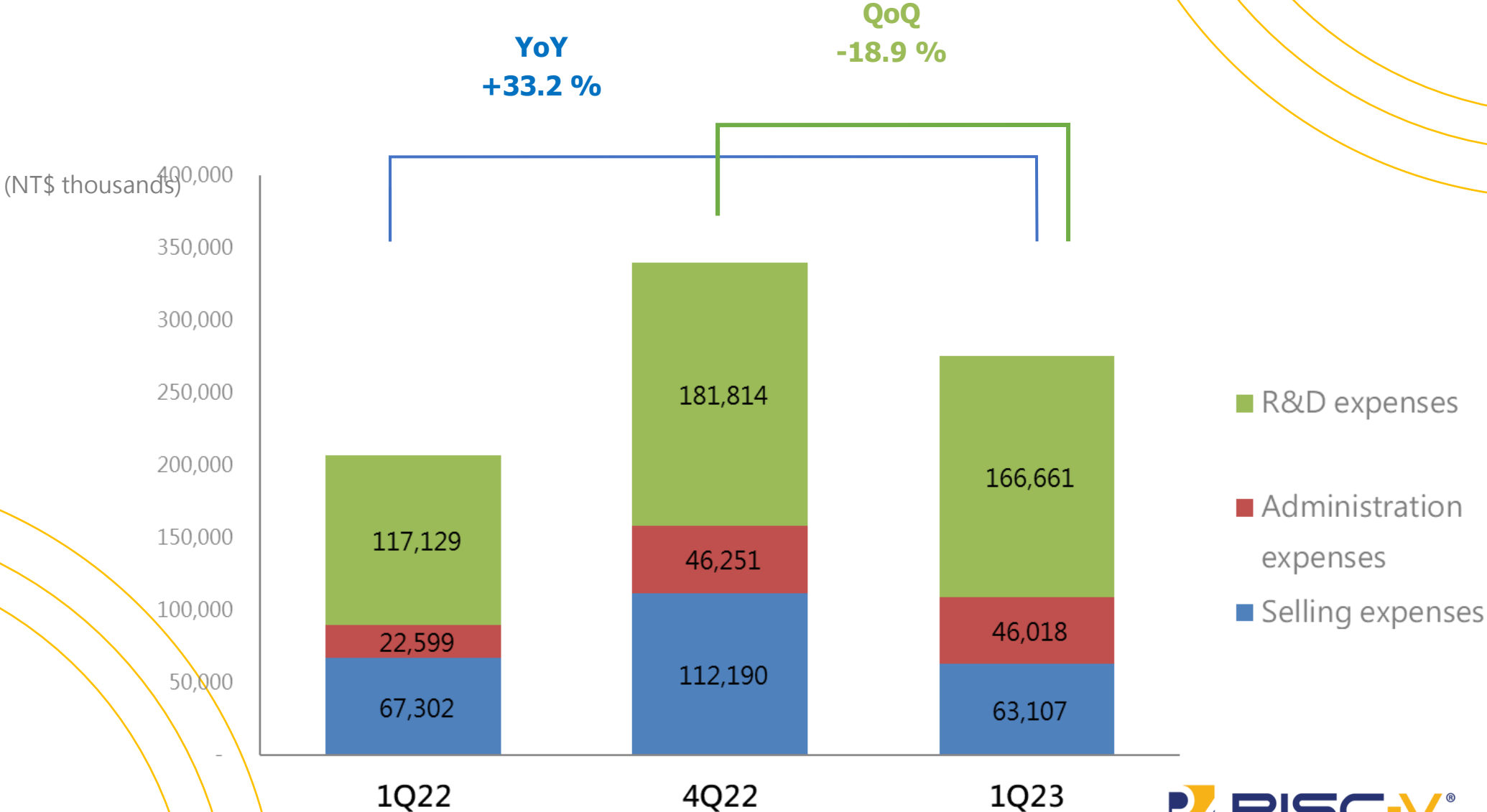


1Q23 Consolidated Gross Margin

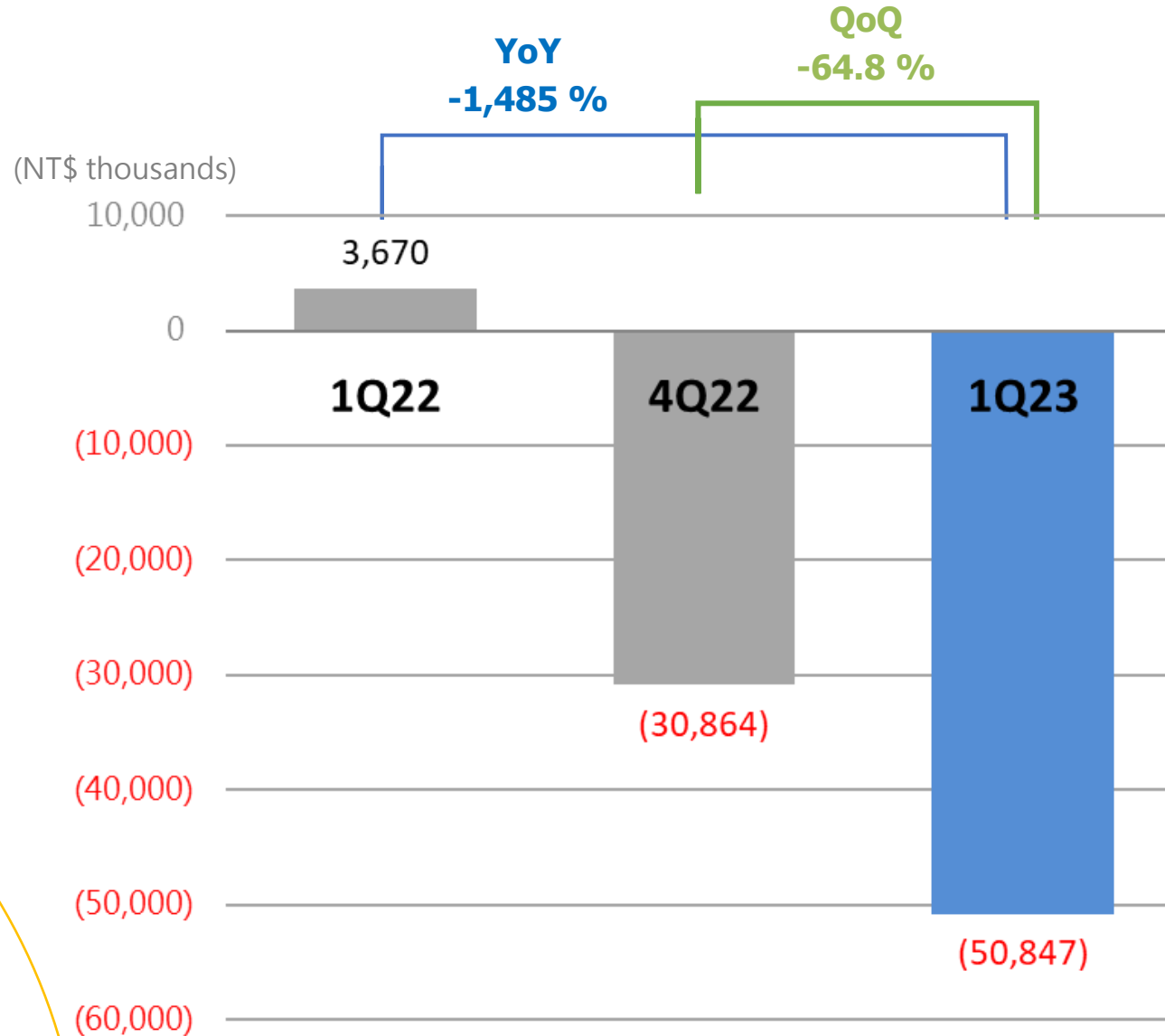
(NT\$ thousands)



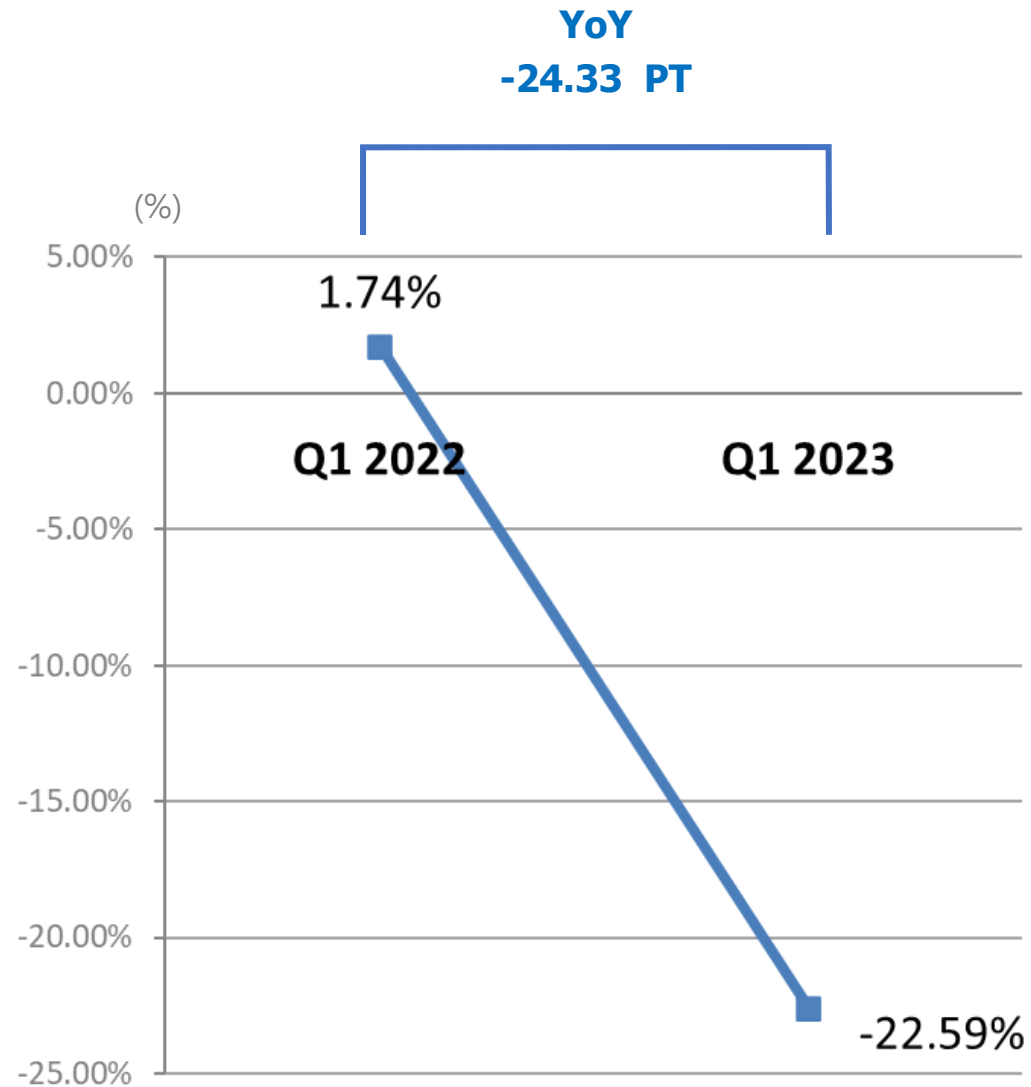
1Q23 Consolidated Operating Expenses



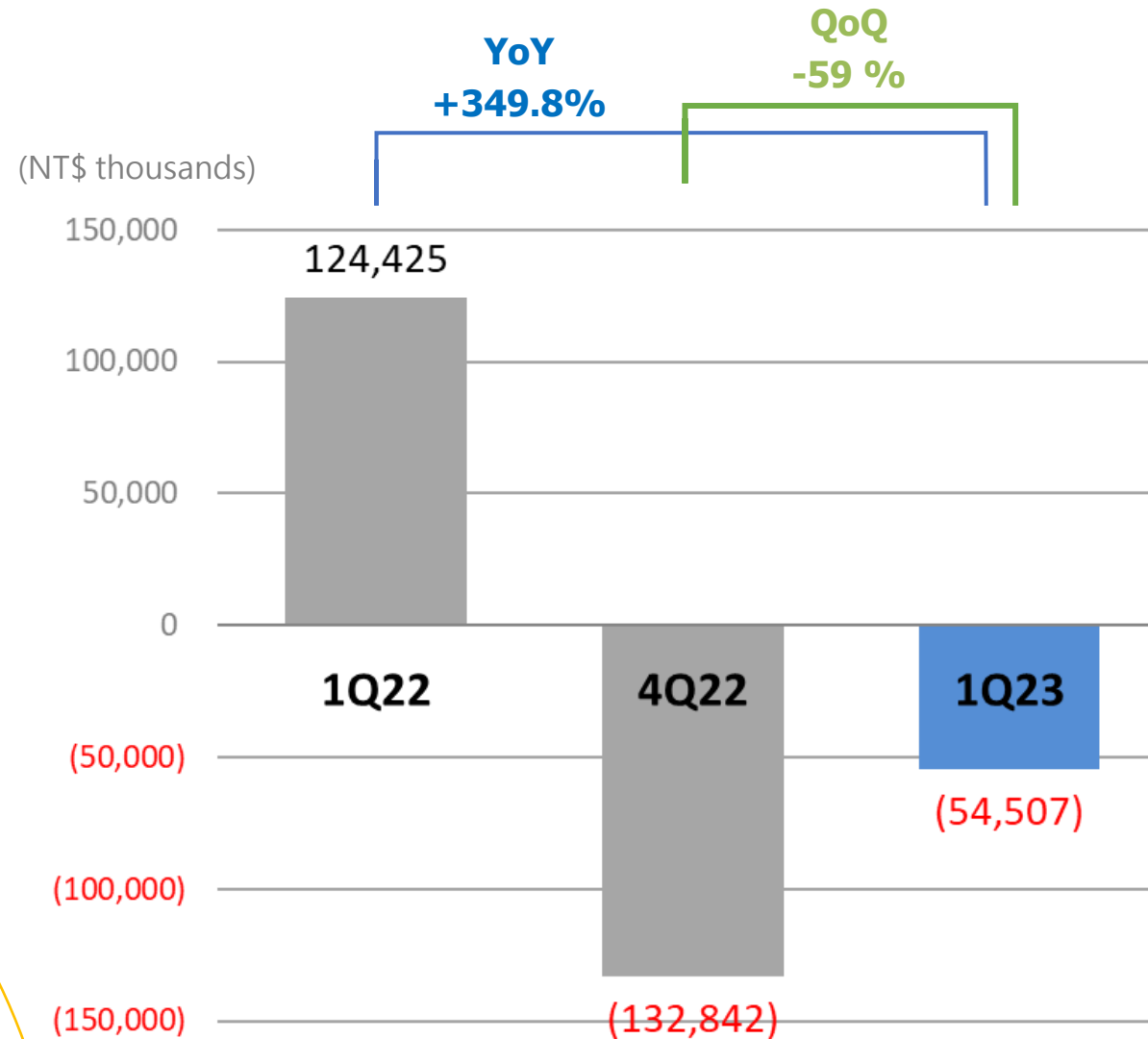
1Q23 Consolidated Operating Income



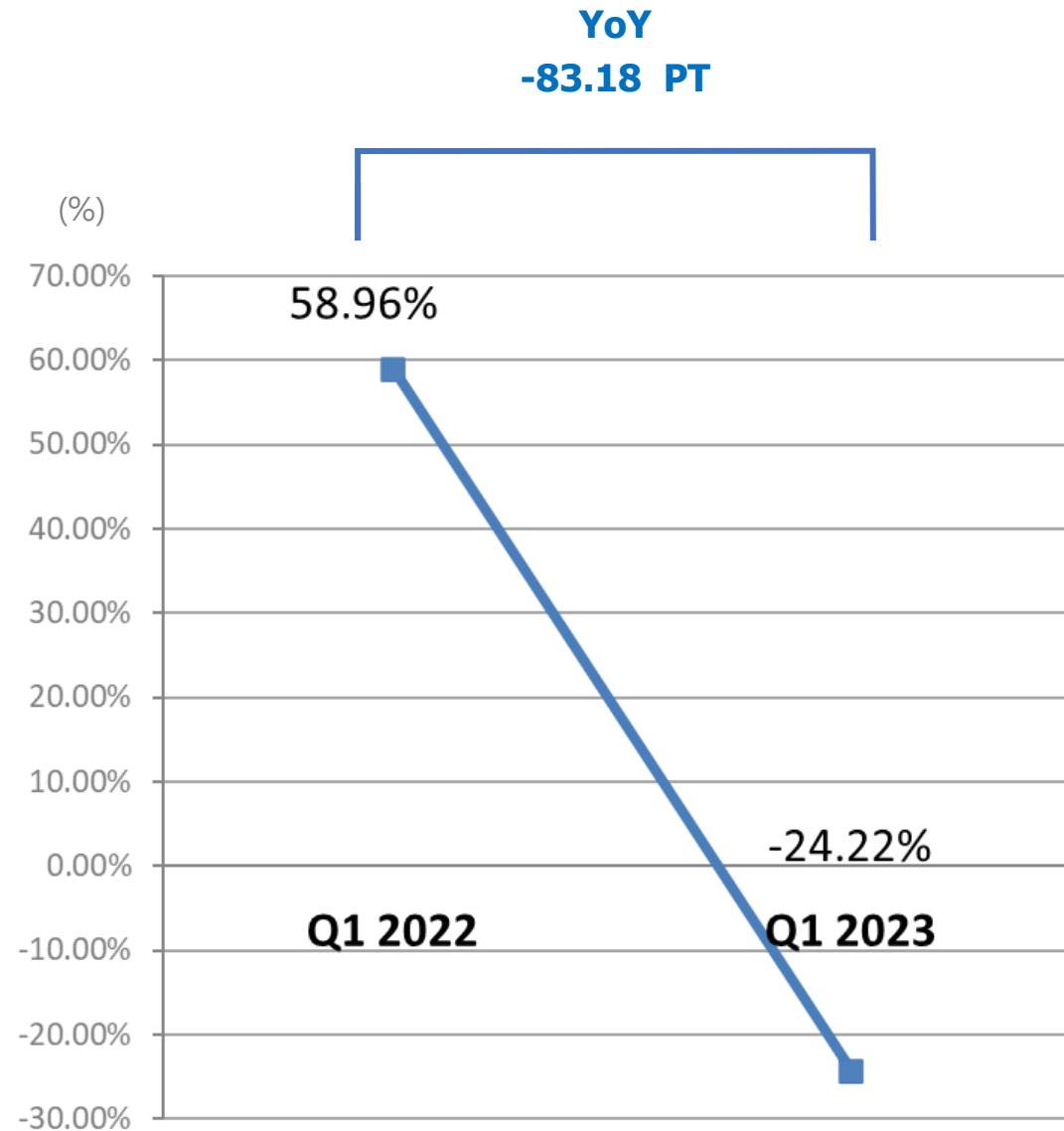
1Q23 Consolidated Operating Margin



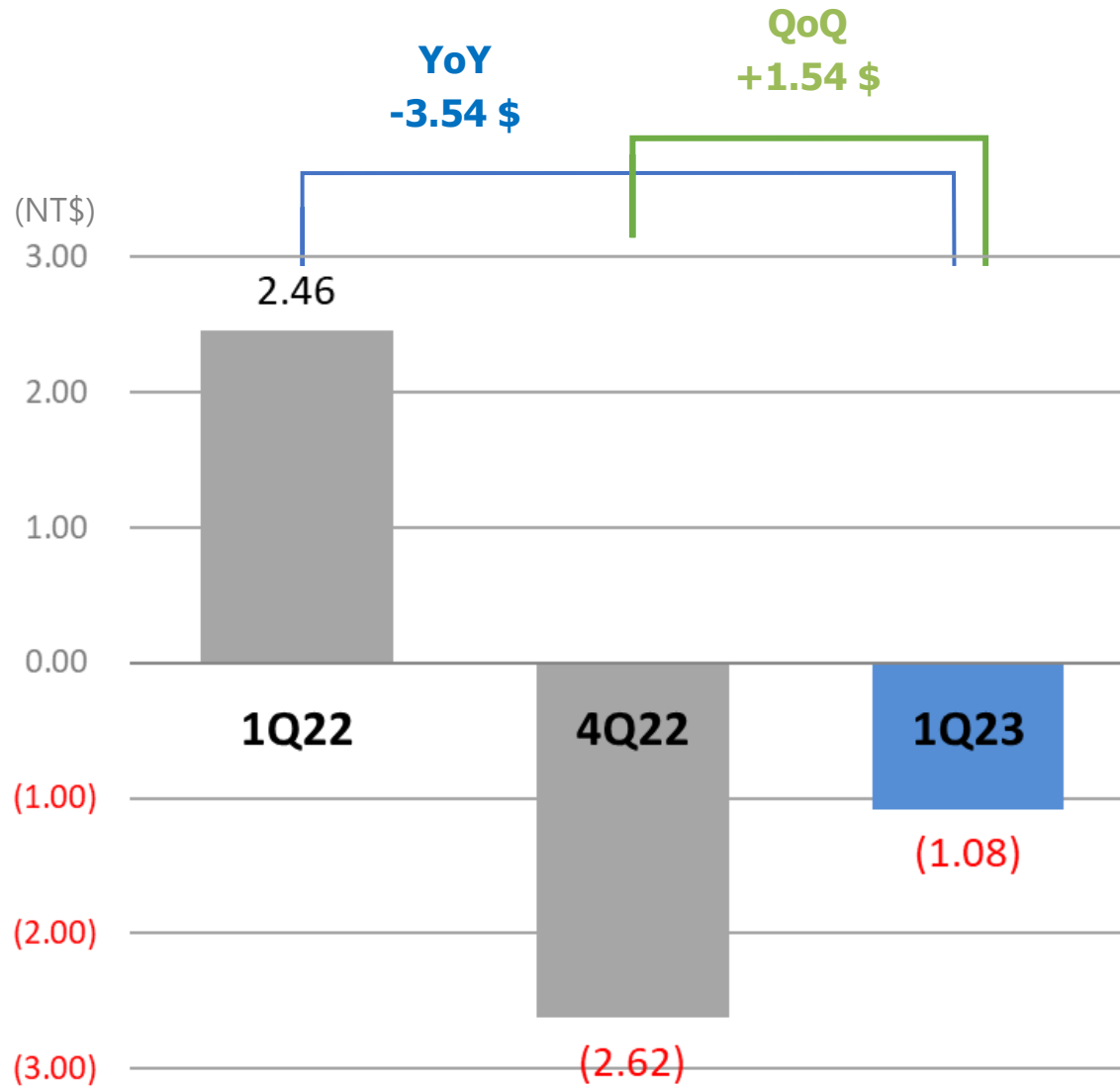
1Q23 Consolidated Net Income



1Q23 Consolidated Net Profit Margin



1Q23 Consolidated EPS





Product Applications

<http://www.andestech.com>



V5 Adoption Examples: From MCU to Datacenters

❖ Edge to Cloud

- ADAS
- AIoT
- Blockchain
- FPGA
- MCU
- Multimedia
- Security
- Wireless (BT/WiFi)
- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

❖ 40nm to 3nm

❖ Many in AI



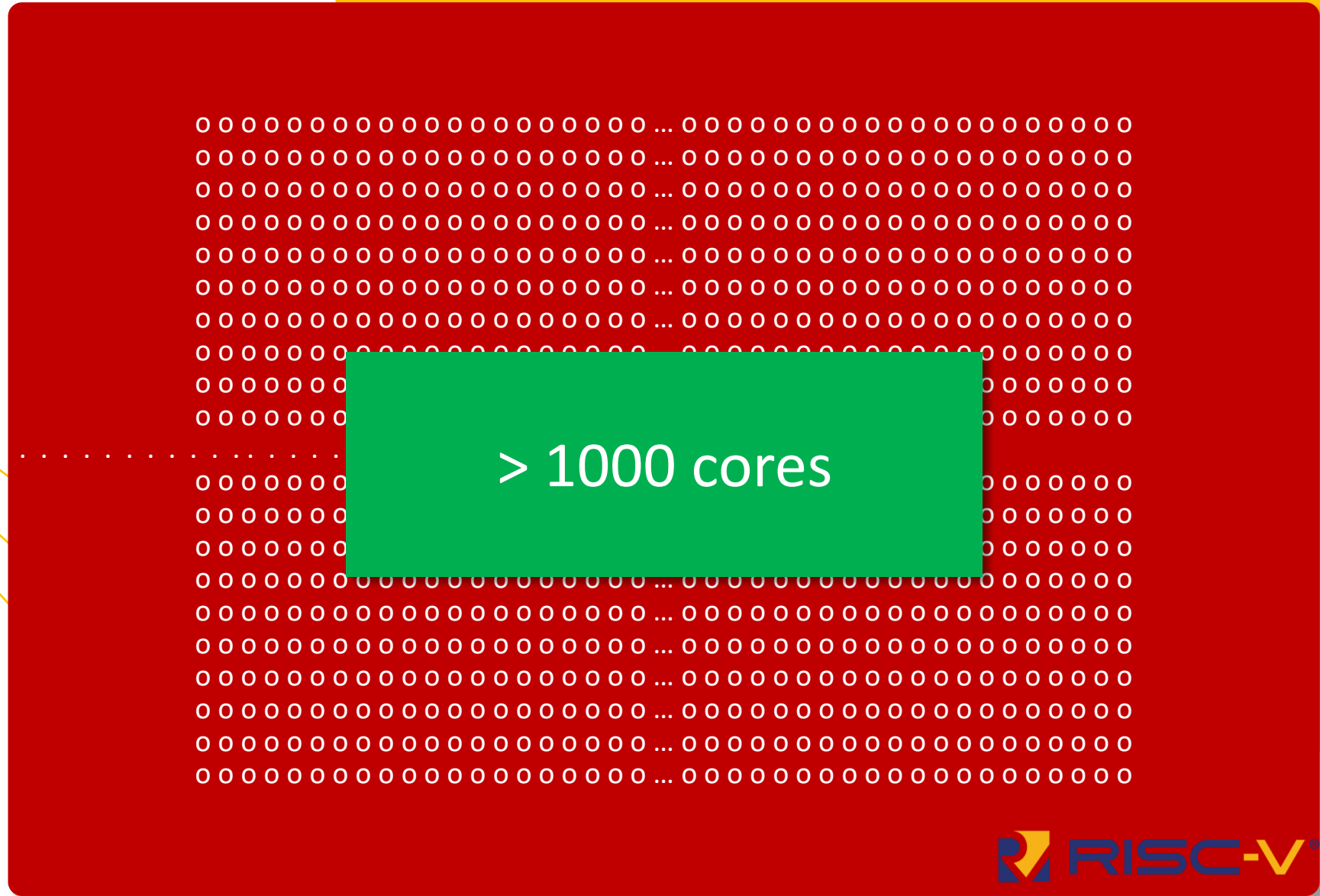
Andes RISC-V Cores Adopted in SoC

○ single core

○○○○○
○○○ 2-8 cores

○○○○○○○○○
> 30 cores
○○○○○○○○○

○○○○○○○○○○○○○○○○○○○○
> 100 cores
○○○○○○○○○○○○○○○○○○○○
○○○○○○○○○○○○○○○○○○○○
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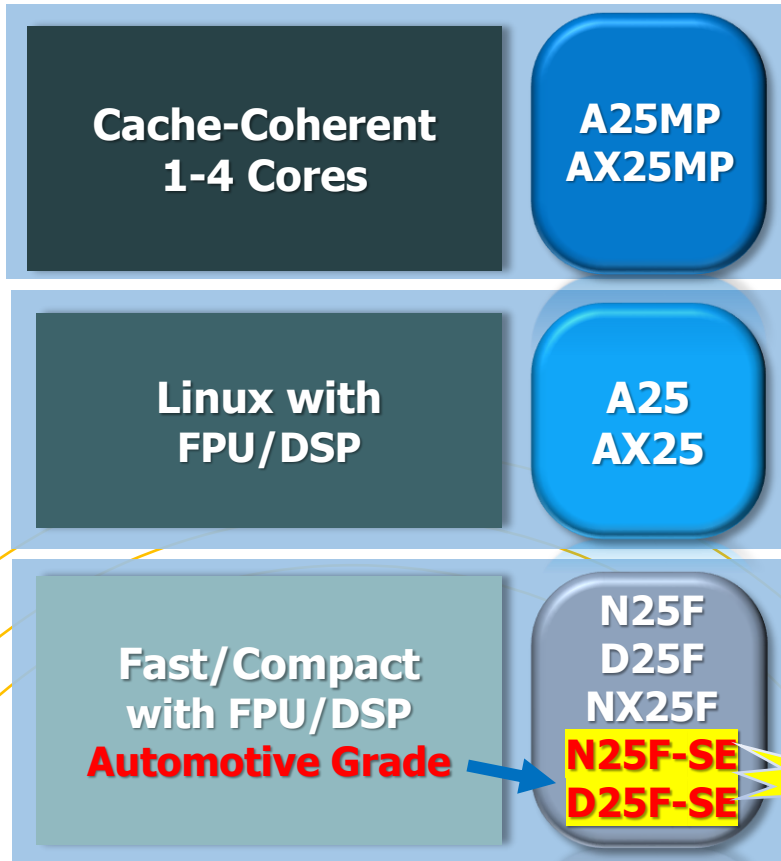


New Products and Ecosystems

<http://www.andestech.com> 

Andes RISC-V Product Roadmap

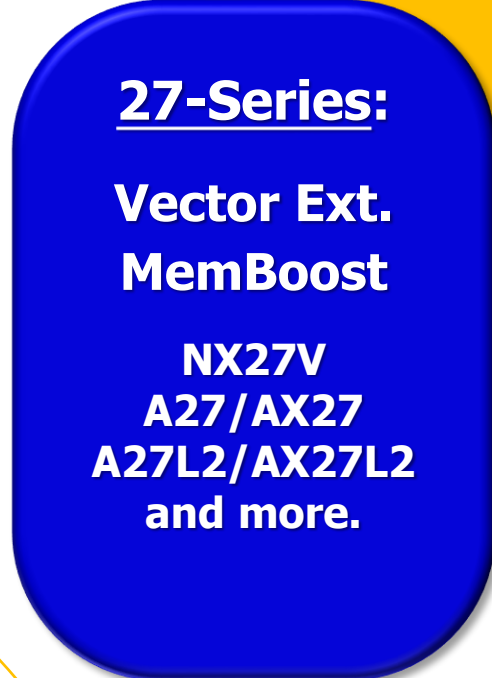
RV32/RV64



5-stage (1.1 GHz)

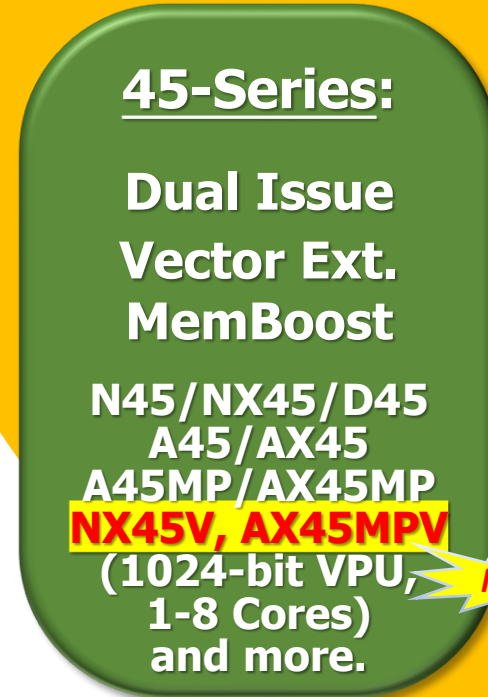


Vector Ext.



5-stage (1.1 GHz)

Superscalar



8-stage (1.2 GHz)

Out of Order



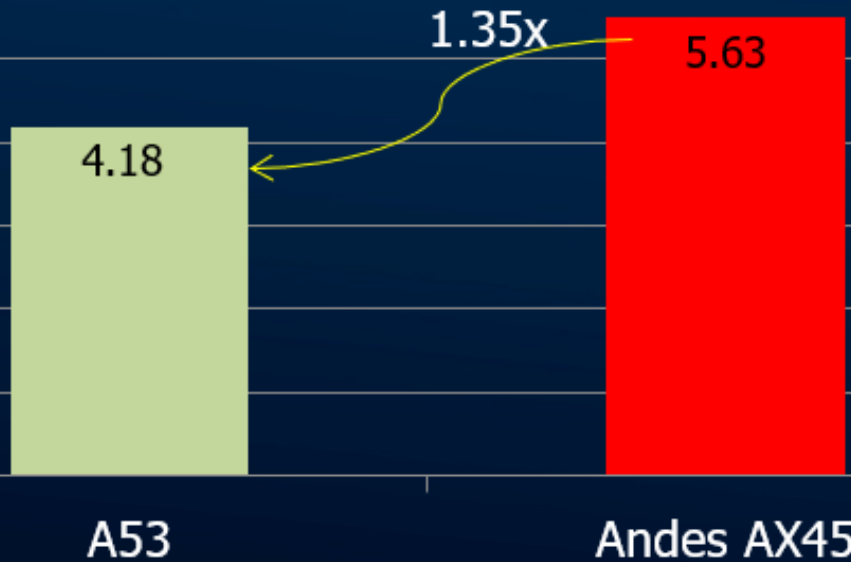
13-stage

Leading positions:

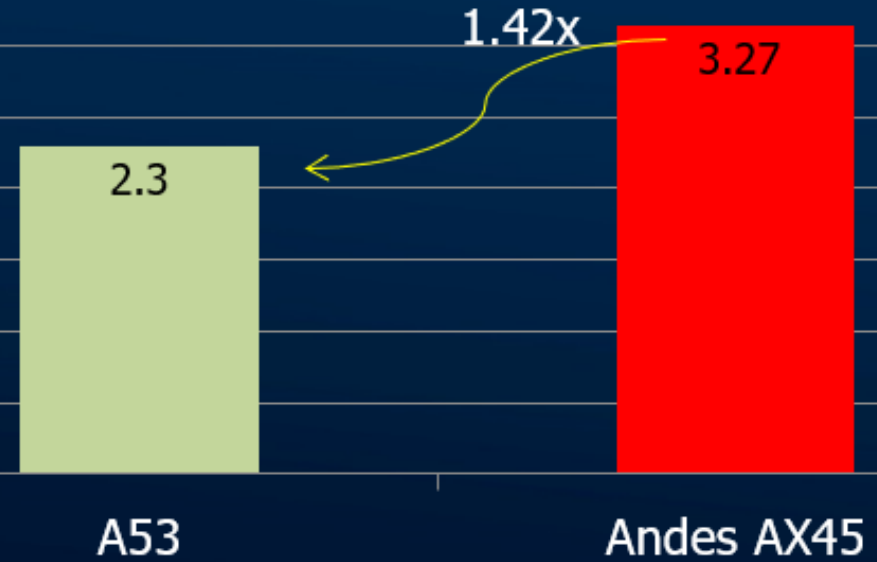
- ❖ The 1st company offering commercial RVP DSP CPU
- ❖ The 1st company offering the most updated spec of commercial RVV vector processor
- ❖ The 1st RISC-V core certified with ISO 26262 full compliance
- ❖ Tools for RISC-V custom extension: ACE

AX45 Can Do More (vs. 64bit A-series)

Coremark/MHz



Dhrystone/MHz



■ A53

- 8-stage In-Order Dual Issue
- **Widely adopted by industries in many applications**

■ AX45

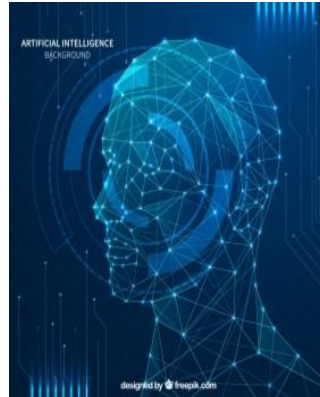
- 8-stage In-Order Dual Issue
- **Performance is better!**
 - Coremark/MHz: 1.35x
 - Dhrystone/MHz: 1.42x

Target Applications for 25, 45, 60-Series

■ AI/Deep Learning

■ AR/VR

■ 5G



■ Video Surveillance

■ ADAS



■ Networking



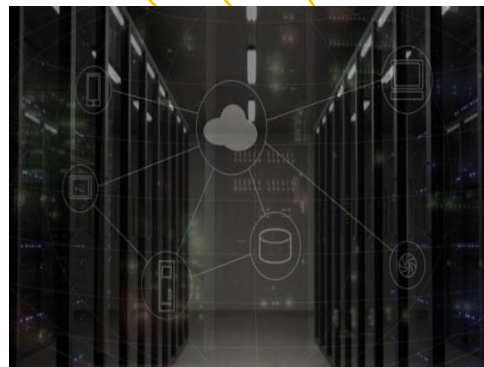
■ V2X (Vehicle to Everything)



■ IVI (In-Vehicle-Infotainment)



■ Storage



Metaverse, HPC and more...

The Andes AX60 Processor Series



■ A new generation of AndesCore™

- Advanced Performance 13-stage Out-of-Order Superscalar Multicore
- Latest RISC-V Architecture
- Supported by Andes Long-term Roadmap
 - AX65 as the first member of the AX60 series
 - More products based on the AX60 micro-architecture planned, including for automotive functional safety

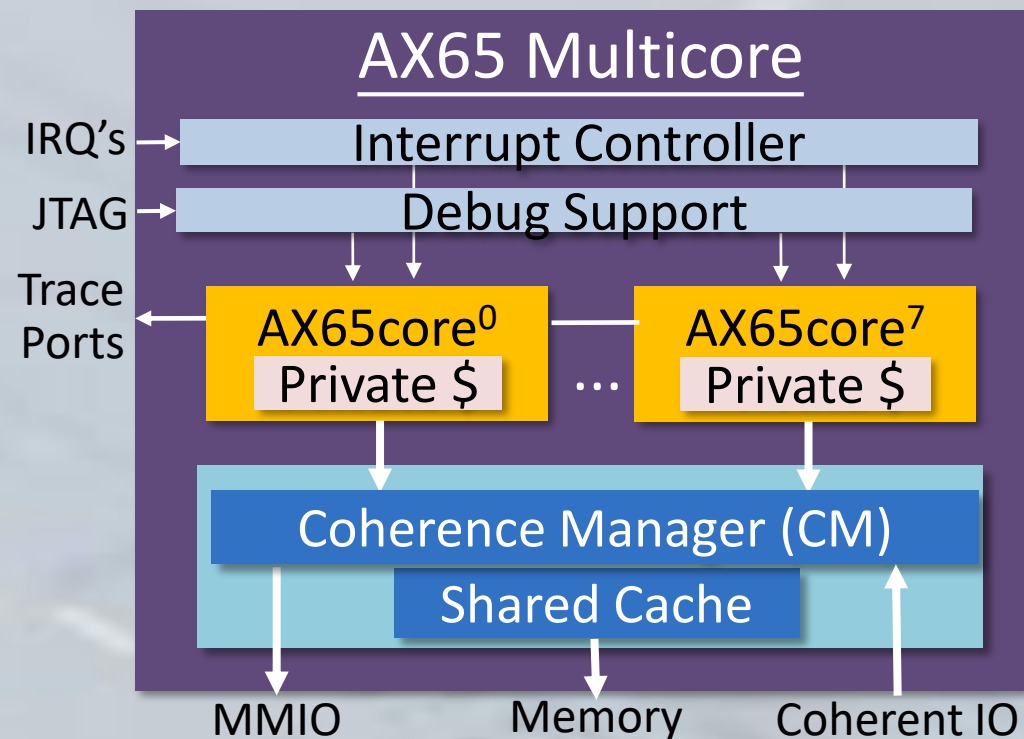
■ AndesCore™ AX65

- Offering performance surpassing CA72
- > 2.5 GHz, > 2x per-GHz performance of AX45MP
- Engaging with early customers

AndesCore AX65: 1st Member of AX60-Series



- 64-bit, RV64GCBK
- 8-core Multiprocessor
- 13-stage OoO Pipeline
- 128-entry Reorder Buffer (ROB)
- 4-wide Frontend Decoder
- 8 Execution Pipeline engines
- 2-level Branch Target Buffer (BTB)
- TAGE-L Branch Predictor
- 1024-entry 4-way L2 TLBs
- 64 KB, 4-way Private I/D Caches
- 8 MB, 16-way Shared Cache
- 256-bit AXI4, MMIO and IOCP Buses



Andes is *Driving* Innovations in Automotive



with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar



Radio	Radar Subsystem N25F-SE	Host Controller N25F-SE
	Memory	Peripheral

CMOS Sensor

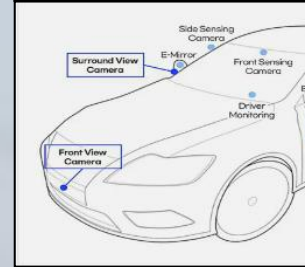

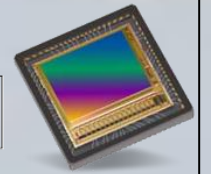




Diagram illustrating the CMOS sensor architecture and its application in automotive systems, including components like Camera, Image Sensor, and various processing blocks.

Auto TDDI

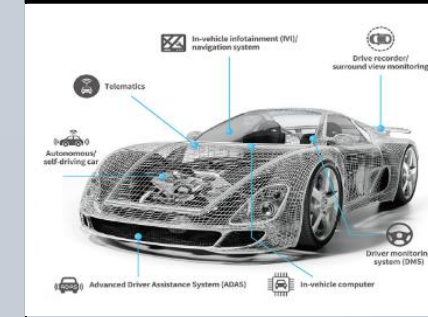
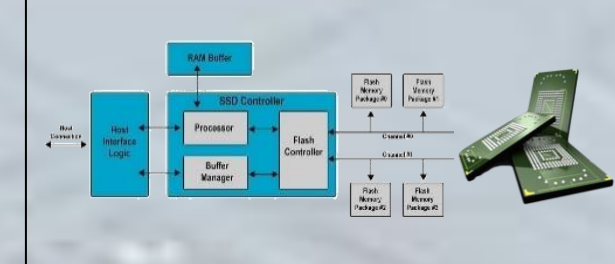



Auto MCU




器件	封装	物料号
MCU	RISC-V CPU 0	3208 L14 3208 L10
MCU	RISC-V CPU 1	3208 L14 3208 L10
MCU	RISC-V CPU 2	3208 L14 3208 L10
MCU	RISC-V CPU 3	3208 L14 3208 L10
MCU	RISC-V CPU 4	3208 L14 3208 L10
MCU	RISC-V CPU 5	3208 L14 3208 L10
MCU	RISC-V CPU 6	3208 L14 3208 L10
MCU	RISC-V CPU 7	3208 L14 3208 L10
MCU	RISC-V CPU 8	3208 L14 3208 L10
MCU	RISC-V CPU 9	3208 L14 3208 L10
MCU	RISC-V CPU 10	3208 L14 3208 L10
MCU	RISC-V CPU 11	3208 L14 3208 L10
MCU	RISC-V CPU 12	3208 L14 3208 L10
MCU	RISC-V CPU 13	3208 L14 3208 L10
MCU	RISC-V CPU 14	3208 L14 3208 L10
MCU	RISC-V CPU 15	3208 L14 3208 L10
MCU	RISC-V CPU 16	3208 L14 3208 L10
MCU	RISC-V CPU 17	3208 L14 3208 L10
MCU	RISC-V CPU 18	3208 L14 3208 L10
MCU	RISC-V CPU 19	3208 L14 3208 L10
MCU	RISC-V CPU 20	3208 L14 3208 L10
MCU	RISC-V CPU 21	3208 L14 3208 L10
MCU	RISC-V CPU 22	3208 L14 3208 L10
MCU	RISC-V CPU 23	3208 L14 3208 L10
MCU	RISC-V CPU 24	3208 L14 3208 L10
MCU	RISC-V CPU 25	3208 L14 3208 L10
MCU	RISC-V CPU 26	3208 L14 3208 L10
MCU	RISC-V CPU 27	3208 L14 3208 L10
MCU	RISC-V CPU 28	3208 L14 3208 L10
MCU	RISC-V CPU 29	3208 L14 3208 L10
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MCU	RISC-V CPU 31	3208 L14 3208 L10
MCU	RISC-V CPU 32	3208 L14 3208 L10
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MCU	RISC-V CPU 34	3208 L14 3208 L10
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MCU	RISC-V CPU 85	3208 L14 3208 L10
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MCU	RISC-V CPU 90	3208 L14 3208 L10
MCU	RISC-V CPU 91	3208 L14 3208 L10
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MCU	RISC-V CPU 97	3208 L14 3208 L10
MCU	RISC-V CPU 98	3208 L14 3208 L10
MCU	RISC-V CPU 99	3208 L14 3208 L10
MCU	RISC-V CPU 100	3208 L14 3208 L10

Auto Storage

The Rise of

AndesAIRE™ AnDLA™ I350

The First Generation of Andes Deep Learning Accelerator

AndesAIRE™ NN SDK

Unleash the maximum AI/ML performance
and synergy of RISC-V CPU and AnDLA™



AndesAIRE™
Andes AI Runs Everywhere

Andes AI Total Solutions



NN models

AndeSight™ IDE

- GCC/LLVM Toolchains
- Build, debug, deploy, profile
- Analysis and tuning
- RTOS & Linux
- Device drivers
- Sample codes
- Simulator
- Documentation

AndesAIRE™ NN SDK

AndesAIRE™ NN Pilot™

Generated C code template

NN inference engines

TensorFlow Lite TensorFlow Lite tvm

AndesAIRE™ NN Library
AndeSoft™ Vector / DSP Library
AnDLA driver

Linux Host Processor
AX45MP(V), AX65

Compute Acceleration
Vector: 27V, 45V
DSP/SIMD: D25F, D45

Accelerator
AnDLA™ I350

Bus

AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera



Smart Sensor



Smart Home Appliance



AIoT / tinyML



Robotics



Wearable



一張含有 醫療設備, 醫療, 保健, 人員 的圖片
自動產生的描述

Thank You

<http://www.andestech.com>

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N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor



- ISO 26262 Certification for Development Process: ASIL-D
 - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- ISO-9001 QMS achieved and maintained since 2010
- ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE
 - ISO 26262-2,4,5,8,9
 - Covers all the sections applicable to CPU core

AndesAIRE™ AnDLA™ I350



- **Andes Deep Learning Accelerator (AnDLA™)**
 - High performance-efficient deep learning accelerator for **edge and end-point inference**
 - Scalable and multi-DLA
 - Cooperate with AndesCore™ full series (22/23/25/27/45/65)
- **Accelerating for most of NN Applications**
 - Image and video
 - Speech/voice and audio
- **Target performance**
 - Configurable MACs: **32 to 4096 (INT8)**
 - Performance: **64 GOPS to 8 TOPS (INT8 @1GHz)**
 - Configurable local memory: 16KB to 4MB
 - Leading power efficiency >5 TOPS/W (@28nm)
- **Integrated DMA and local memory**

AnDLA™ I350

