晶心科技股份有限公司

ANDES TECHNOLOGY

投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

01 公司簡介

02 營運成果

03 產品應用

04 新產品及生態系統

05 總結

公司簡介

http://www.andestech.com

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 根基穩健的高科技上市公司。
- 員工人數超過400人；80%為工程師。
- 獲得TSMC 2015年新的 IP OIP Award 。
- 晉升為RISC-V國際聯盟(前身為RISC-V基金會) 首席會員。 (2020)
- 獲得AI Global Media頒發「2020年最傑出嵌入式處理器IP供應商」。
- EE Awards亞洲金選獎 -「Taiwan 產品獎」,「Asia 企業獎」(2021)
- 2023亞太區 前五百大高成長企業

晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

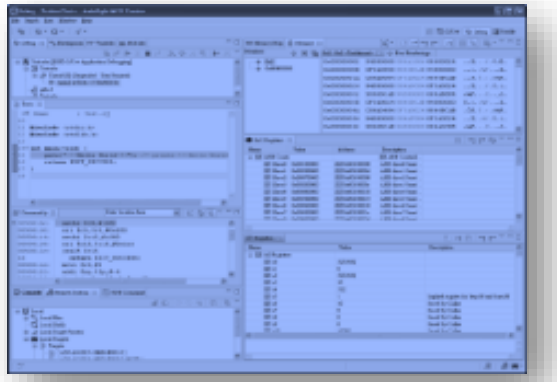
晶心利基

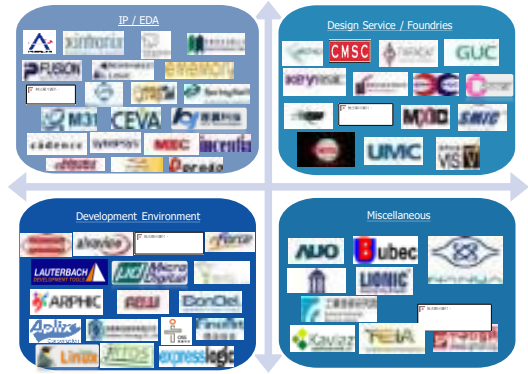
- 智能及環保之電子設備
- 雲端應用,人工智慧及物聯網

ANDES TECHNOLOGY

重要里程碑

- **300+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **600+** license agreements signed
- AndeSight™ IDE:
  - **25,000+** installations
- Eco-system:
  - **500+** partners
- **12B+** Accumulative SoC Shipped



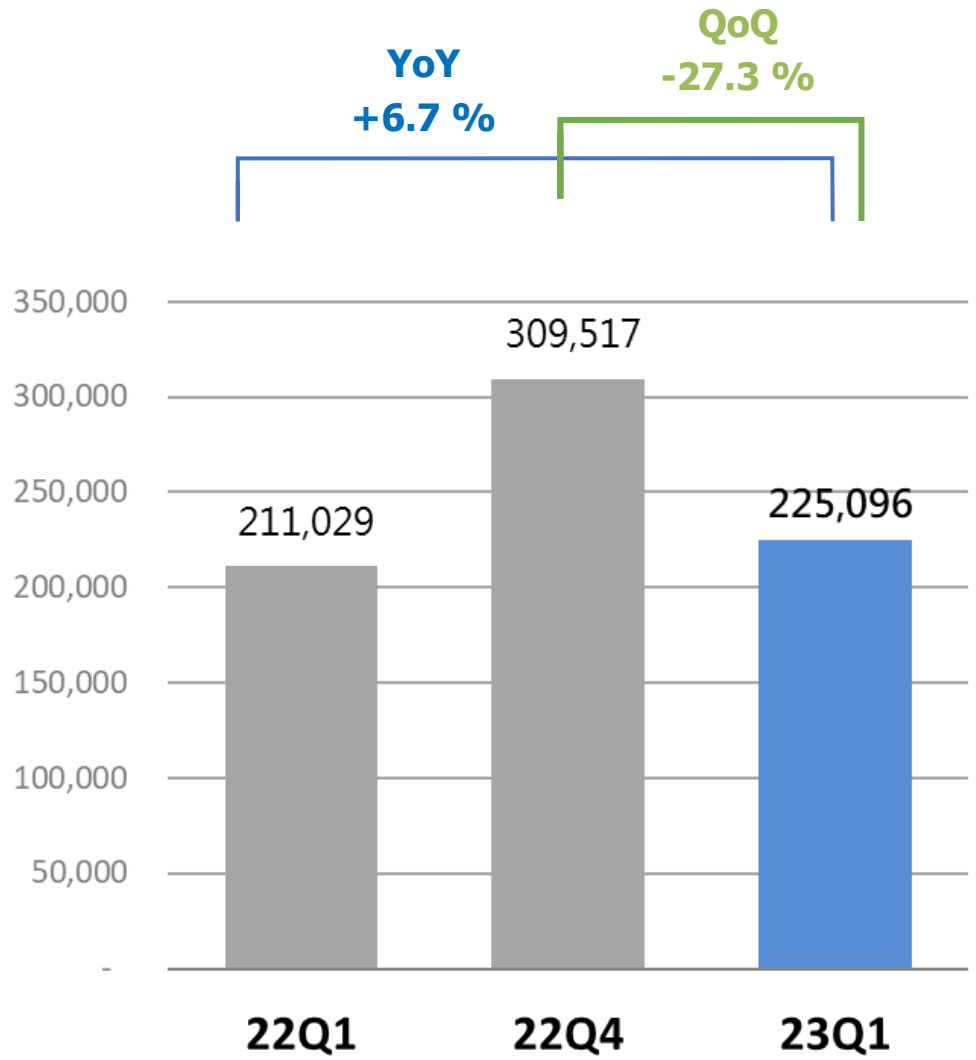


營運成果

http://www.andestech.com

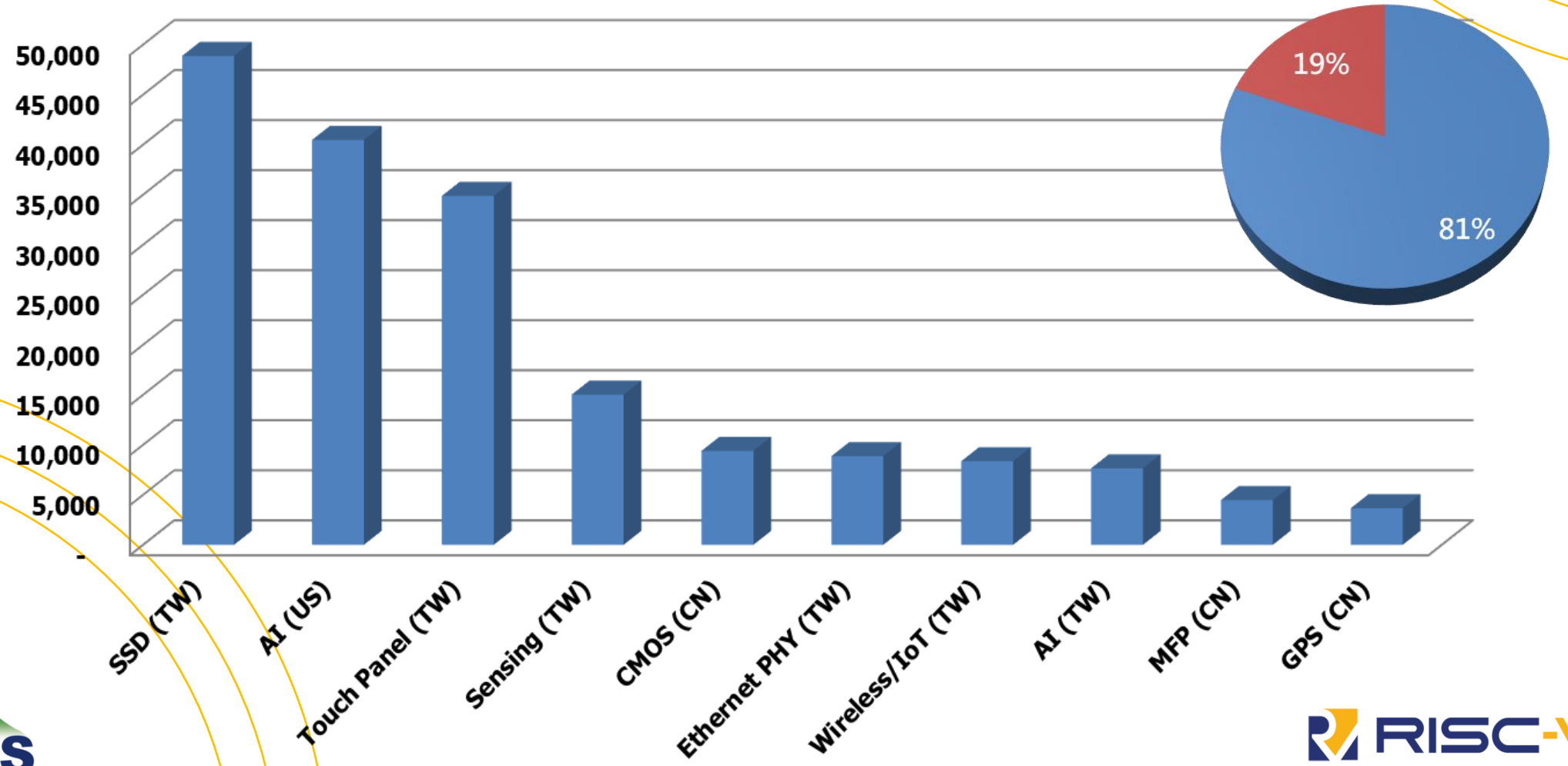
2023年第一季營業收入

(單位:新台幣千元)



2023年第一季前十大客戶之應用分析

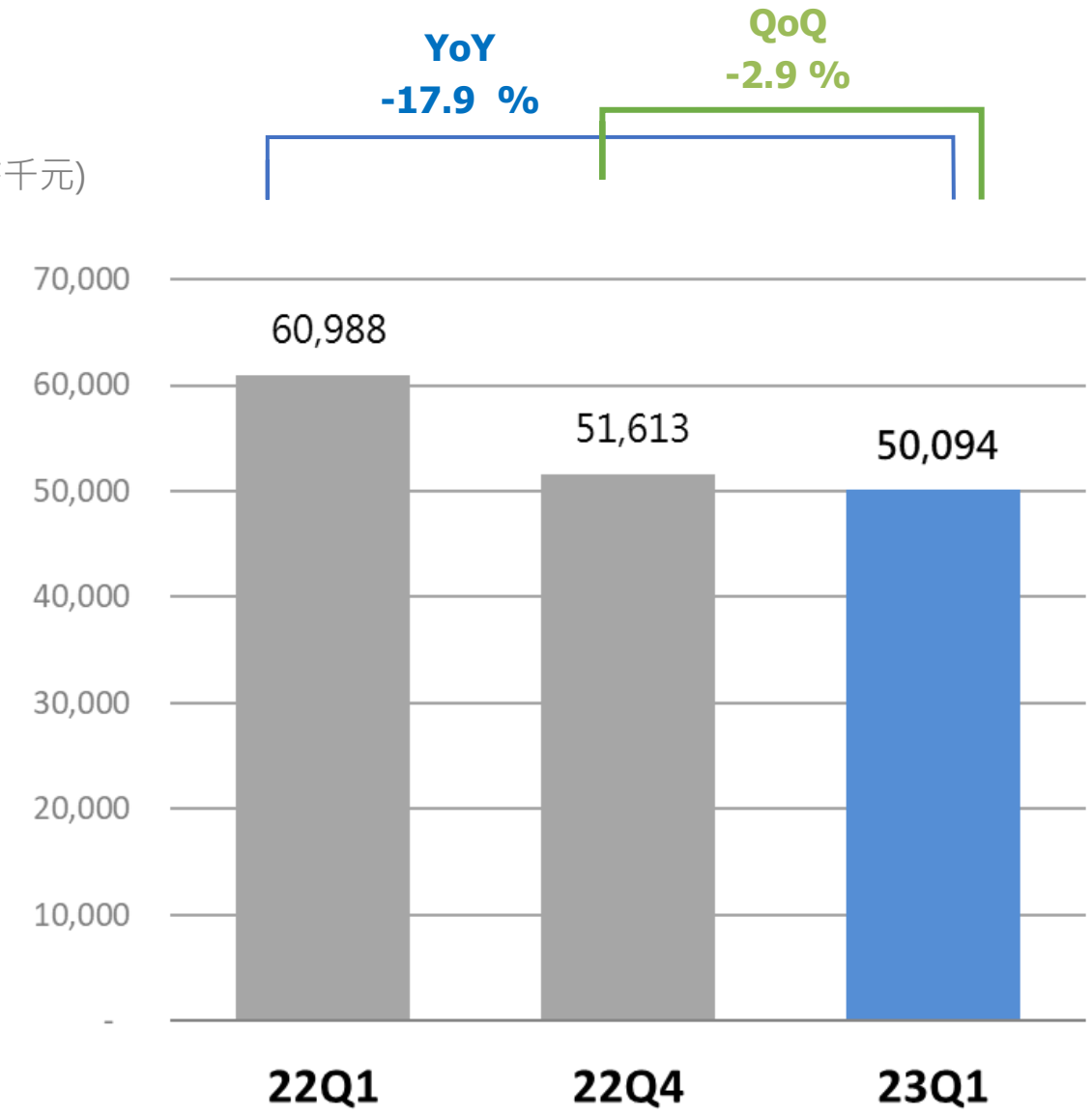
單位: 新台幣千元



前十大客戶貢獻81%的營收

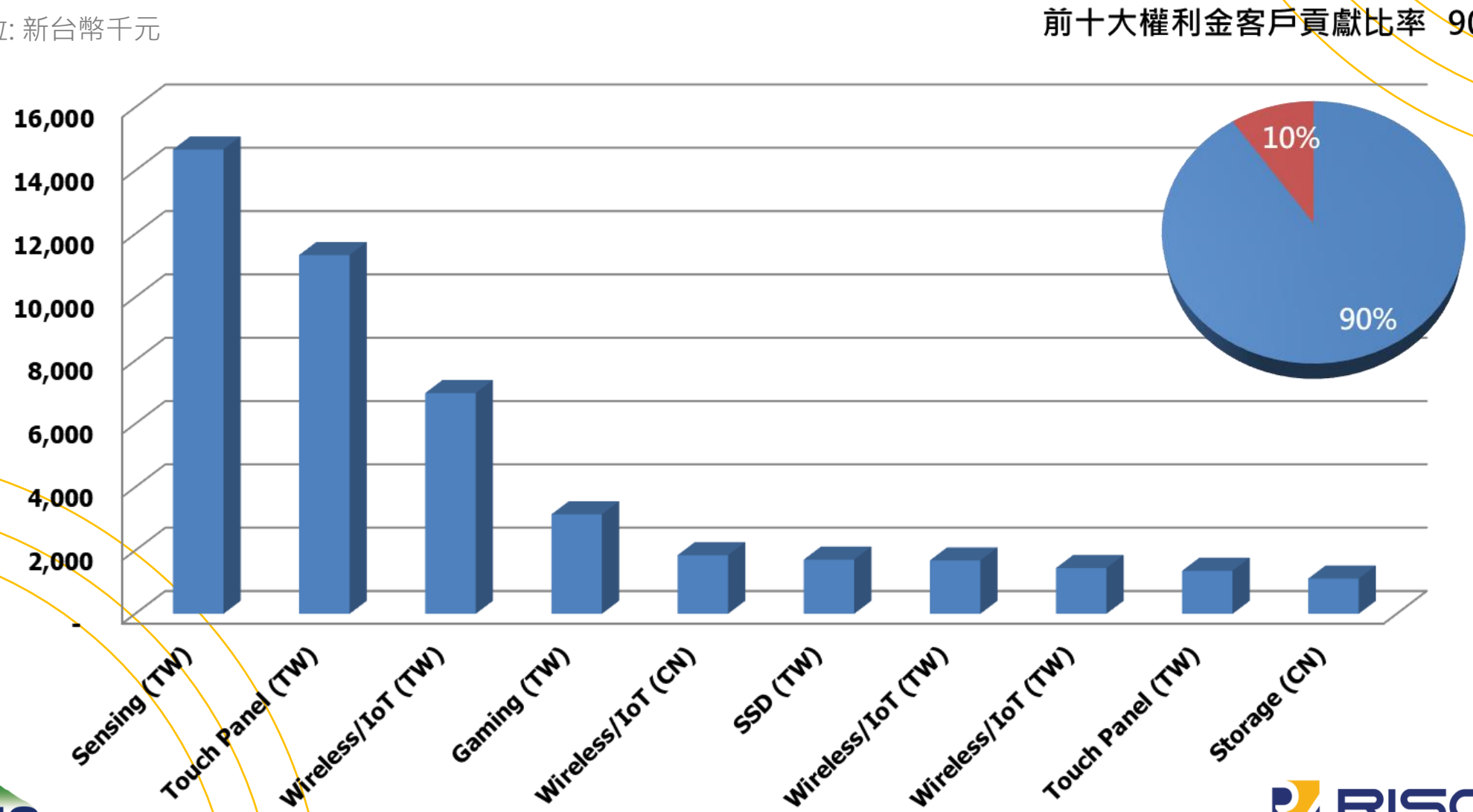
2023年第一季度權利金收入

(單位:新台幣千元)



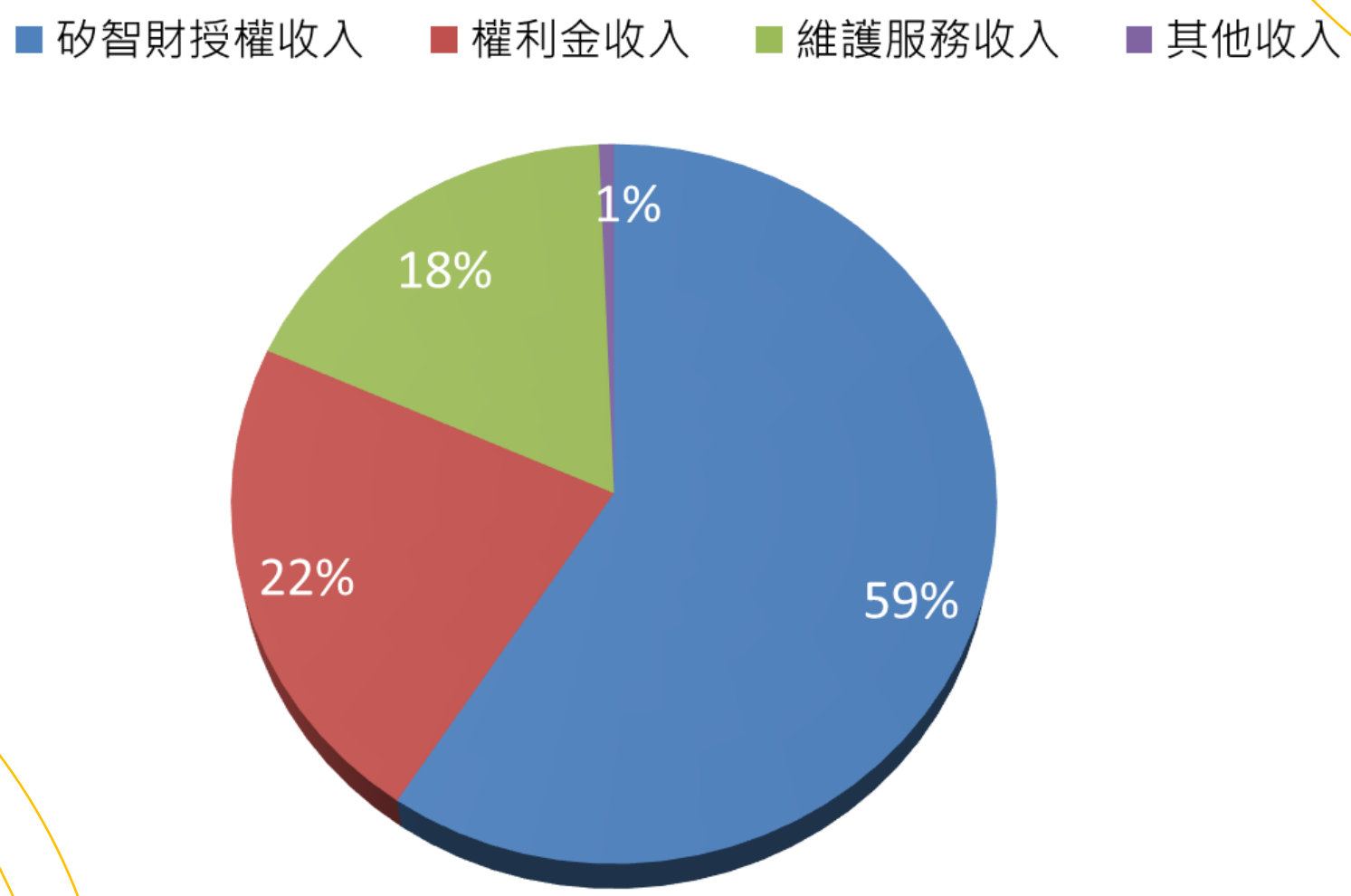
2023年第一季權利金應用分析

單位: 新台幣千元

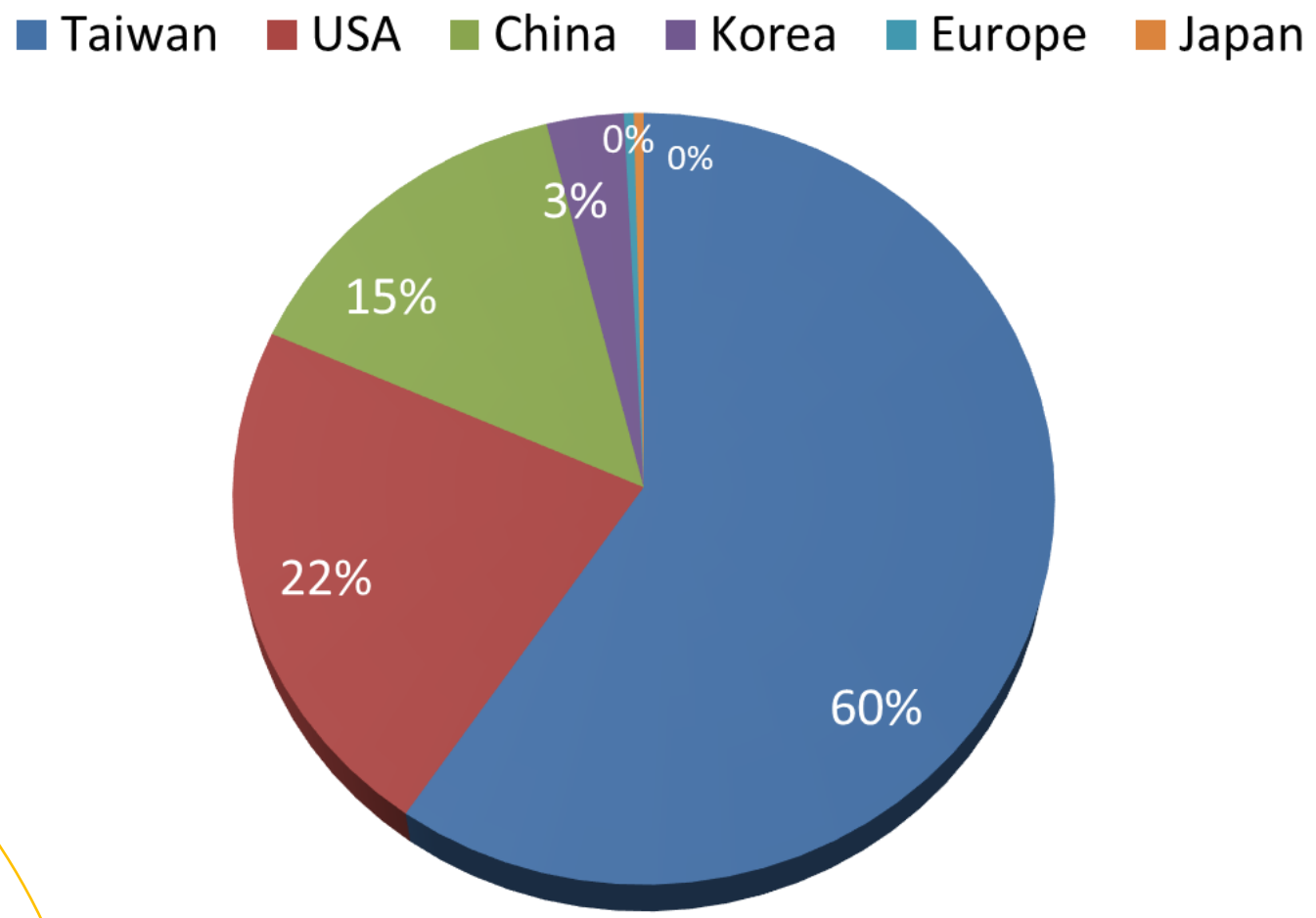


前十大權利金客戶貢獻比率 90%

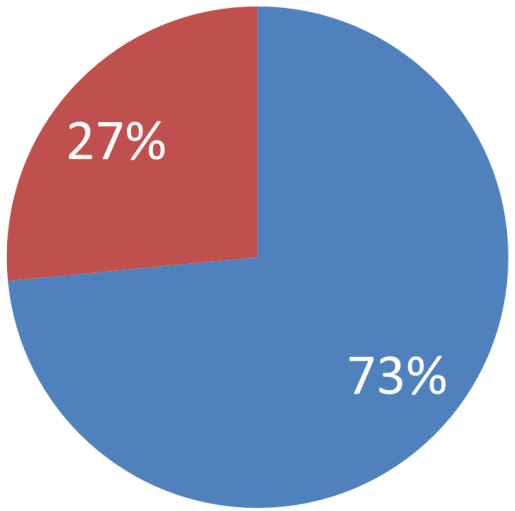
2023年第一季 銷售分析-收入模式

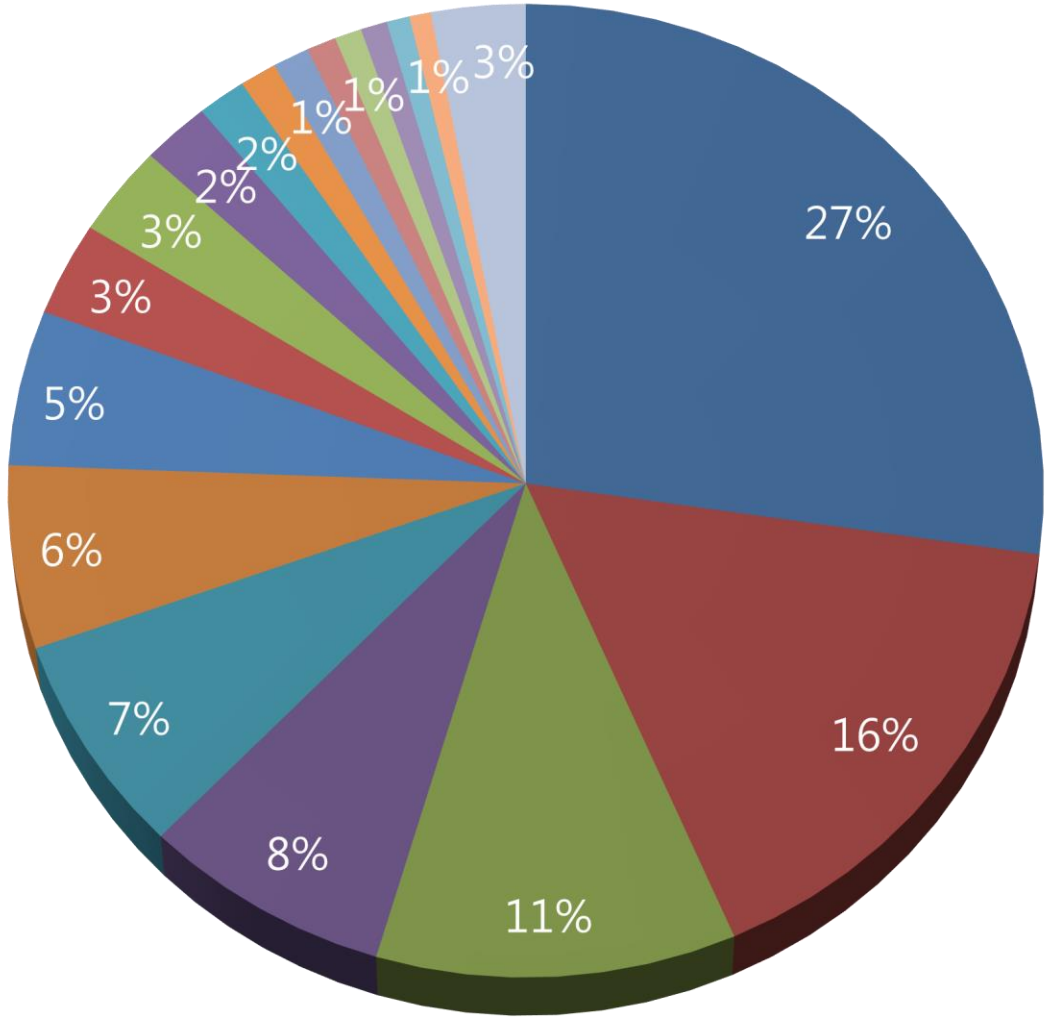


2023年第一季 銷售分析-地區別



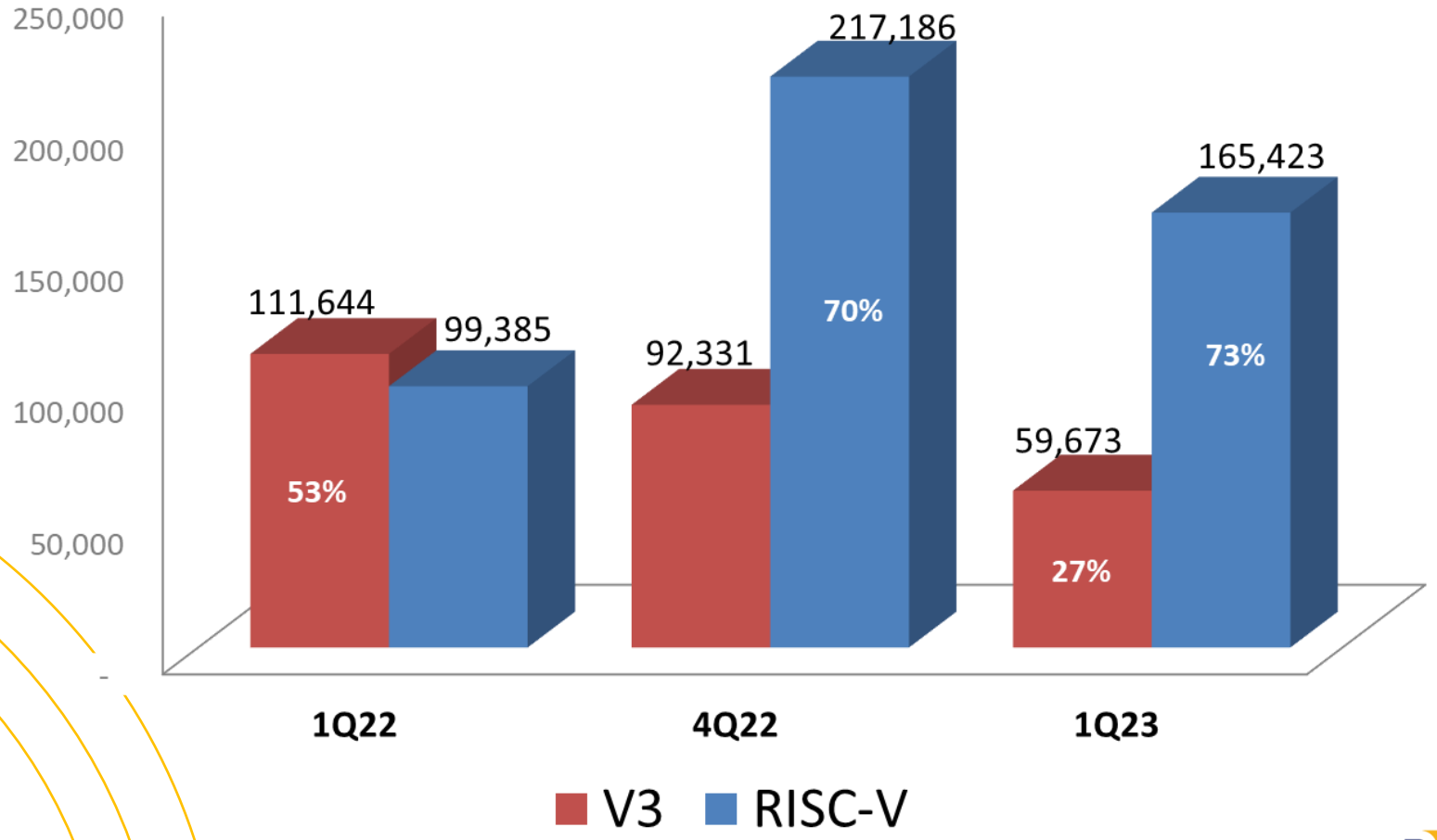
2023年第一季 銷售分析-產品別





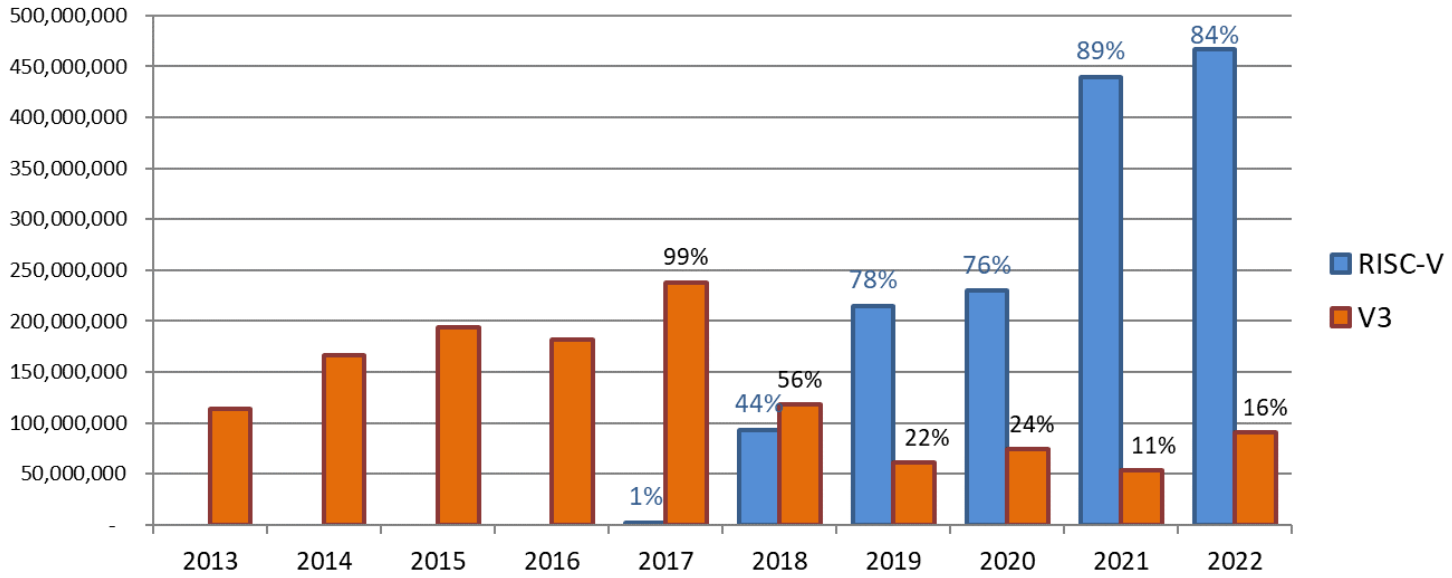
2023年第一季 銷售分析- RISC-V

(單位:新台幣千元)

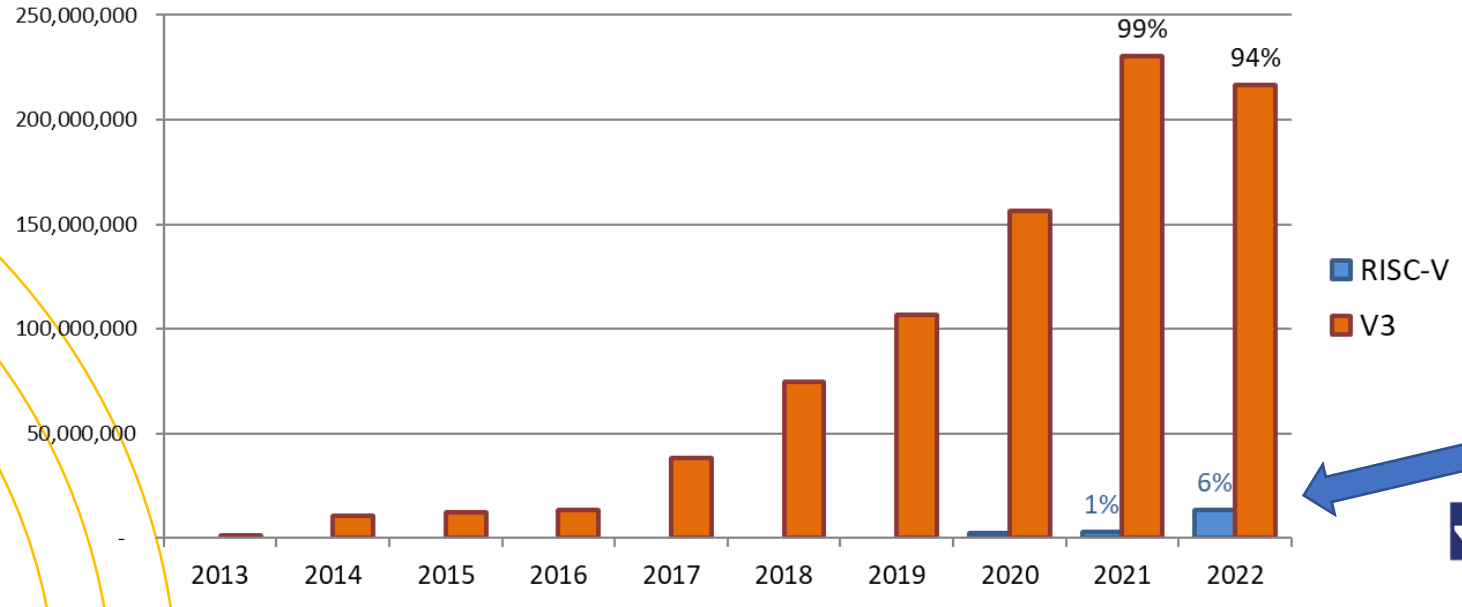


歷史營收分析

(NT$)



License

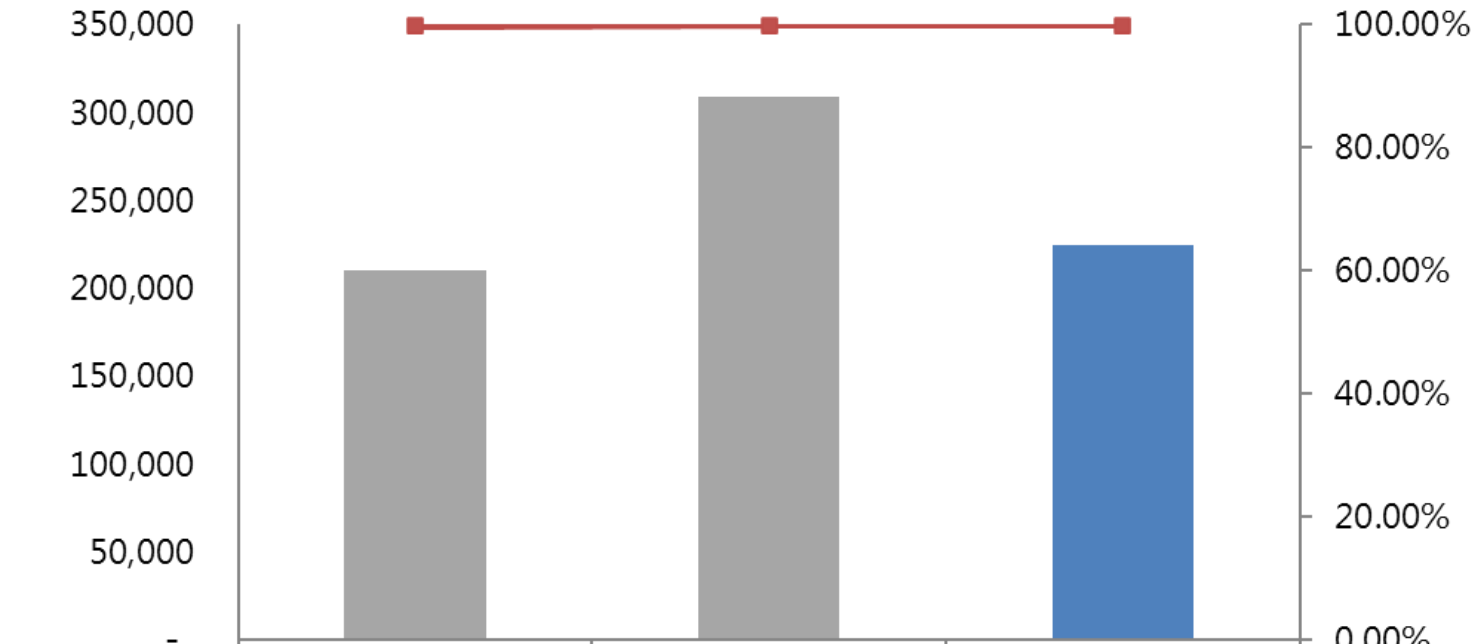


Royalty

RISC-V 2022: 6%

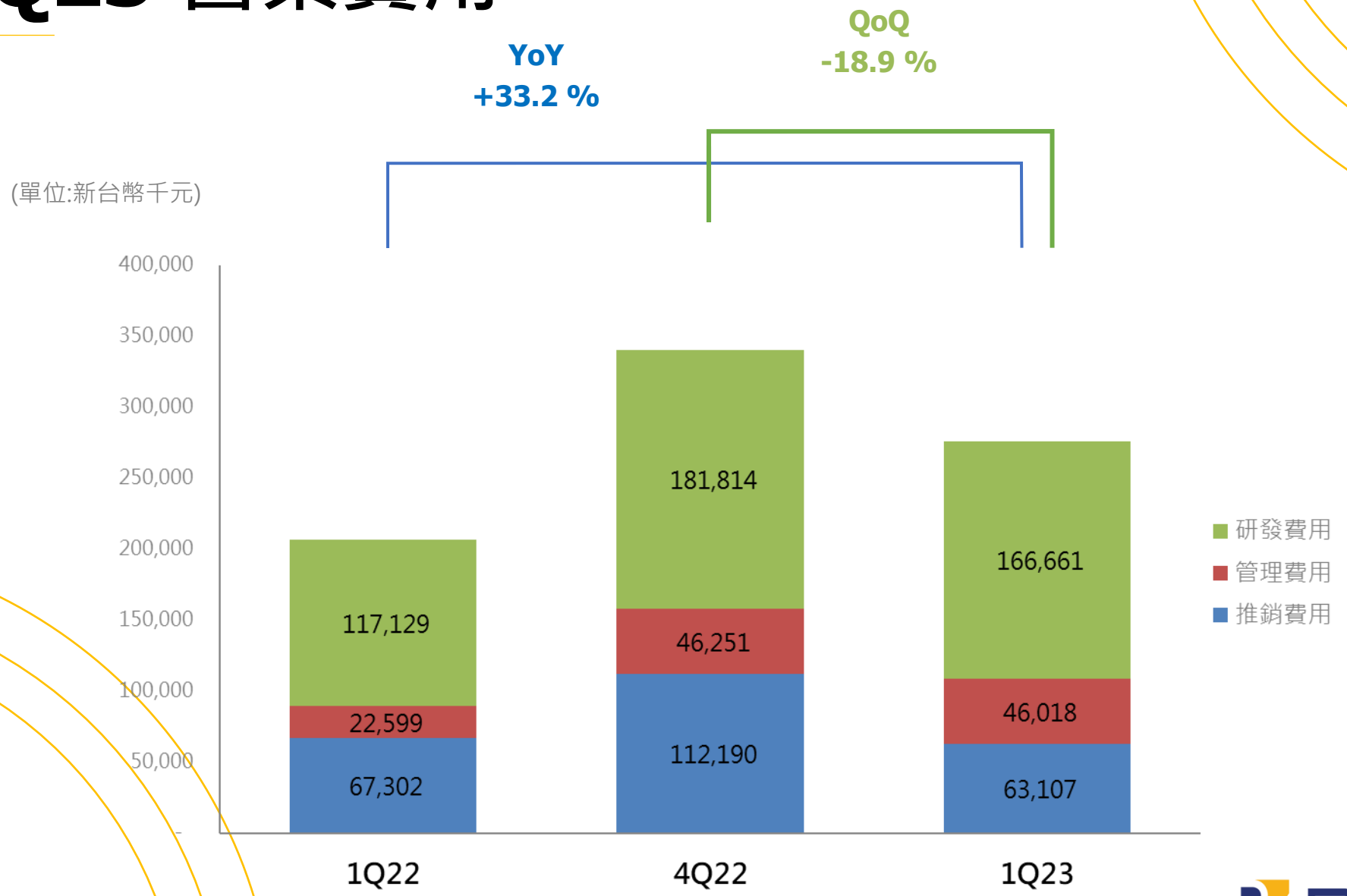
1Q23 營業毛利與毛利率

(單位:新台幣千元)

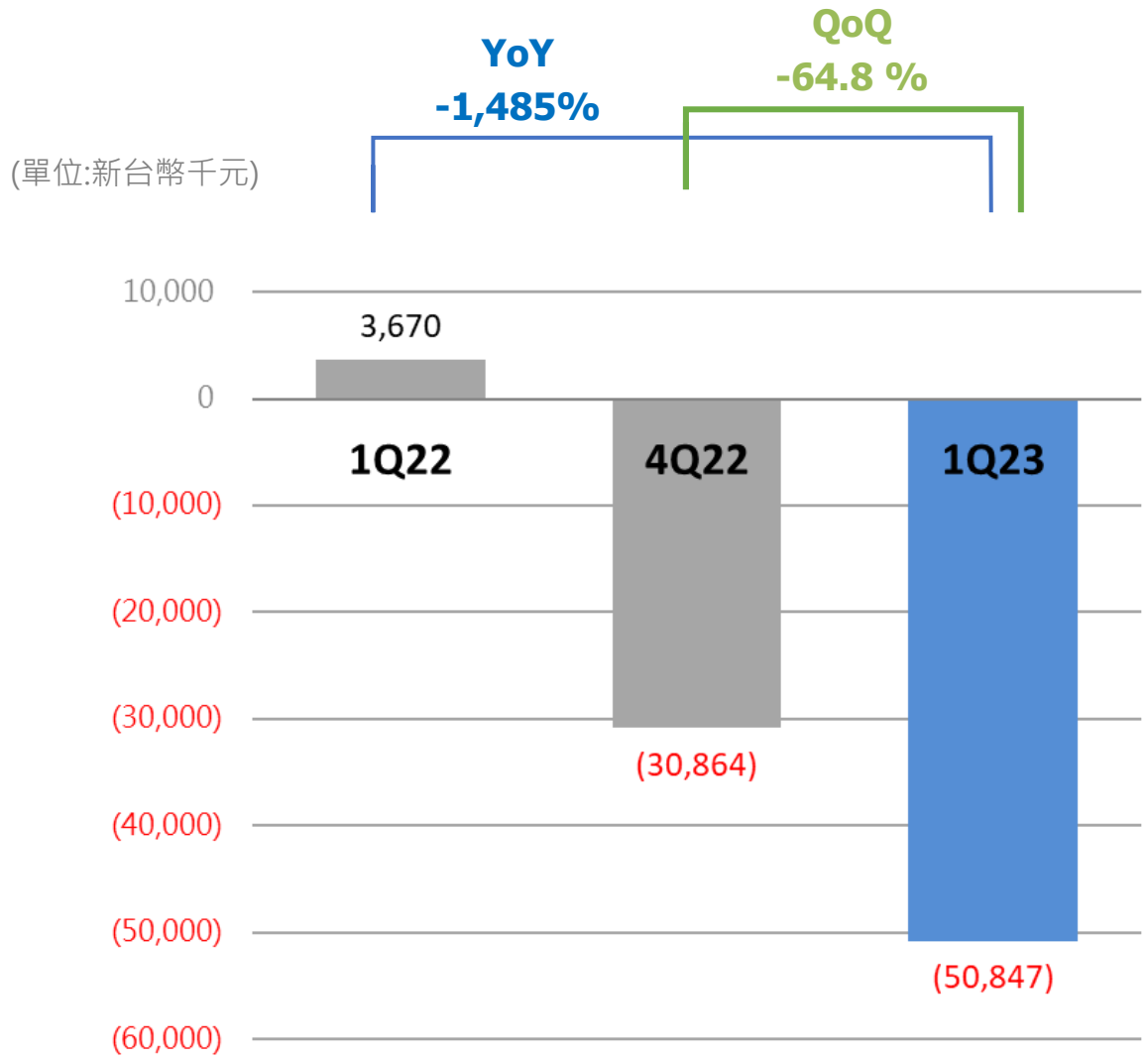


	1Q22	4Q22	1Q23
營業毛利	210,700	309,391	224,939
毛利率	99.84%	99.96%	99.93%

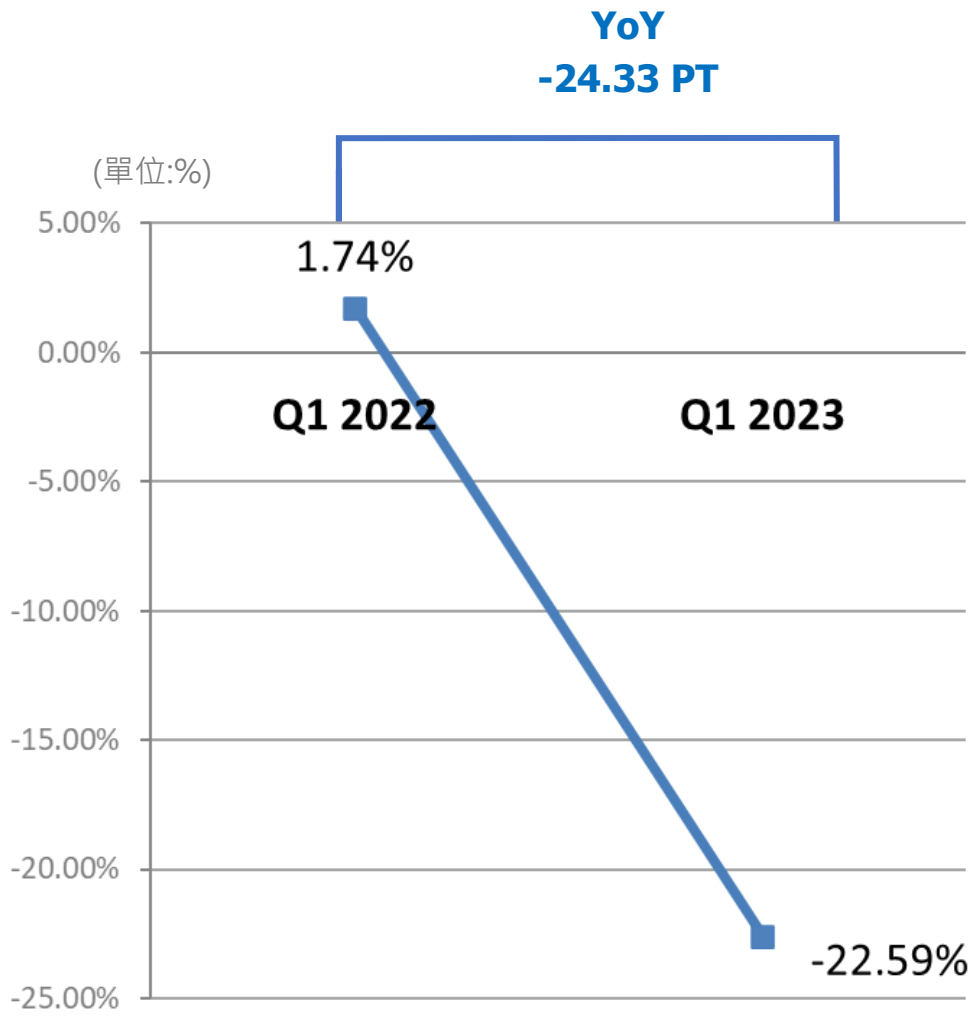
1Q23 營業費用


YoY
+33.2 %
QoQ
-18.9 %
(單位:新台幣千元)
400,000
350,000
300,000
250,000
200,000
150,000
100,000
50,000
-
117,129
22,599
67,302
181,814
46,251
112,190
166,661
46,018
63,107
1Q22
4Q22
1Q23
研發費用
管理費用
推銷費用

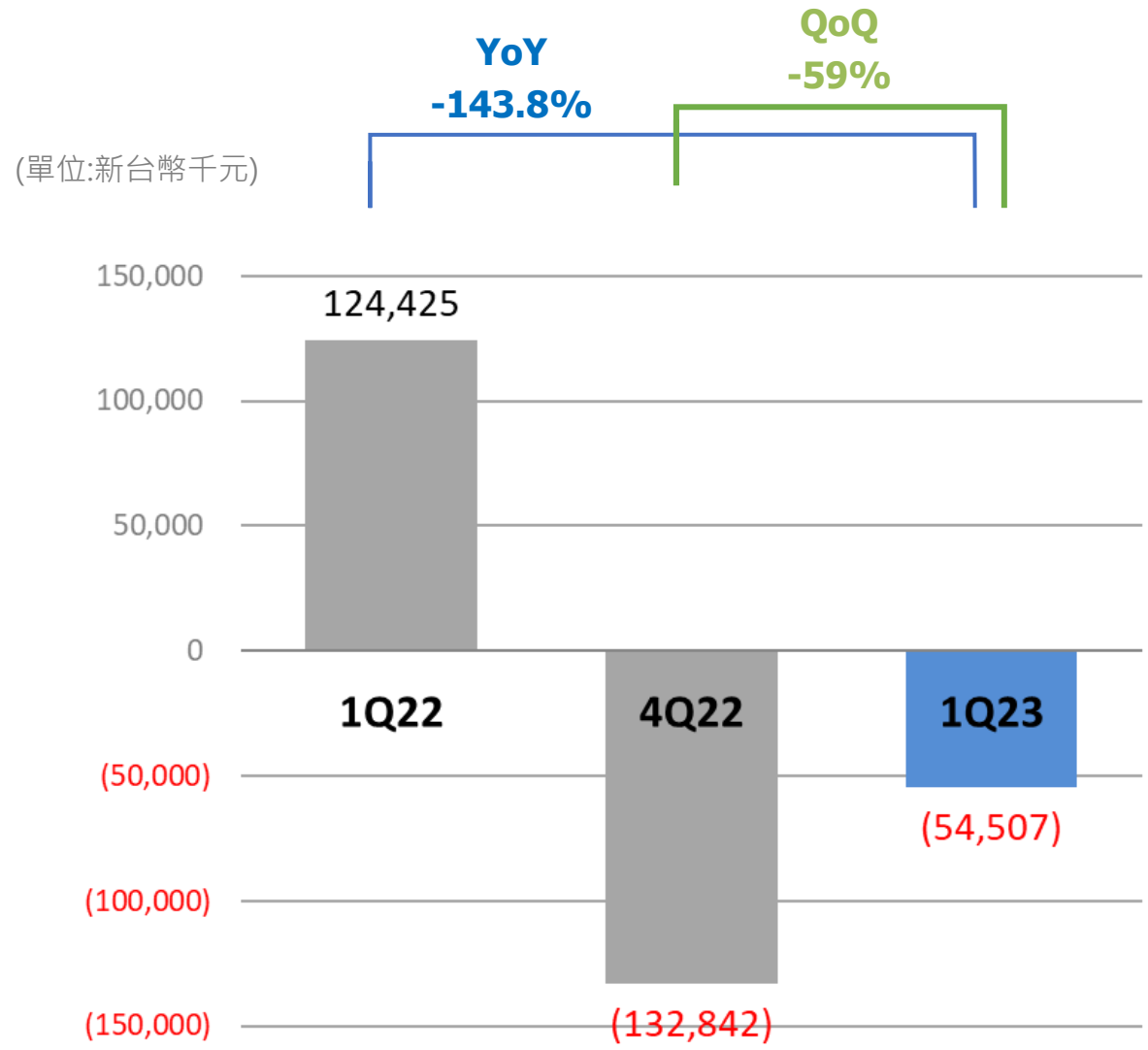
1Q23 營業利益


YoY
-1,485%
QoQ
-64.8 %
(單位:新台幣千元)
10,000
0
(10,000)
(20,000)
(30,000)
(40,000)
(50,000)
(60,000)
3,670
(30,864)
(50,847)
1Q22
4Q22
1Q23

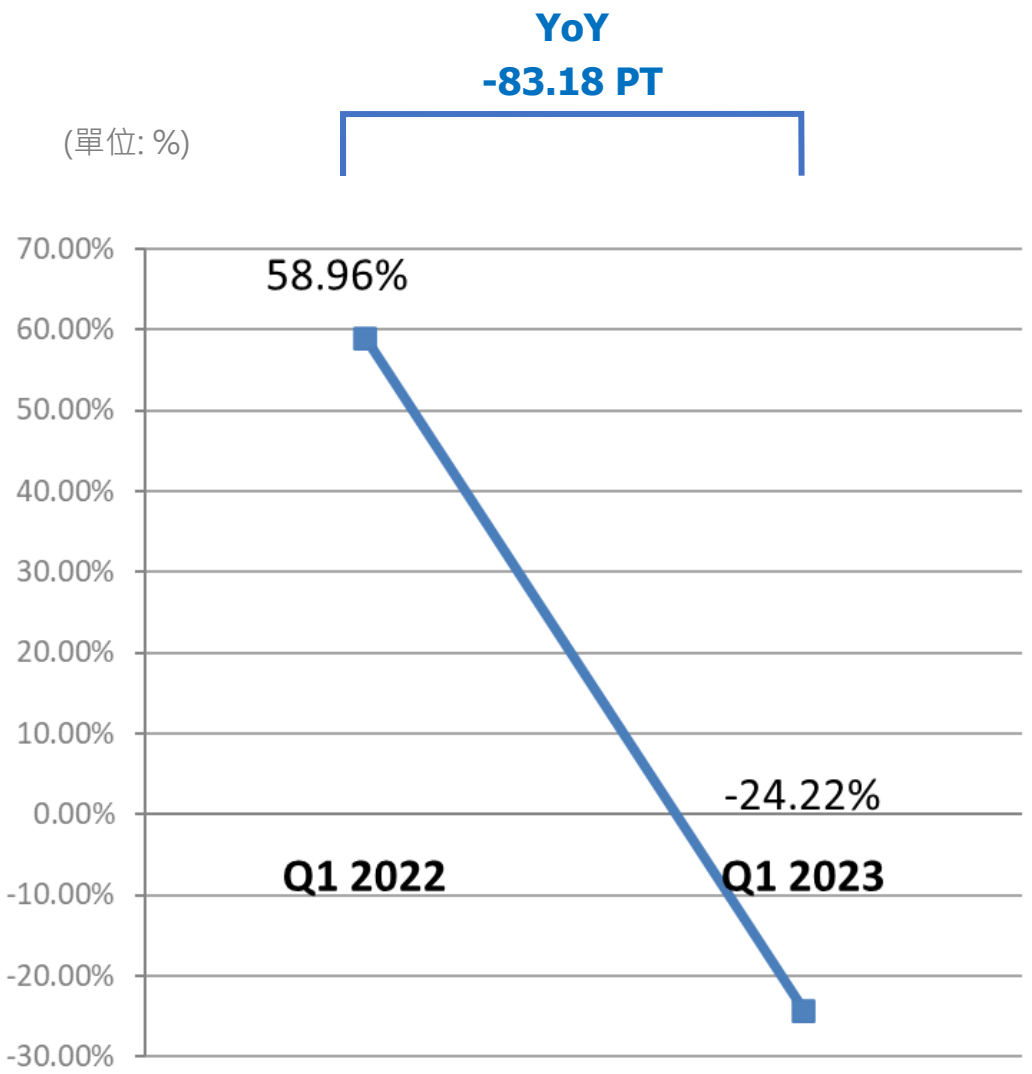
1Q23 營業利益率


YoY
-24.33 PT
(單位:%)
5.00%
0.00%
-5.00%
-10.00%
-15.00%
-20.00%
-25.00%
1.74%
-22.59%
Q1 2022
Q1 2023

1Q23 合併淨利

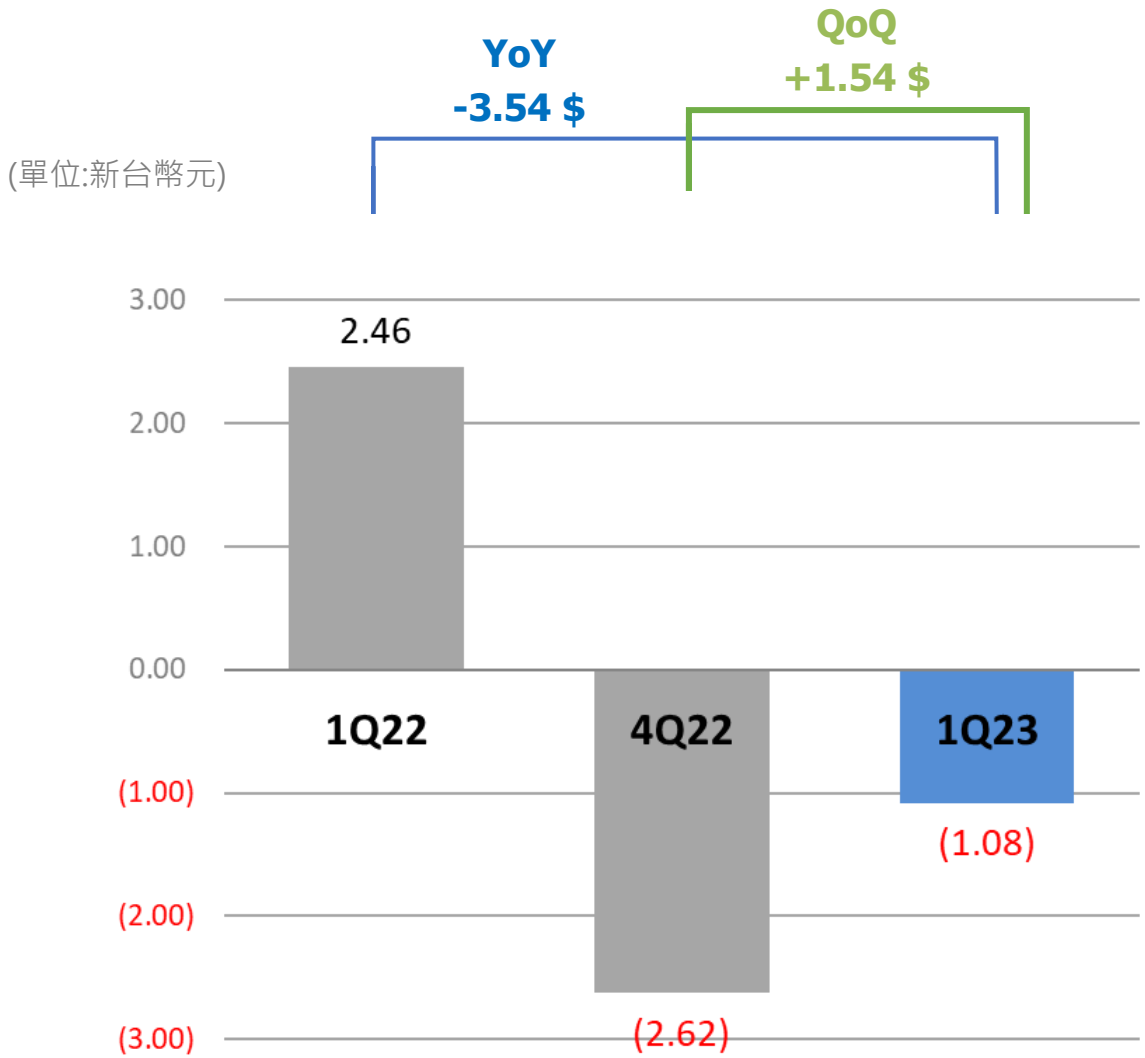

YoY
-143.8%
QoQ
-59%
(單位:新台幣千元)
150,000
100,000
50,000
0
(50,000)
(100,000)
(150,000)
124,425
(132,842)
(54,507)
1Q22
4Q22
1Q23

1Q23 合併淨利率


YoY
-83.18 PT
(單位: %)
70.00%
60.00%
50.00%
40.00%
30.00%
20.00%
10.00%
0.00%
-10.00%
-20.00%
-30.00%
58.96%
-24.22%
Q1 2022
Q1 2023

1Q23 每股盈餘

(單位:新台幣元)



產品應用

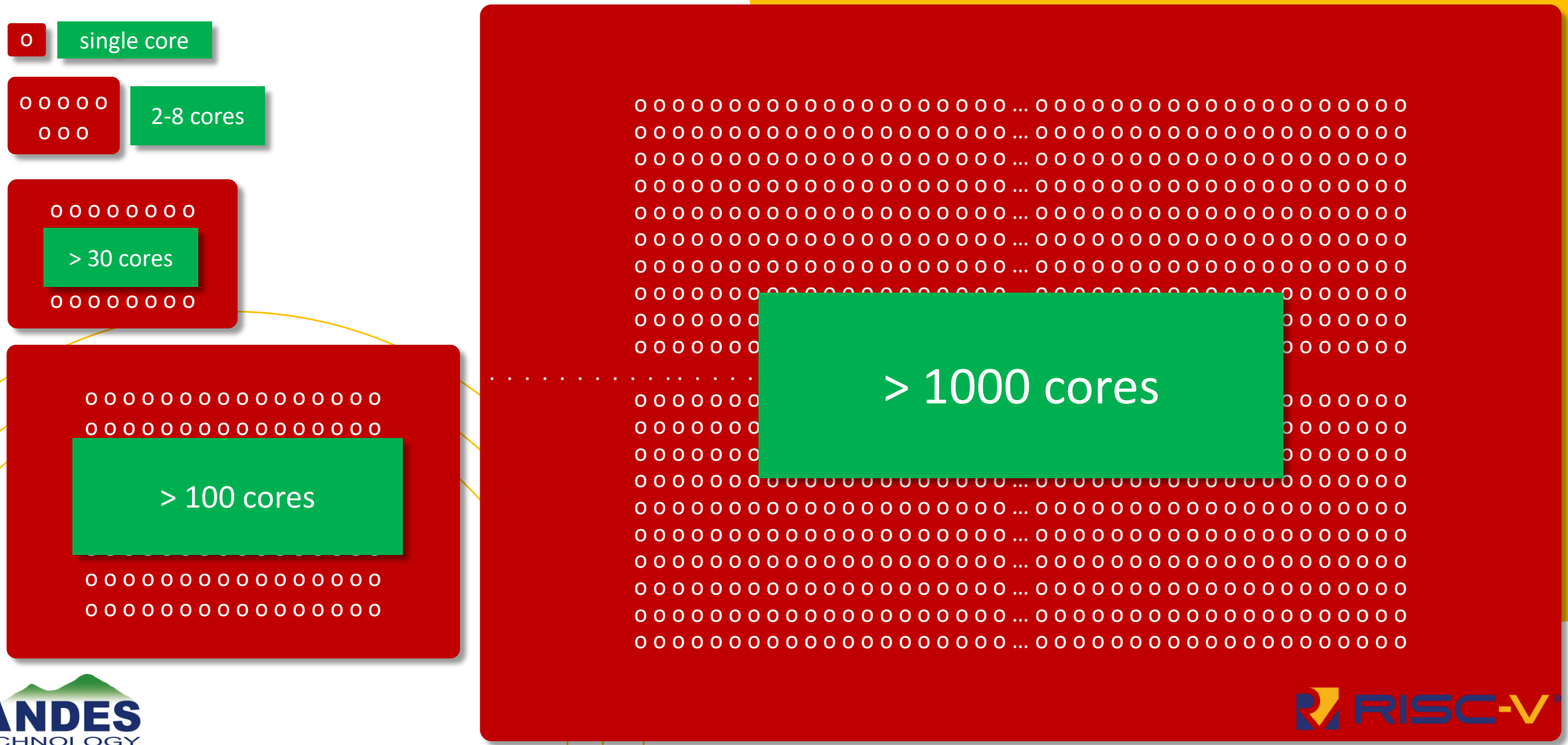
http://www.andestech.com

晶心RISC-V在邊緣到雲端運算SoC的應用實例

- **Edge to Cloud**
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)
- **40nm to 3nm**
- **Many in AI**

- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

晶心RISC-V核心在SoC中被採用的數目



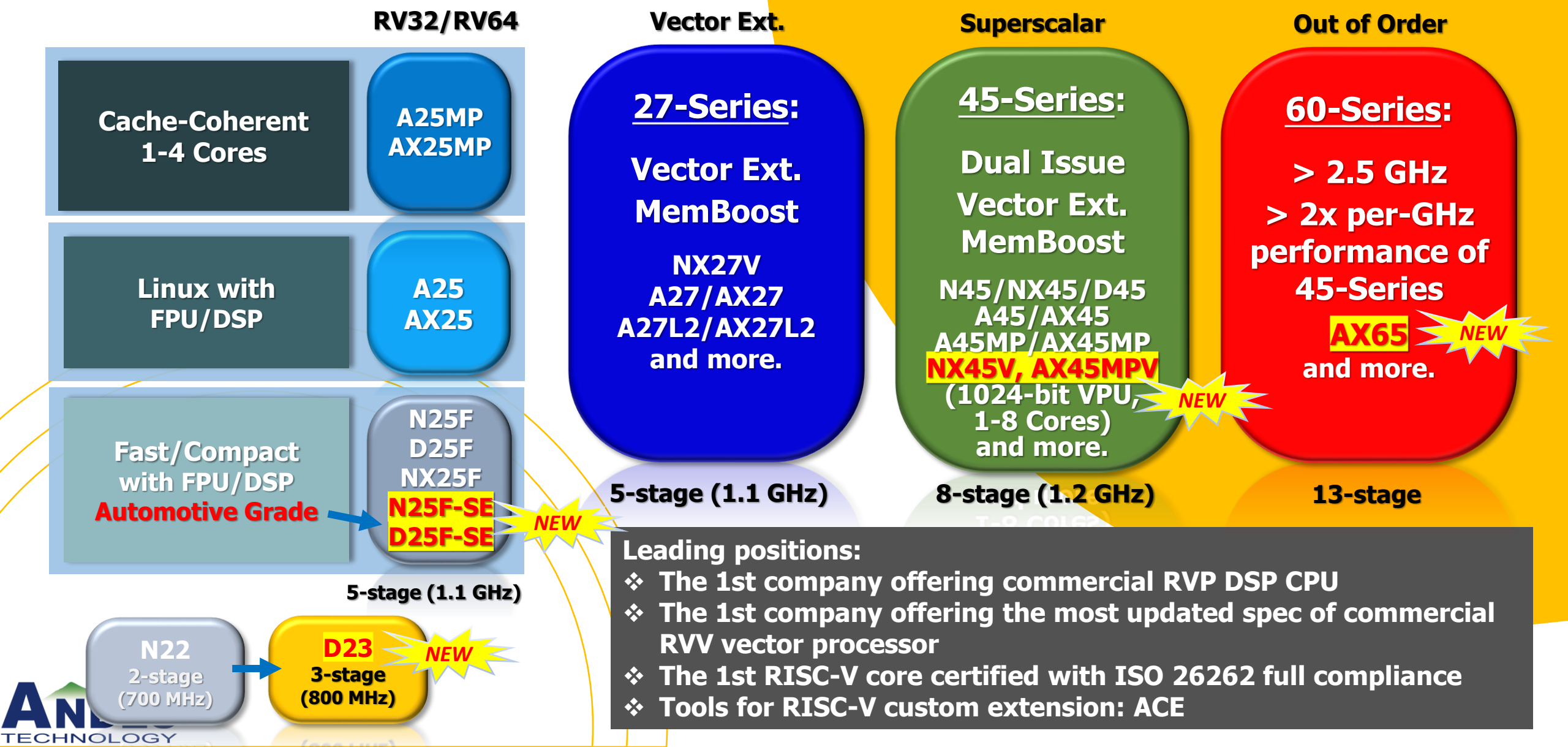
ANDES TECHNOLOGY

RISC-V

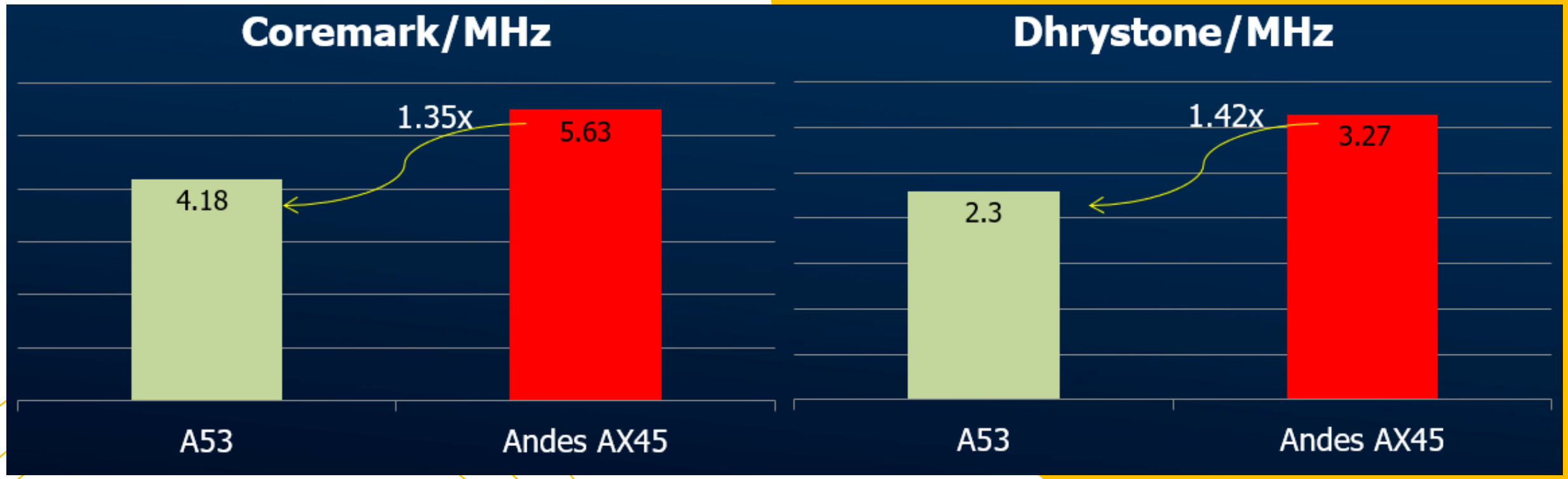
新產品及生態系統

http://www.andestech.com

晶心RISC-V產品路線圖



AX45 Can Do More (vs. 64bit A-series)



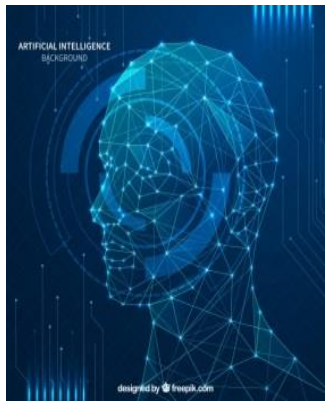
- **A53**
  - 8-stage In-Order Dual Issue
  - **Widely adopted by industries in many applications**

- **AX45**
  - 8-stage In-Order Dual Issue
  - **Performance is better!**
    - **Coremark/MHz: 1.35x**
    - **Dhrystone/MHz: 1.42x**

ANDES TECHNOLOGY

25, 45, 60系列產品的目標市場

- AI/Deep Learning
- AR/VR
- 5G



- Networking

- Storage

- Video Surveillance

- ADAS

- V2X (Vehicle to Everything)

- IVI (In-Vehicle-Infotainment)

Metaverse, HPC and more…

ANDES TECHNOLOGY

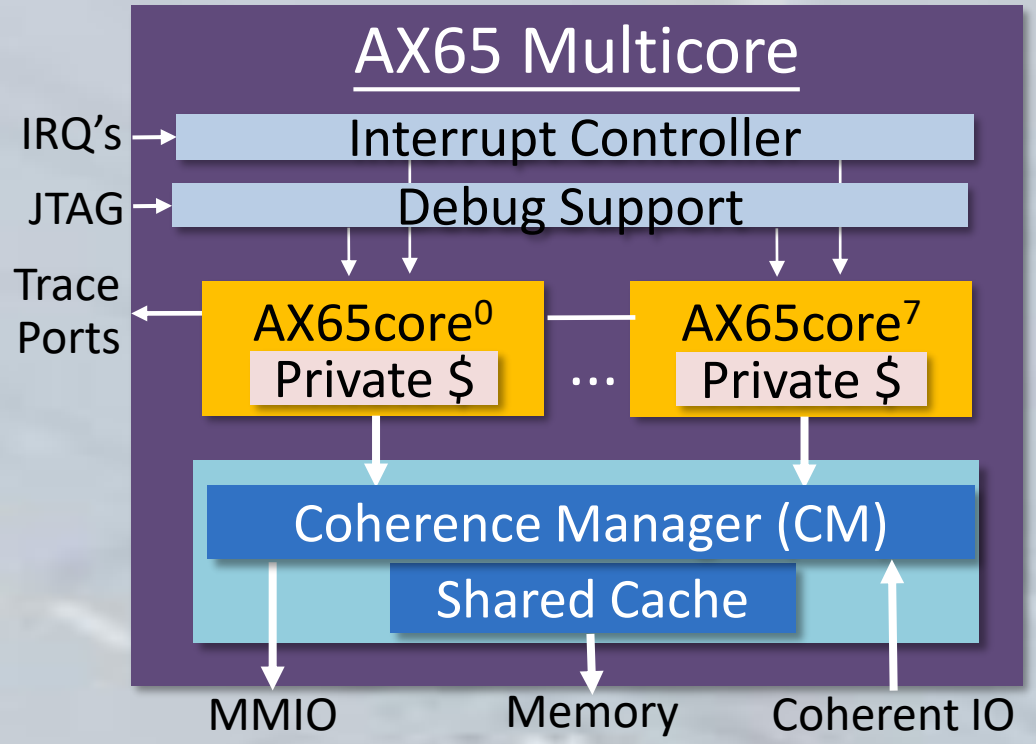
The Andes AX60 Processor Series

- A new generation of AndesCore™
  - Advanced Performance 13-stage Out-of-Order Superscalar Multicore
  - Latest RISC-V Architecture
  - Supported by Andes Long-term Roadmap
    - AX65 as the first member of the AX60 series
    - More products based on the AX60 micro-architecture planned, including for automotive functional safety

- AndesCore™ AX65
  - Offering performance surpassing CA72
  - > 2.5 GHz, > 2x per-GHz performance of AX45MP
  - Engaging with early customers

AndesCore AX65: 1st Member of AX60-Series

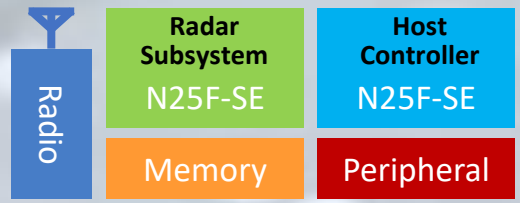
- 64-bit, RV64GCBK
- 8-core Multiprocessor
- 13-stage OoO Pipeline
- 128-entry Reorder Buffer (ROB)
- 4-wide Frontend Decoder
- 8 Execution Pipeline engines
- 2-level Branch Target Buffer (BTB)
- TAGE-L Branch Predictor
- 1024-entry 4-way L2 TLBs
- 64 KB, 4-way Private I/D Caches
- 8 MB, 16-way Shared Cache
- 256-bit AXI4, MMIO and IOCP Buses



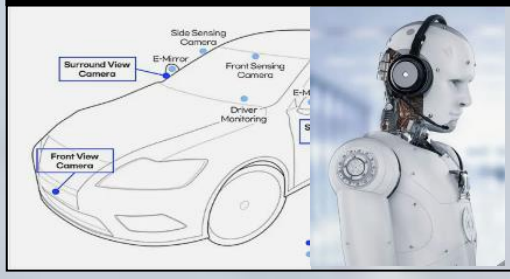
Andes is *Driving* Innovations in Automotive

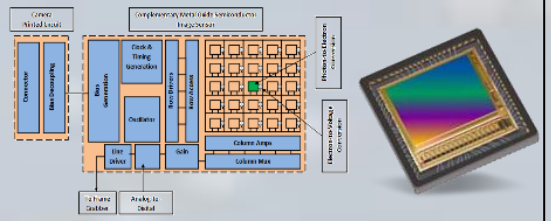
with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar

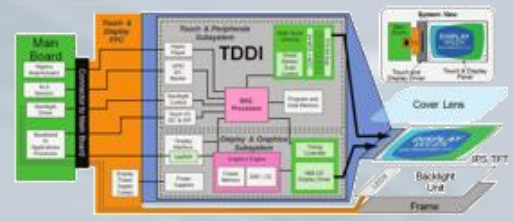


CMOS Sensor



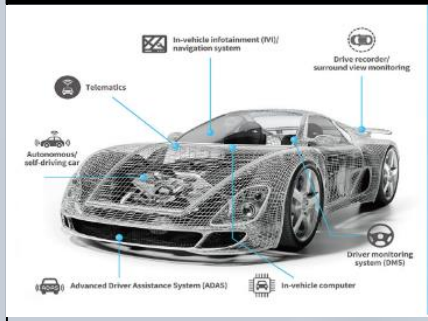


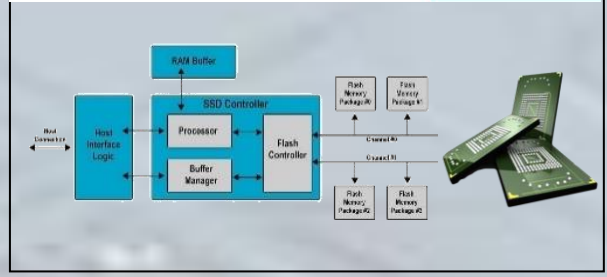
Auto TDDI



Auto MCU

Auto Storage





The Rise of

AndesAIRE™ AnDLA™ I350

The First Generation of Andes Deep Learning Accelerator

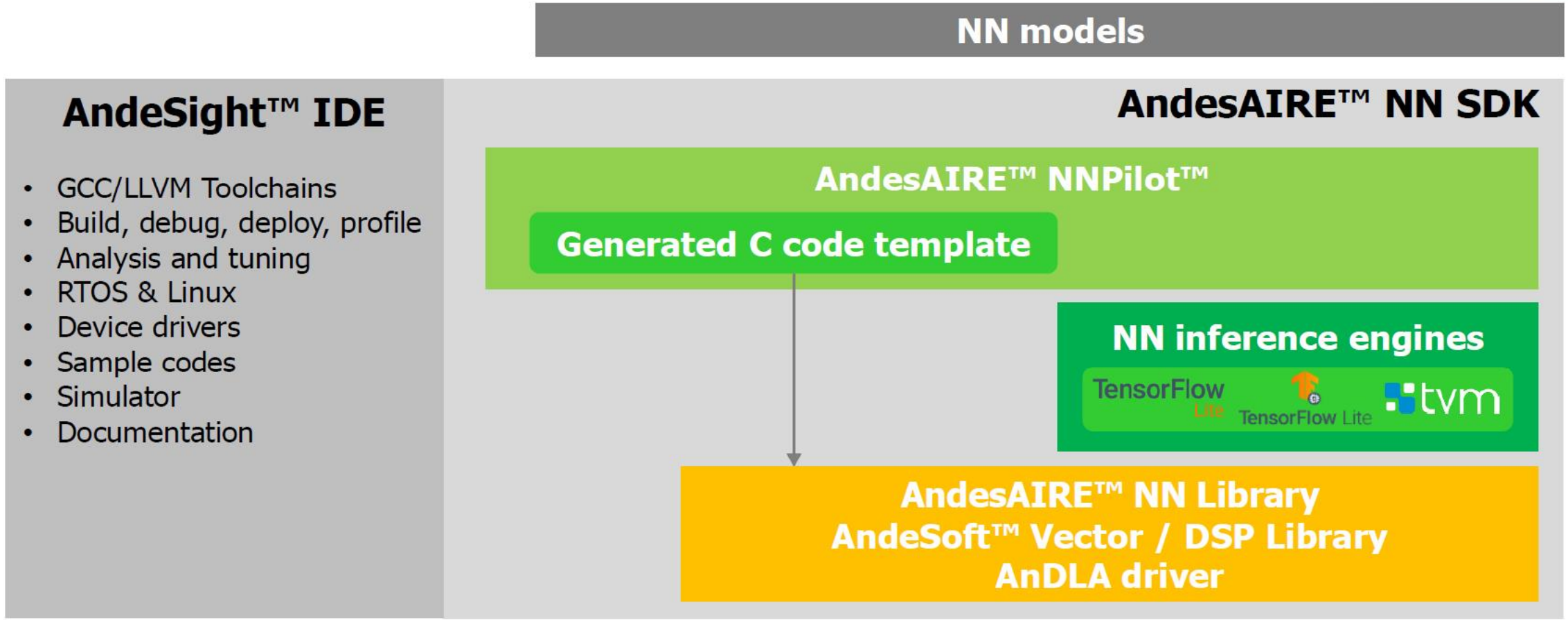
AndesAIRE™ NN SDK

Unleash the maximum AI/ML performance
and synergy of RISC-V CPU and AnDLA™

AndesAIRE™

Andes AI Runs Everywhere

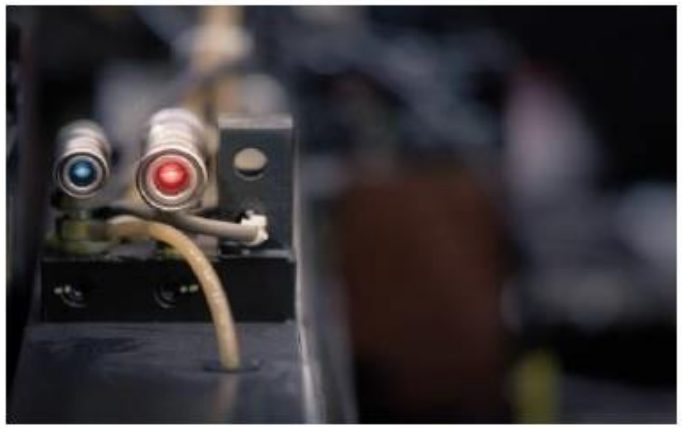
Andes AI Total Solutions



AndesAIRE™ - Andes AI Runs Everywhere

Smart Camera

Smart Sensor



Smart Home Appliance

AIoT / tinyML

Robotics

Wearable

Taking RISC-V® Mainstream

Thank You

http://www.andestech.com

+886-3-5726533

ANDES TECHNOLOGY

RISC-V®

N25F-SE Industry First ISO 26262 Full Compliance RISC-V Processor

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/20/0639 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY
TAIWAN R.O.C 30069

Project-No/-ID	LICENSED TEST MARK	Report No.
P30L	SGS TÜV SAAR FUNKTIONALE SICHERHEIT GEPRÜFT / FUNCTIONAL SAFETY APPROVED	P30L0001

Tested according to ISO 26262:2018

Certified Process Development process for Functional Safety related components up to ASIL D
Version V1.0/202011

Technical Data/Parameter The audited development process complies with the ISO 26262 standard part requirements

ISO 26262-2:2018 ISO 26262-6:2018
ISO 26262-4:2018 ISO 26262-8:2018
ISO 26262-5:2018 ISO 26262-9:2018

Specific Requirements The certificate is created for the purpose of providing conformity of the development and support process in accordance with ISO 26262. Changes which are not covered in the Audit Report have to be reconsidered.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

Munich, December 22nd, 2020

Marcus Rau

The test mark regulation is an integral part of this certificate.

CERTIFICATE

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID	LICENSED TEST MARK	Report No.
S280	SGS TÜV SAAR ASIL B COMPLIANT Functional Safety ISO 26262	S2800001

Tested according to ISO 26262:2018 (Parts 2, 4 partly, 5, 8, 9)

Certified Product(s) CPU IP "N25F-SE"
Version: R320

Technical Data/Parameter The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance with **ASIL B** requirements.

Specific Requirements The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval.
The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

The validation status is documented via SGS Certification Database.

The test mark regulation is an integral part of this certificate.

Munich, October 28th, 2022

Marcus Rau

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E-Mail: fs@sgs.com

CERTIFICATE

- ISO 26262 Certification for Development Process: ASIL-D
  - In Dec. 2020, Andes certified by SGS-TÜV Saar GmbH
- ISO-9001 QMS achieved and maintained since 2010
- ISO 26262 Edition 2018 ASIL B Compliant Certification for N25F-SE
  - ISO 26262-2,4,5,8,9
  - Covers all the sections applicable to CPU core

AndesAIRE™ AnDLA™ I350

- Andes Deep Learning Accelerator (AnDLA™)
  - High performance-efficient deep learning accelerator for edge and end-point inference
  - Scalable and multi-DLA
  - Cooperate with AndesCore™ full series (22/23/25/27/45/65)
- Accelerating for most of NN Applications
  - Image and video
  - Speech/voice and audio
- Target performance
  - Configurable MACs: 32 to 4096 (INT8)
  - Performance: 64 GOPS to 8 TOPS (INT8 @1GHz)
  - Configurable local memory: 16KB to 4MB
  - Leading power efficiency >5 TOPS/W (@28nm)
- Integrated DMA and local memory