Andes Technology Corp. Investor Conference Report
Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
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Company Overview

http://www.andestech.com
Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 330 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)
- EE Awards - “Taiwan-Product Award” & ”Asia-Company Award” (2021)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning
Business Status Overview

❖ 250+ commercial licensees
  ■ Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  ■ 600+ license agreements signed

❖ AndeSight™ IDE:
  ■ 23,000+ installations

❖ Eco-system:
  ■ 500+ partners

❖ 11B+ Accumulative SoC Shipped
Operation Results

http://www.andestech.com
3Q22 Revenue Analysis

YoY
+41%

QoQ
+93.5%

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Revenue (NT$ thousands)</th>
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</thead>
<tbody>
<tr>
<td>3Q21</td>
<td>192,228</td>
</tr>
<tr>
<td>2Q22</td>
<td>140,138</td>
</tr>
<tr>
<td>3Q22</td>
<td>271,137</td>
</tr>
</tbody>
</table>
22 Q1-Q3 Revenue Analysis

YoY +13%

(NT$ thousands)

21 Q1-Q3: 550,724
22 Q1-Q3: 622,304
22 Q1-Q3 Top 10 Customers Analysis by Revenue

(NT$ thousands)

Top 10 Customer Contributed 65% Revenue

- Touch Panel (TW)
- AT (US)
- Wireless/IoT (TW)
- Touch (US)
- FPGA (US)
- Sensing (TW)
- MCU (CN)
- Datacenter (KR)
- Video/TDD1 (CN)
- Server (CN)
3Q22 Royalty Analysis

YoY -7.5%  QoQ +7.7%

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Royalty (NT$ thousands)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3Q21</td>
<td>65,668</td>
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<tr>
<td>2Q22</td>
<td>56,379</td>
</tr>
<tr>
<td>3Q22</td>
<td>60,745</td>
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</tbody>
</table>
22 Q1-Q3 Royalty Analysis

YoY
+4.2%

(NT$ thousands)

170,904
178,112

21 Q1-Q3          22 Q1-Q3
22 Q1-Q3 Top 10 Royalty Contributors Analysis by Application

(NT$ thousands)

Top 10 Royalty Customers Contribution Analysis: 86%
22 Q1-Q3 Revenue Analysis by Payment Model

- License Fee: 56%
- Running Royalty: 29%
- Maintenance: 14%
- Others: 1%

Andes Technology
22 Q1-Q3 Revenue Analysis by Region

- Taiwan: 39%
- USA: 29%
- China: 6%
- Korea: 2%
- Europe: 1%
- Japan: 1%
3Q22 Revenue Analysis - RISC-V

(NT$ thousands)

- 3Q21: V3 79,530, RISC-V 112,698
  - V3: 41%, RISC-V: 59%
- 2Q22: V3 60,920, RISC-V 79,218
  - V3: 43%, RISC-V: 57%
- 3Q22: V3 53,880, RISC-V 217,257
  - V3: 20%, RISC-V: 80%
Andes Updates

- A 17-year-old public CPU IP company
- 3B+ Andes-Embedded SoC annually in 2021

- A founding premier member of the RISC-V International
- An active role in RISC-V International & its extension task groups
  - RISC-V Board Director
  - Member of Technical Steering Committee
  - RISC-V Ambassador
  - Chair of P-xtension (Packed DSP/SIMD) Task Group
  - Chair of IOPMP Task Group
  - Vice Chair of Fast Interrupt Task Group

- A major open source maintainer/contributor
Andes Embedded in Various Applications

- Smart Speakers: WiFi IoT
- Bike Sharing: GPS Ctrl
- X-Trail: ADAS Ctrlr
- Switch: Game Flash Ctrlr

- In leading **machine learning computers** for datacenter
- In tier-one **switch routers** for datacenter
- Recent applications: **5G networking, WiFi 6/7, AI processors** (using Andes Custom Extension, ACE)
V5 Adoptions: From MCU to Datacenters

- **Edge to Cloud**
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)

- **40nm to 5nm**
- **Many in AI**

- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells
Andes RISC-V Cores Adopted in SoC
New Products and Ecosystems

http://www.andestech.com
Andes RISC-V Product Overview

- **AndeStar™ Architecture V5**: Best extensions to RISC-V; EDA tools
- **AndesCore™ Processors**: Highly optimized designs with leading PPA
- **AndeSight™ Tools**: Professional IDE with high code quality
- **AndeShape™ Platforms**: Handy peripheral IPs to speed up SoC construction
- **AndeSoft™ Stacks**: Extensive SW stacks from bare metal, RTOS to Linux; NN lib
Andes V5 Architecture for All Levels of Computing

**AndeStar™ V5 CPUs**

- **N/D-series**
  - N22 N(X)25 D25...
- **A-series**
  - A(X)25 A(X)27 A(X)45 Multicore...
- **Vector**
  - NX27V NX45V...

**Conventional Computing Architecture**

- Leading PPA Embedded Processor
  - IoT, Sensing, Storage, Audio, GPS
- High Performance and Power Efficient AP
  - 5G, AI, Datacenter, Video Surveillance, Networking

**Domain Specific Architecture (DSA)**

- Define custom instruction to handle time critical codes
- Better approach for accelerator/co-processor to do particular jobs
- Automation Tool for the generation of toolchain, ISS, partial RTL and verification

**Andes Custom Extension**

- Cray Style, Scalable Vector Processor
  - Datacenter, Server, Deep Learning
Andes RISC-V Product Roadmap

RV32/RV64

- Cache-Coherent 1-4 Cores
- Linux with FPU/DSP
- Fast/Compact with FPU/DSP
  - Automotive Grade

- N22 2-stage (700 MHz) >3.56 Coremark/MHz
- A25 MP AX25MP
- A25 MP AX25

Vector Ext.

- 27-Series:
  - MemBoost
  - NX27V
  - A27/AX27
  - A27L2/AX27L2
  - 5-stage (1.1 GHz) >3.56 Coremark/MHz

- 45-Series:
  - Dual Issue MemBoost
  - N45/NX45
  - D45
  - A45/AX45
  - A45MP/AX45MP (1-8 Cores)
  - 8-stage (1.2 GHz) >5.63 Coremark/MHz

Superscalar

- 45-Series:
  - Dual Issue MemBoost
  - N45/NX45
  - D45
  - A45/AX45
  - A45MP/AX45MP (1-8 Cores)
  - 8-stage (1.2 GHz) >5.63 Coremark/MHz

Benefits

- 512-bit SIMD raises MobileNet by 66x (CNN for mobile vision)
- Boost performance by 50%
- Raise bandwidth to 3x; Cut latency by 40%

Leading positions:

❖ The 1st company offering commercial RVP DSP CPU
❖ The 1st company offering the most updated spec of commercial RVV vector processor
❖ Tools for RISC-V custom extension: ACE
❖ The 1st RISC-V core certified for ISO 26262 full compliance
Powering Automotive Applications by Andes RISC-V

Clusters are evolving from analog meters and gauges to all-digital clusters. It offers an intuitive user interface to present this information in an ergonomic and easy-to-consume manner.

Instrument Cluster

Low Power Radar

In-Cabin Radar SoC builds Driver Monitoring System and Occupant Detection – detect head movement and body language for indications that the driver is drowsy.

ECU

High-performance microcontrollers provide great computing power, safe control and rich multimedia capabilities.

Touch & Display

Automotive TDDIs are designed to feature information integration, interactive entertainment, as well as the pursuit of stylish, large, and curved screen design.

Taking RISC-V® Mainstream
AndeCore™ 45-Series

32-bit AndesCore™ N45/D45/A45/A45MP
64-bit AndesCore™ NX45/AX45/AX45MP
AndesCore™ 45-Series Overview

- 8-stage In-Order Dual-Issue
- AndeStar™ V5 ISA:
  - RV*GCN (S/D FPU): All Series
  - RV*P-ext (DSP/SIMD): D45/A(X)45
  - MMU for Linux Applications: A(X)45
- MemBoost memory subsystem
- Low power dynamic branch prediction
- Unaligned data accesses
- Fast or small multiplier
- StackSafe™ (Andes Ext.)
- CoDense™ (Andes Ext.)
- Multi-core support: A(X)45MP
  - Up to 8 cores
AX45 Can Do More (vs. 64bit A-series)

<table>
<thead>
<tr>
<th></th>
<th>Coremark/MHz</th>
<th>Dhrystone/MHz</th>
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<tbody>
<tr>
<td>A53</td>
<td>4.18</td>
<td>2.3</td>
</tr>
<tr>
<td>Andes AX45</td>
<td>5.63</td>
<td>3.27</td>
</tr>
</tbody>
</table>

- **A53**
  - 8-stage In-Order Dual Issue
  - Widely adopted by industries in many applications

- **AX45**
  - 8-stage In-Order Dual Issue
  - Performance is better!
    - Coremark/MHz: 1.35x
    - Dhrystone/MHz: 1.42x
Target Applications for 27 & 45-Series

- AI/Deep Learning
- AR/VR
- 5G
- Networking
- Storage
- Video Surveillance
- ADAS
- V2X (Vehicle to Everything)
- IVI (In-Vehicle-Infotainment)
- Metaverse and more...
Bring Andes Strength to RISC-V Cores

**Performance & Extensibility**
- Leading PPA and code size
- Rich data processing in P, V, and ACE

**Configurability**
- Flexible configurations for rich features

**Maturity**
- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE
Successfully rolled out new RISC-V cores (w/ leading P-/V-/Custom-Ext. and ISO 26262 full compliance), custom computing service and FreeStart program to extend more oppy.

Aggressively involved in RISC-V International new technology development, contributing and leveraging RISC-V eco-system.

Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry.
Thank You

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