



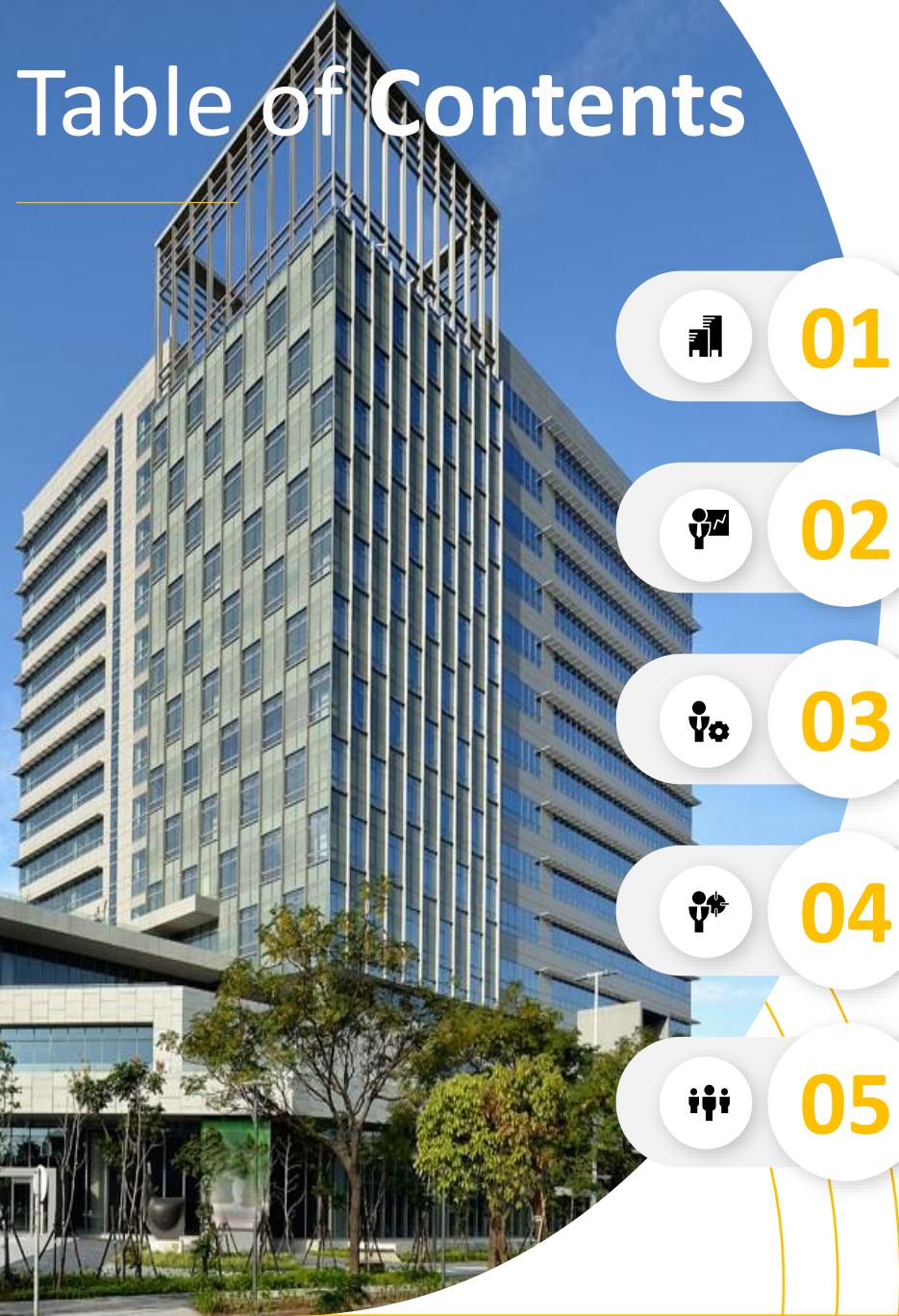
Andes Technology Corp. Investor Conference Report

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

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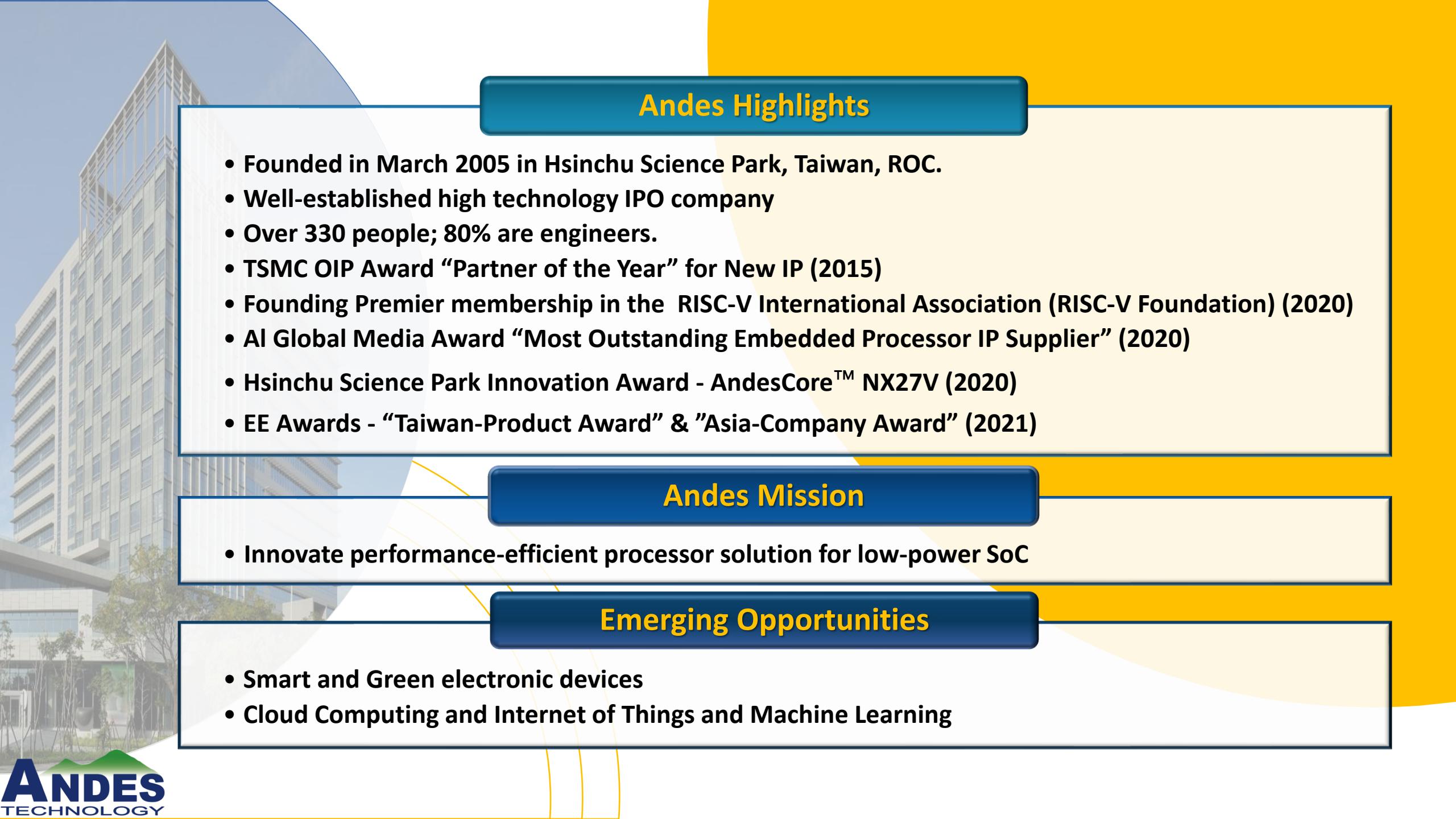
Concluding Remarks



Company Overview

<http://www.andestech.com>





Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 330 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)
- EE Awards - “Taiwan-Product Award” & “Asia-Company Award” (2021)

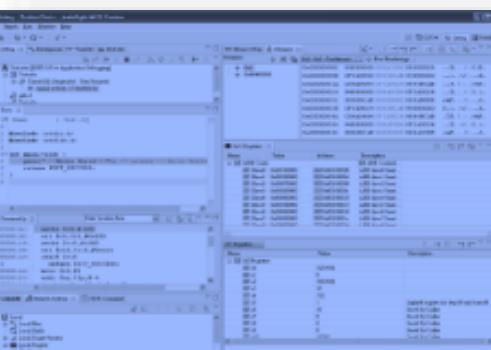
Andes Mission

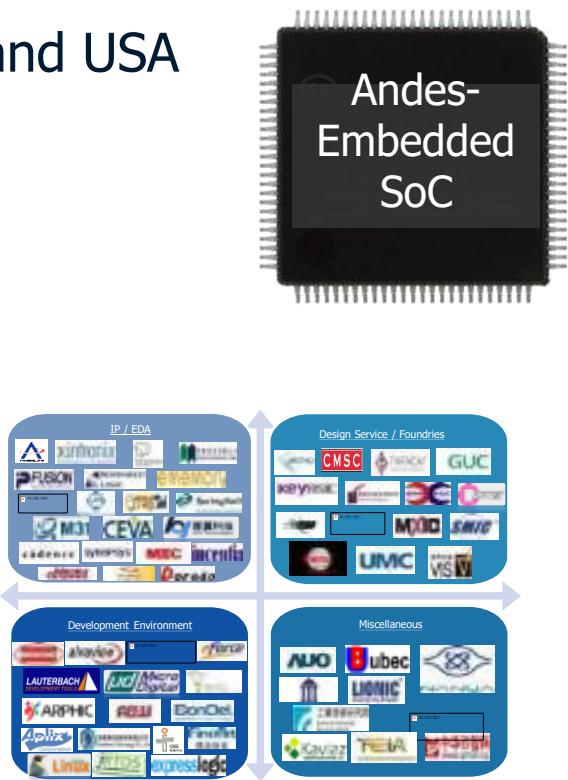
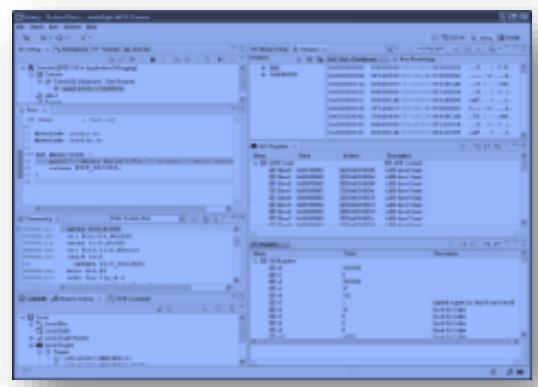
- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

Business Status Overview

- ❖ **250+** commercial licensees
 - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
 - **600+** license agreements signed
 - ❖ AndeSight™ IDE:
 - **23,000+** installations
 - ❖ Eco-system:
 - **500+** partners
 - ❖ **11B+** Accumulative SoC Shipped



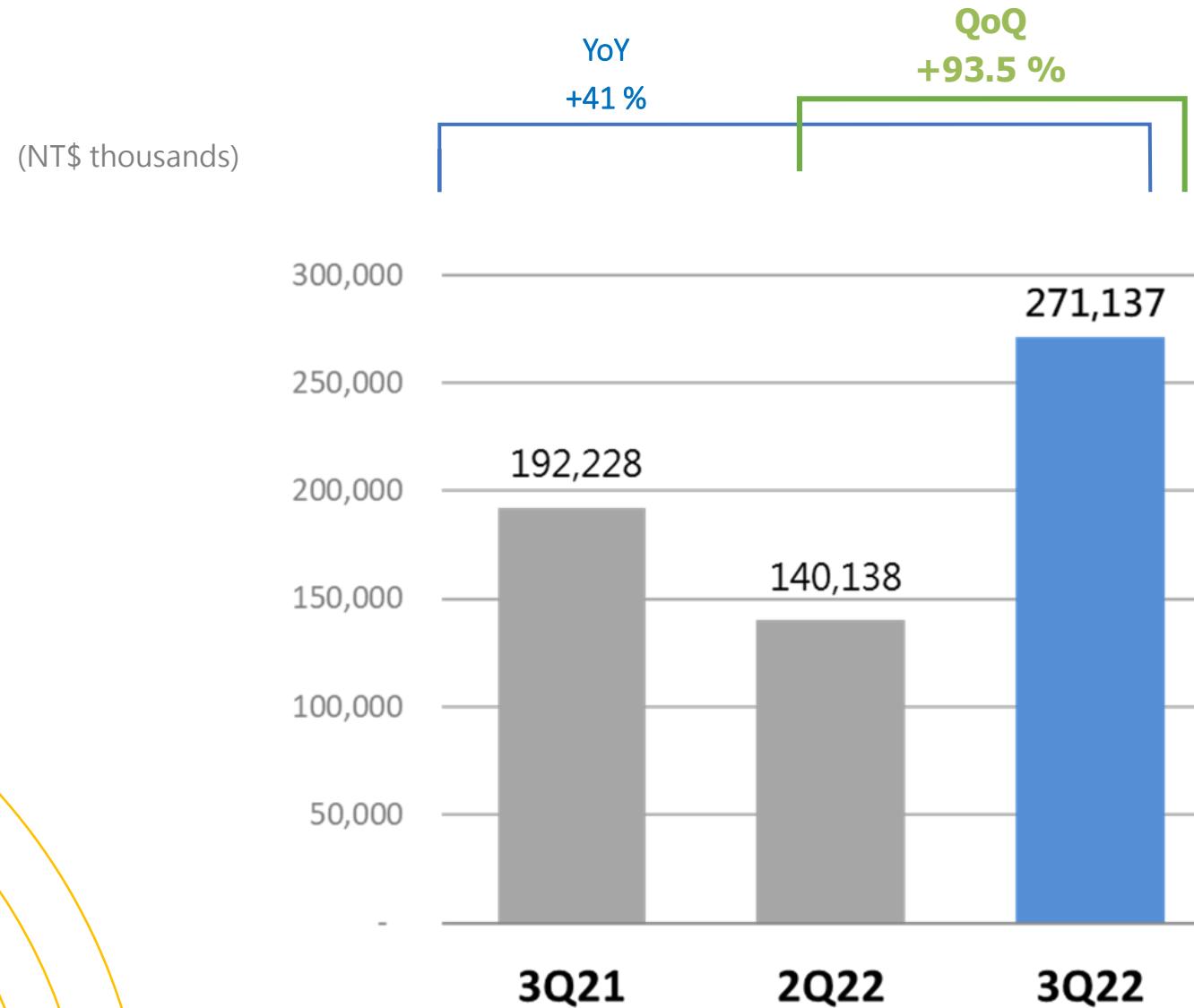


Operation Results

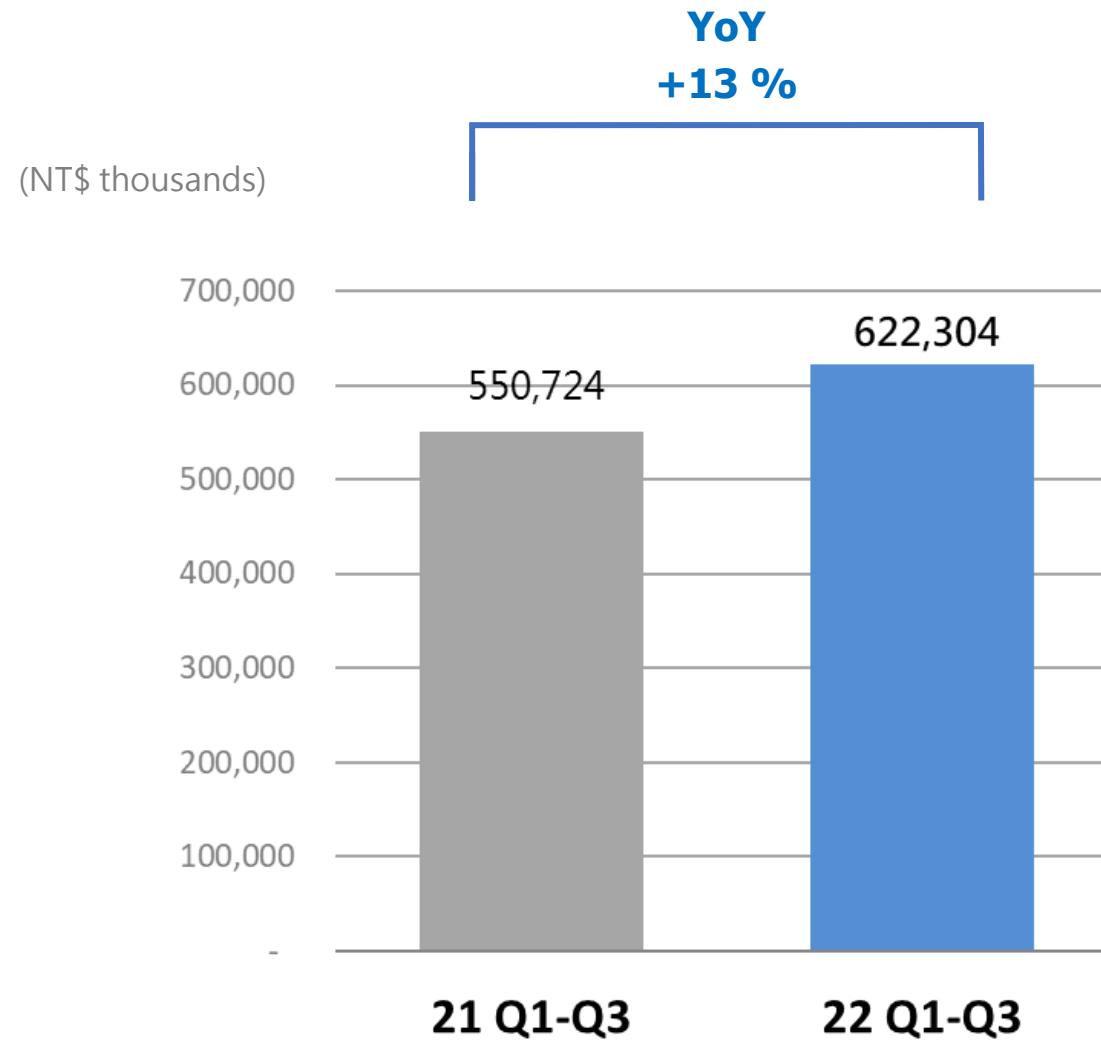
<http://www.andestech.com>



3Q22 Revenue Analysis



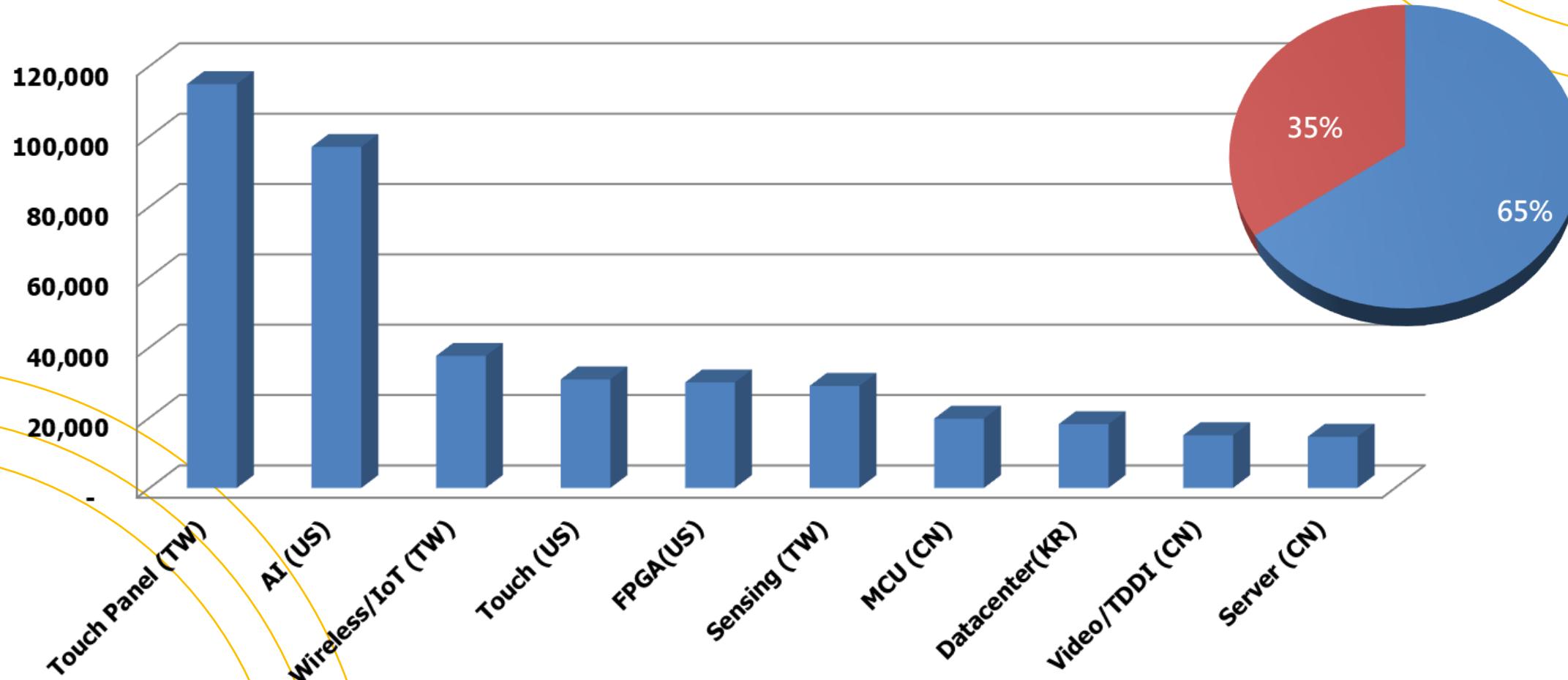
22 Q1-Q3 Revenue Analysis



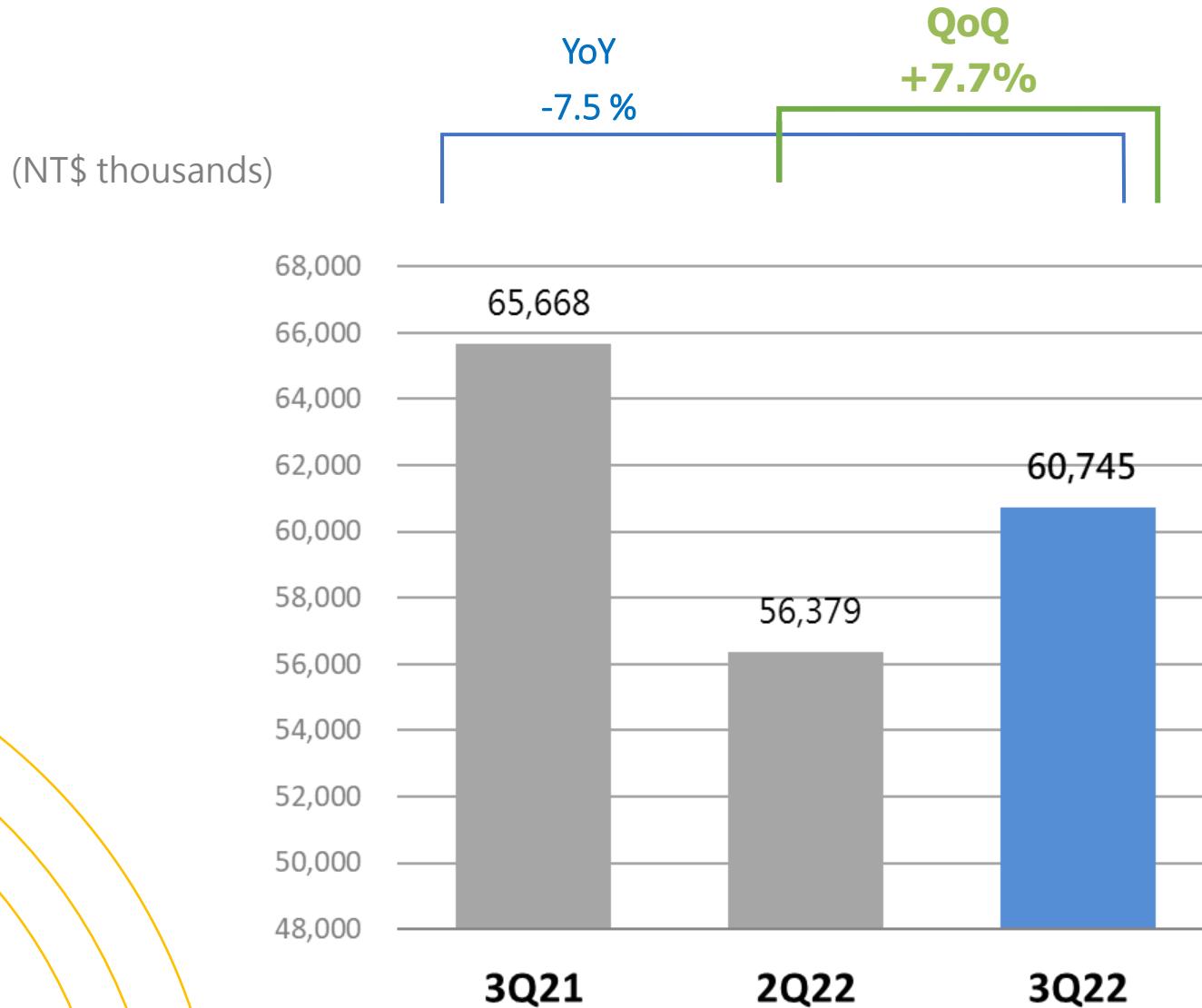
22 Q1-Q3 Top 10 Customers Analysis by Revenue

(NT\$ thousands)

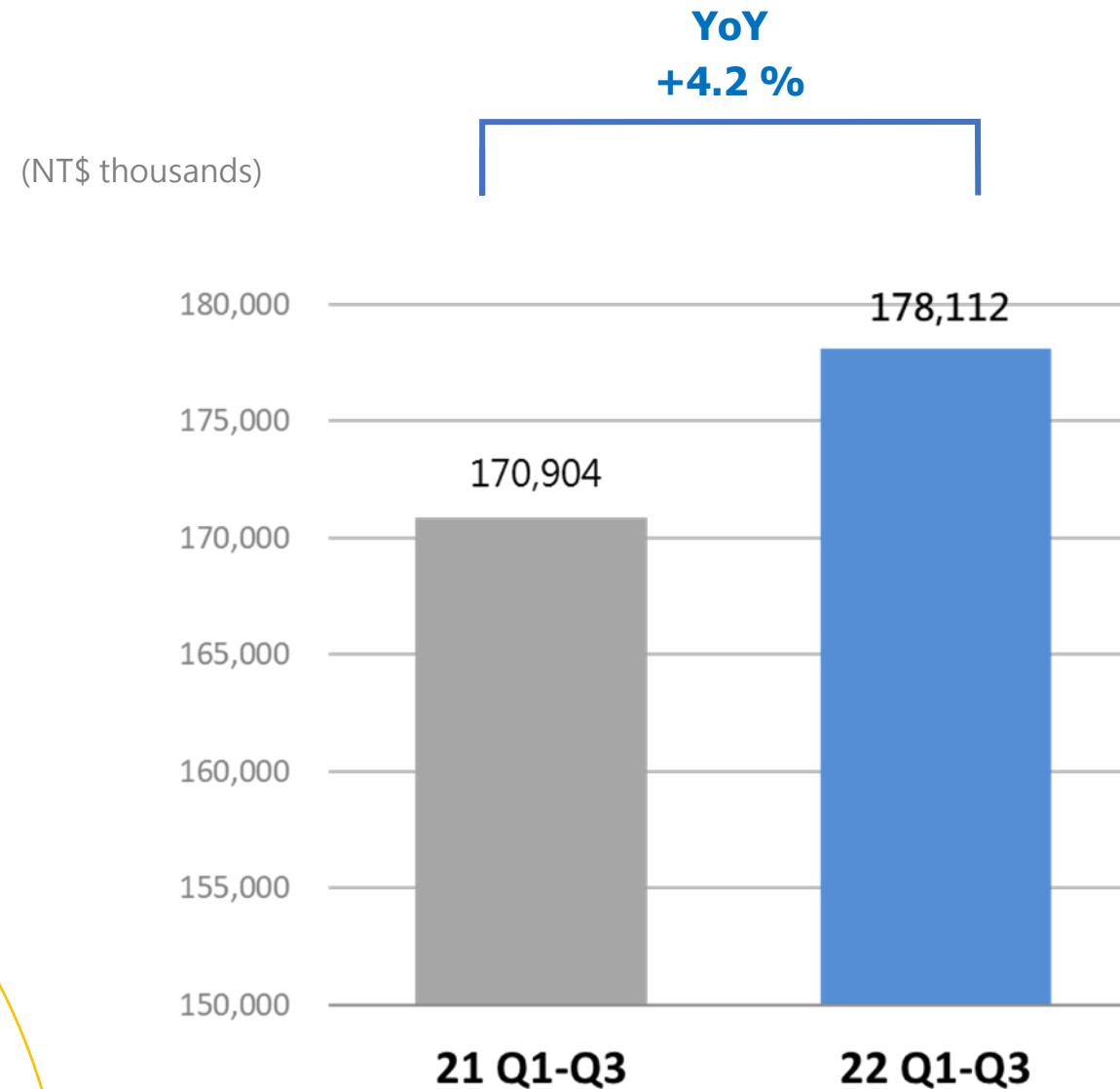
Top 10 Customer Contributed 65% Revenue



3Q22 Royalty Analysis



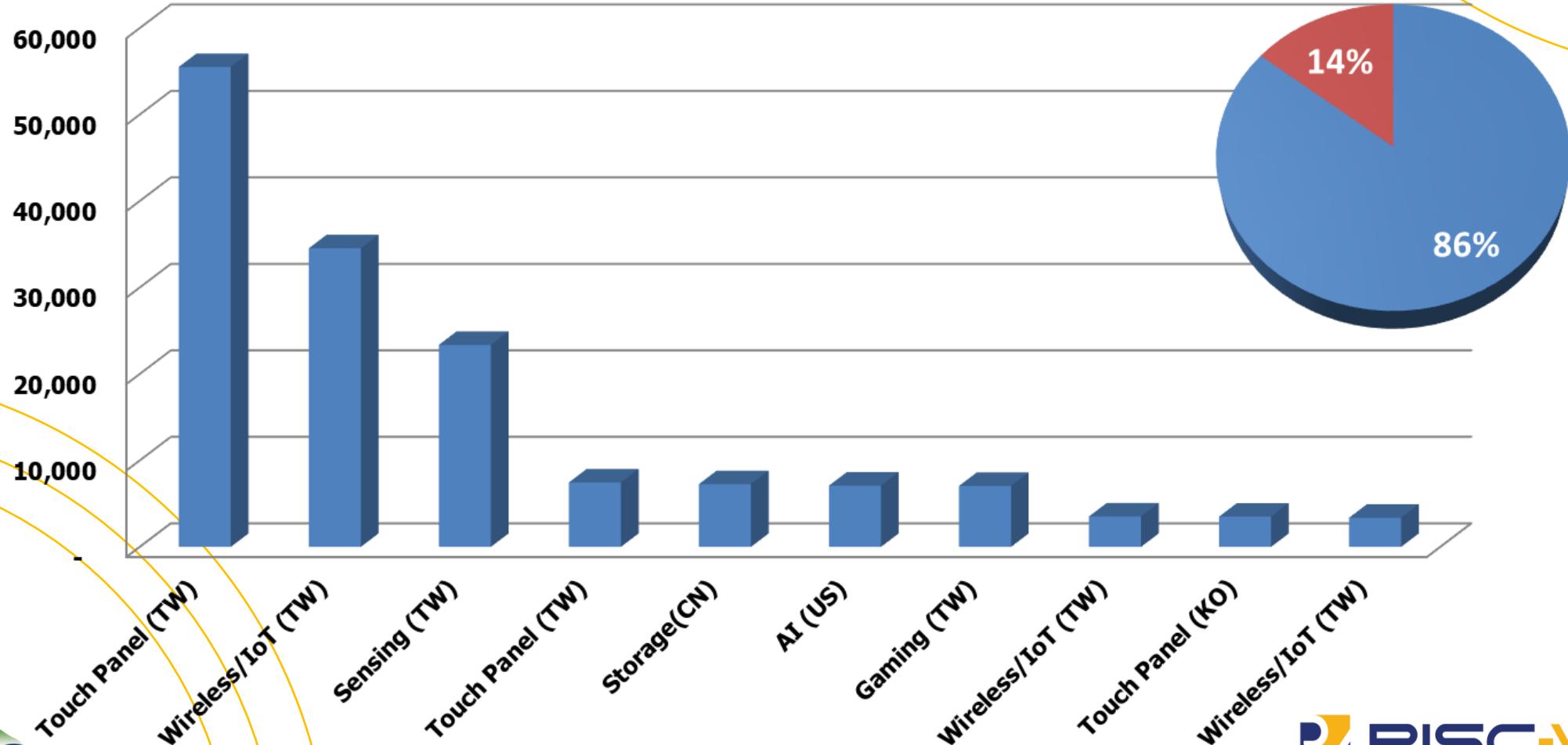
22 Q1-Q3 Royalty Analysis



22 Q1-Q3 Top 10 Royalty Contributors Analysis by Application

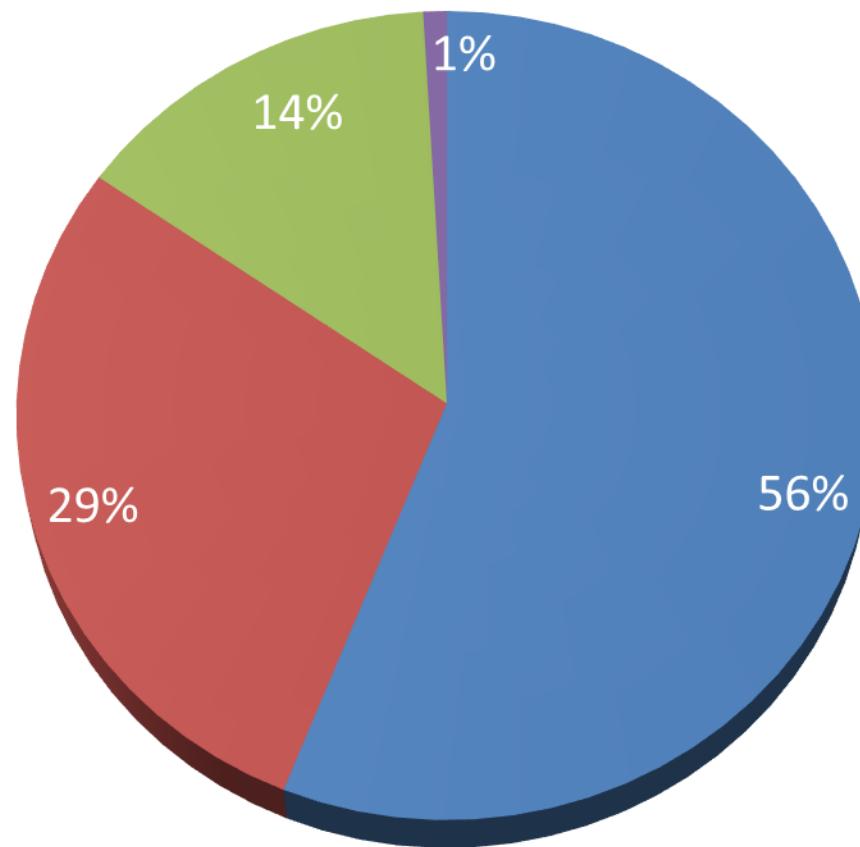
(NT\$ thousands)

Top 10 Royalty Customers
Contribution Analysis: 86%



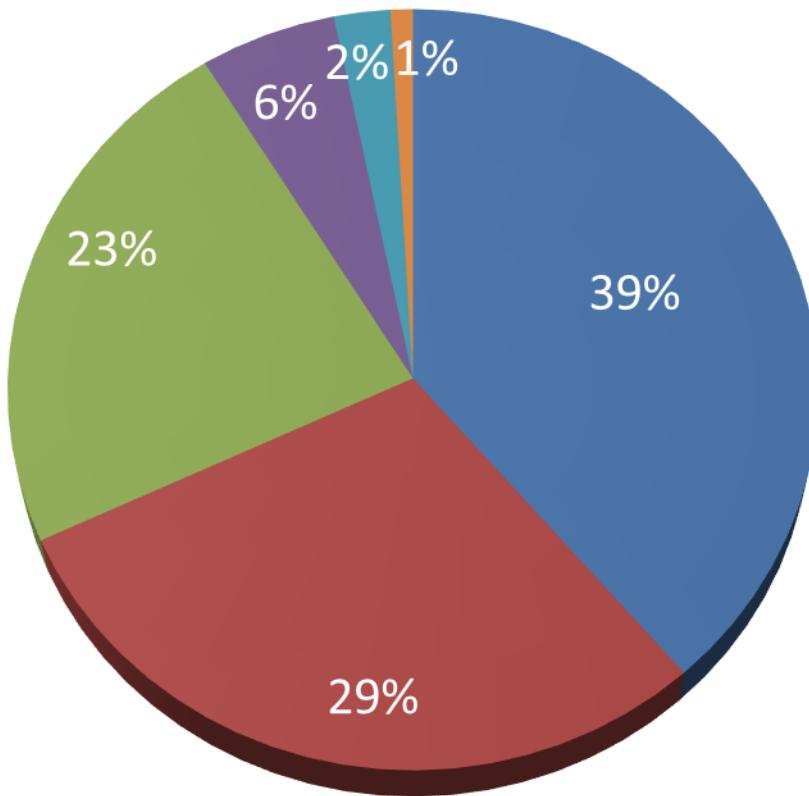
22 Q1-Q3 Revenue Analysis by Payment Model

■ License Fee ■ Running Royalty ■ Maintenance ■ Others

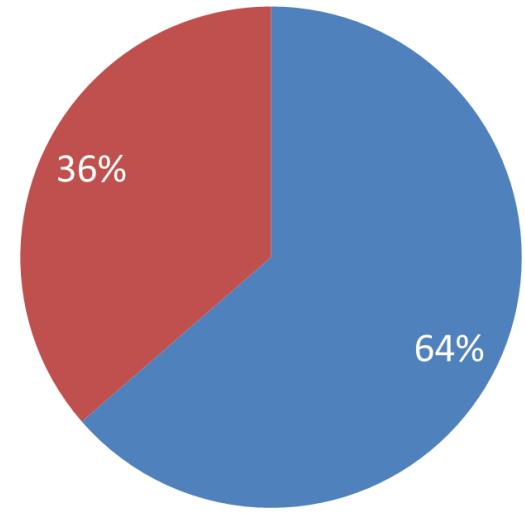


22 Q1-Q3 Revenue Analysis by Region

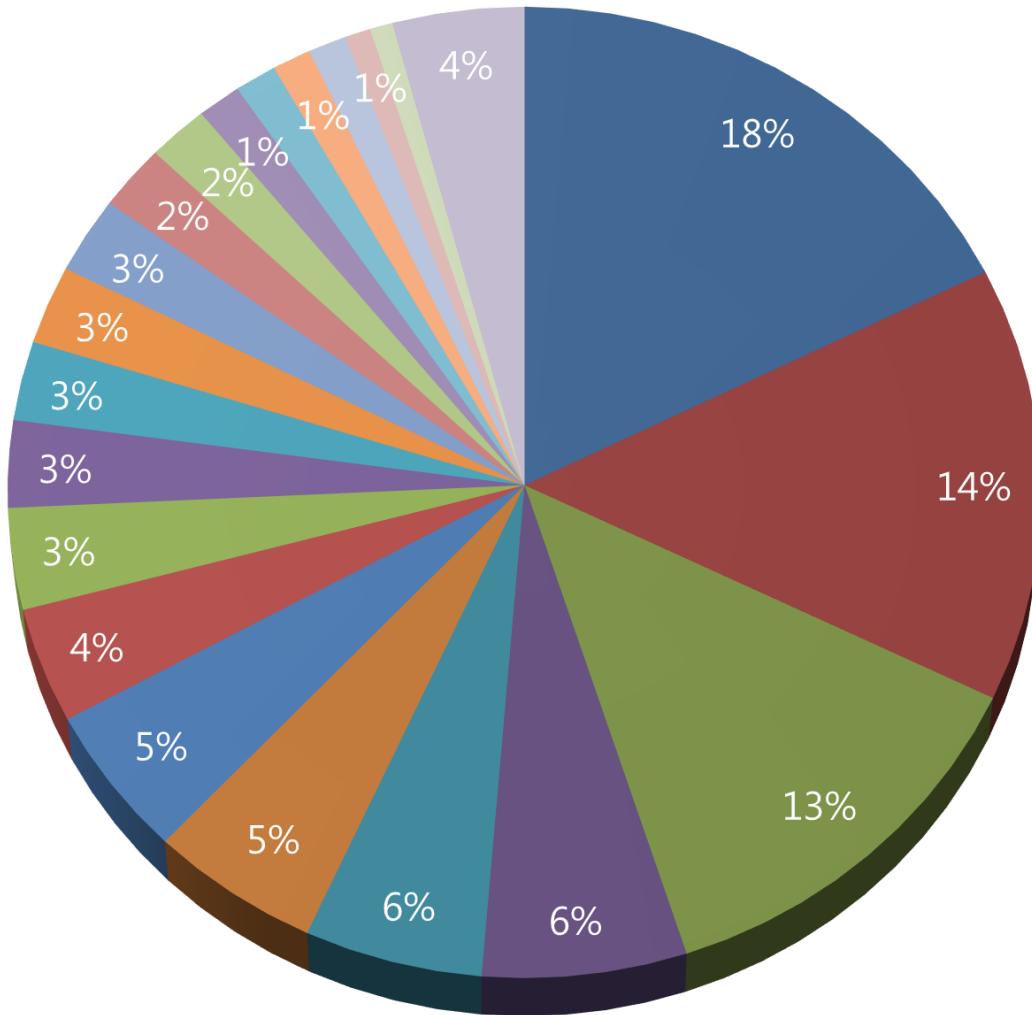
■ Taiwan ■ USA ■ China ■ Korea ■ Europe ■ Japan



22 Q1-Q3 Revenue Analysis by Product



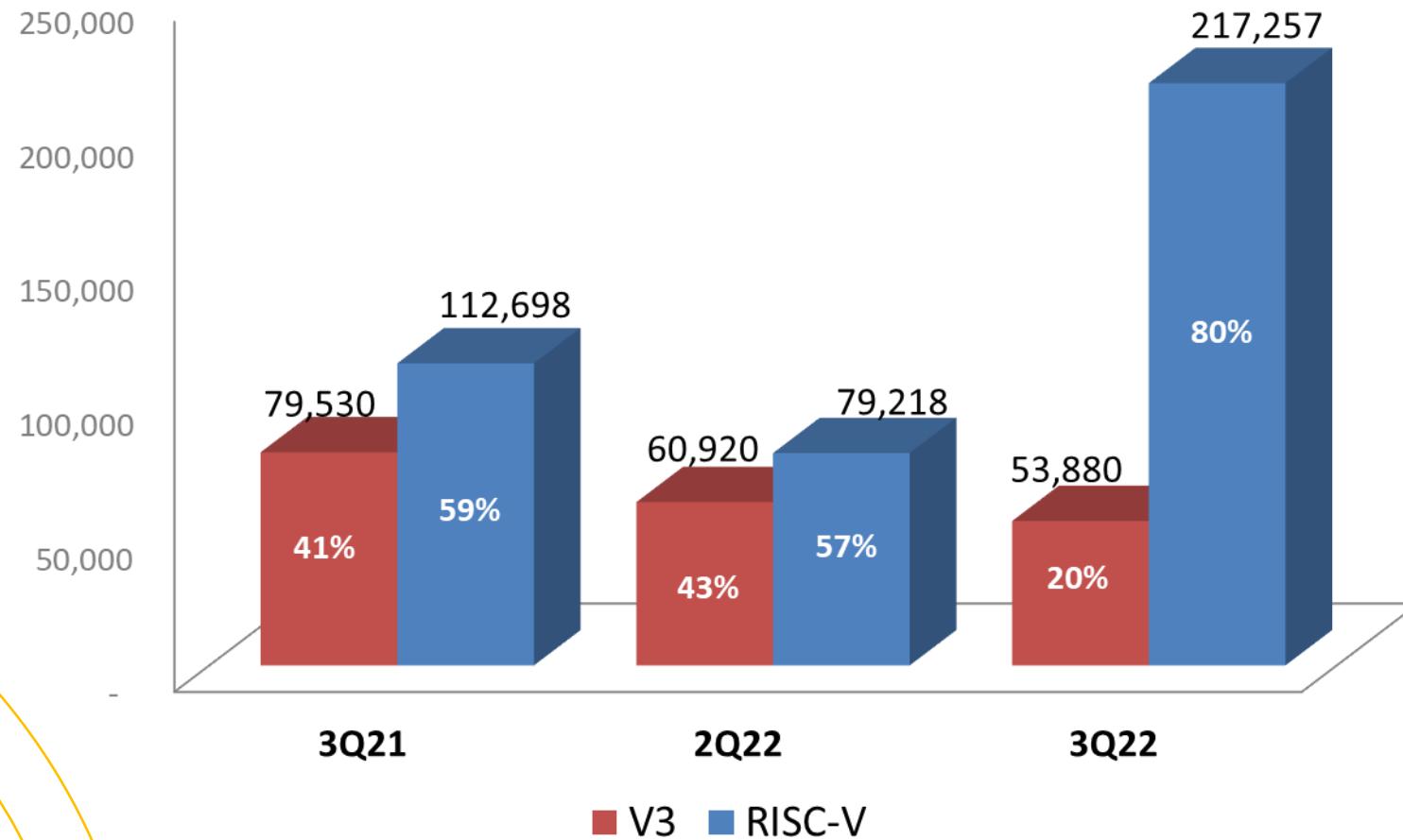
■ RISC-V
■ V3



- N25
- N9
- N8
- AX45
- Customized IP
- A45
- NX27
- N13
- D45
- AX25
- N45
- NX25
- ACE
- N10
- D25
- E8
- LLVM
- N22
- AE250
- N7
- IAR
- OTHERS

3Q22 Revenue Analysis - RISC-V

(NT\$ thousands)





Product Applications

<http://www.andestech.com>



Andes Updates

- ❖ A 17-year-old public CPU IP company
- ❖ 3B+ Andes-Embedded SoC annually in 2021



- ❖ A **founding premier** member of the RISC-V International
- ❖ An active role in RISC-V International & its extension task groups
 - RISC-V Board Director
 - Member of Technical Steering Committee
 - RISC-V Ambassador
 - Chair of P-xtension (Packed DSP/SIMD) Task Group
 - Chair of IOPMP Task Group
 - Vice Chair of Fast Interrupt Task Group
- ❖ A major open source maintainer/contributor

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports rv64i-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

GNU Toolchains

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM port
 - Talk yesterday afternoon
 - Poster on Tuesday night
- RV32IM(A)FI support upstream
 - Missing hard-float calling convention
 - Missing 64-bit support
 - Missing compressed support
- Clang, Go, and OpenJDK have run code
 - Build port in progress
 - Poster on Tuesday

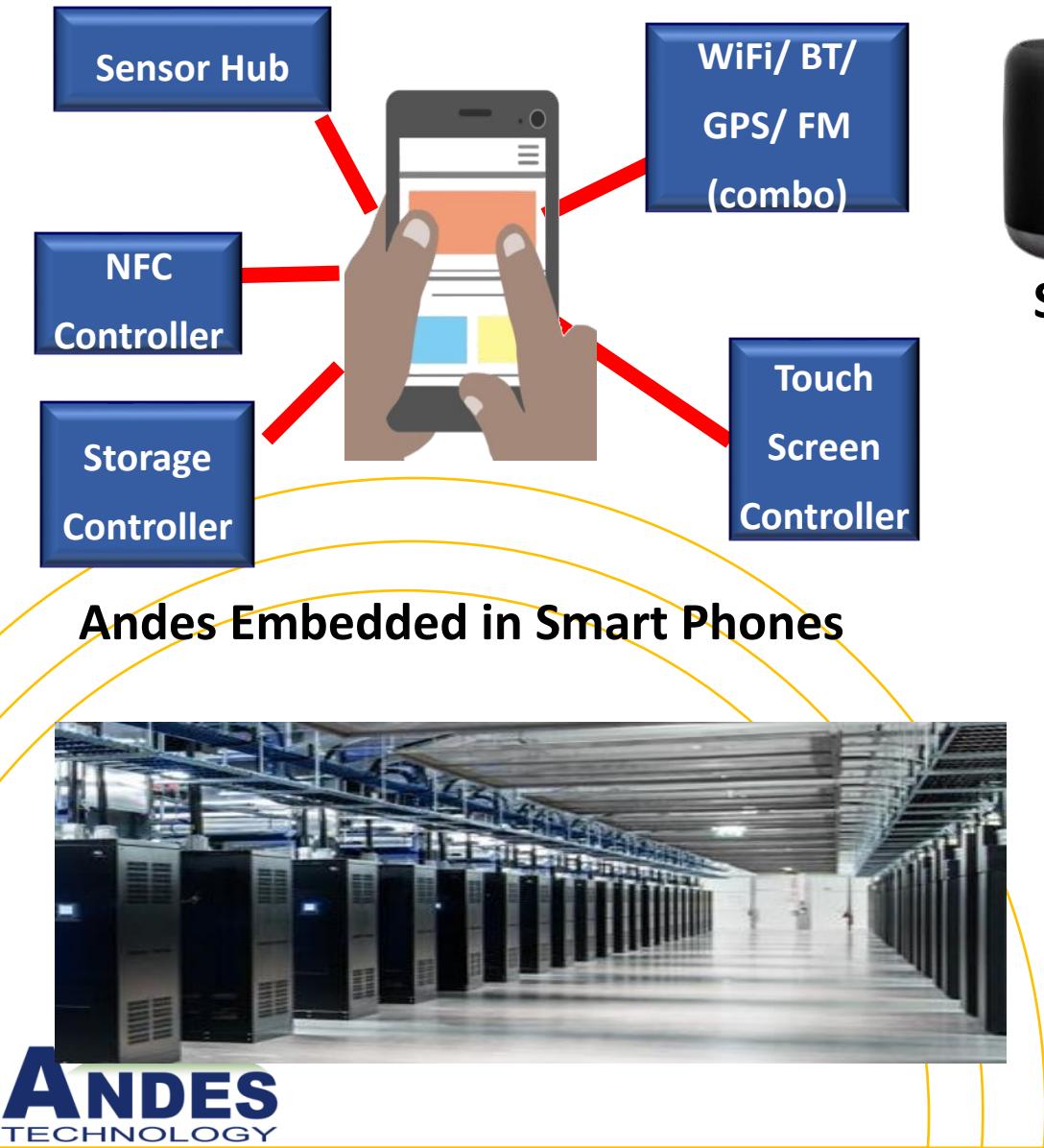
LLVM

RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64i-based systems
 - Drivers are trickling in now

Linux

Andes Embedded in Various Applications



Smart Speakers:
WiFi IoT



Bike Sharing:
GPS Ctrl



X-Trail:
ADAS Ctrl



Switch:
Game Flash Ctrl

- ❖ In leading **machine learning computers** for datacenter
- ❖ In tier-one **switch routers** for datacenter
- ❖ Recent applications: **5G networking, WiFi 6/7, AI processors** (using Andes Custom Extension, ACE)

V5 Adoptions: From MCU to Datacenters

❖ Edge to Cloud

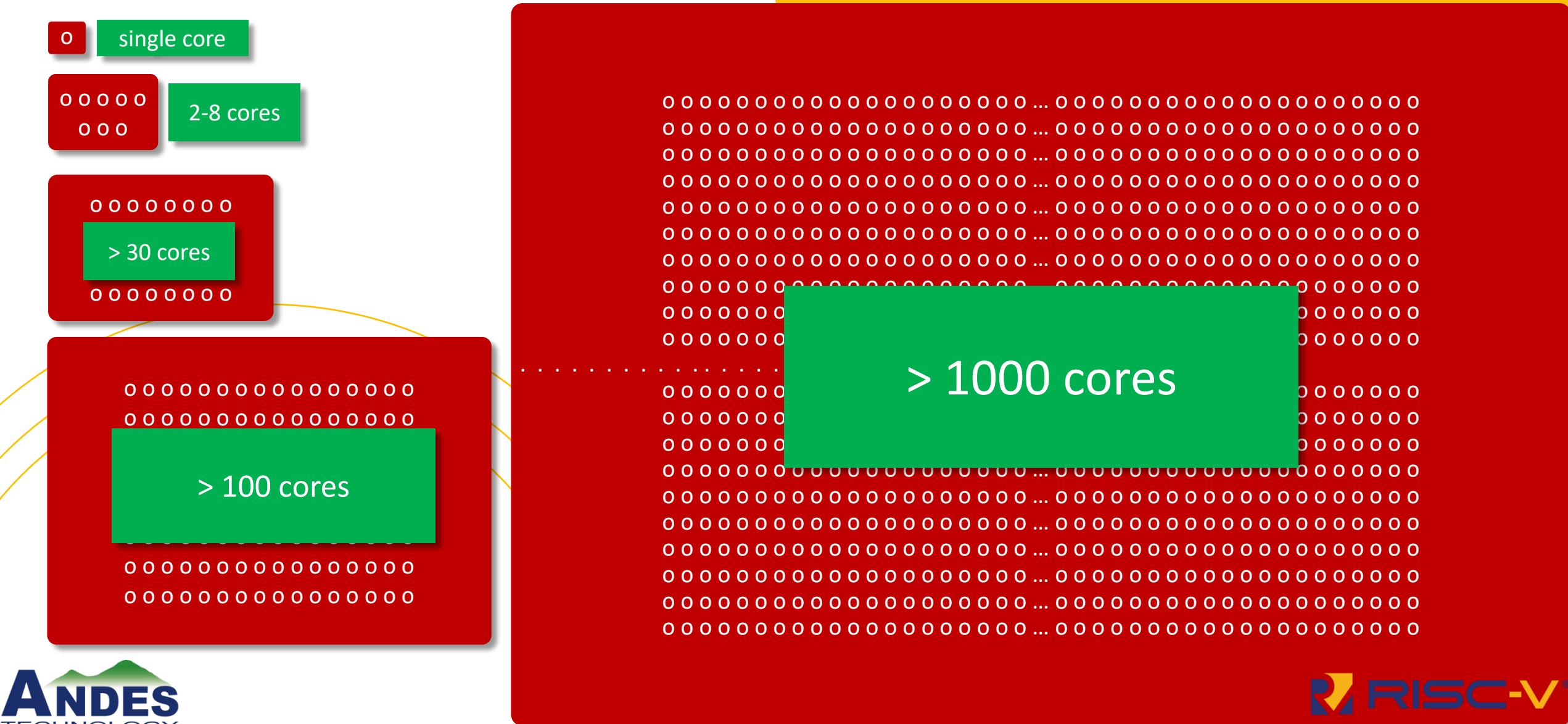
- ADAS
- AIoT
- Blockchain
- FPGA
- MCU
- Multimedia
- Security
- Wireless (BT/WiFi)
- Datacenter/server AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

❖ 40nm to 5nm

❖ Many in AI



Andes RISC-V Cores Adopted in SoC



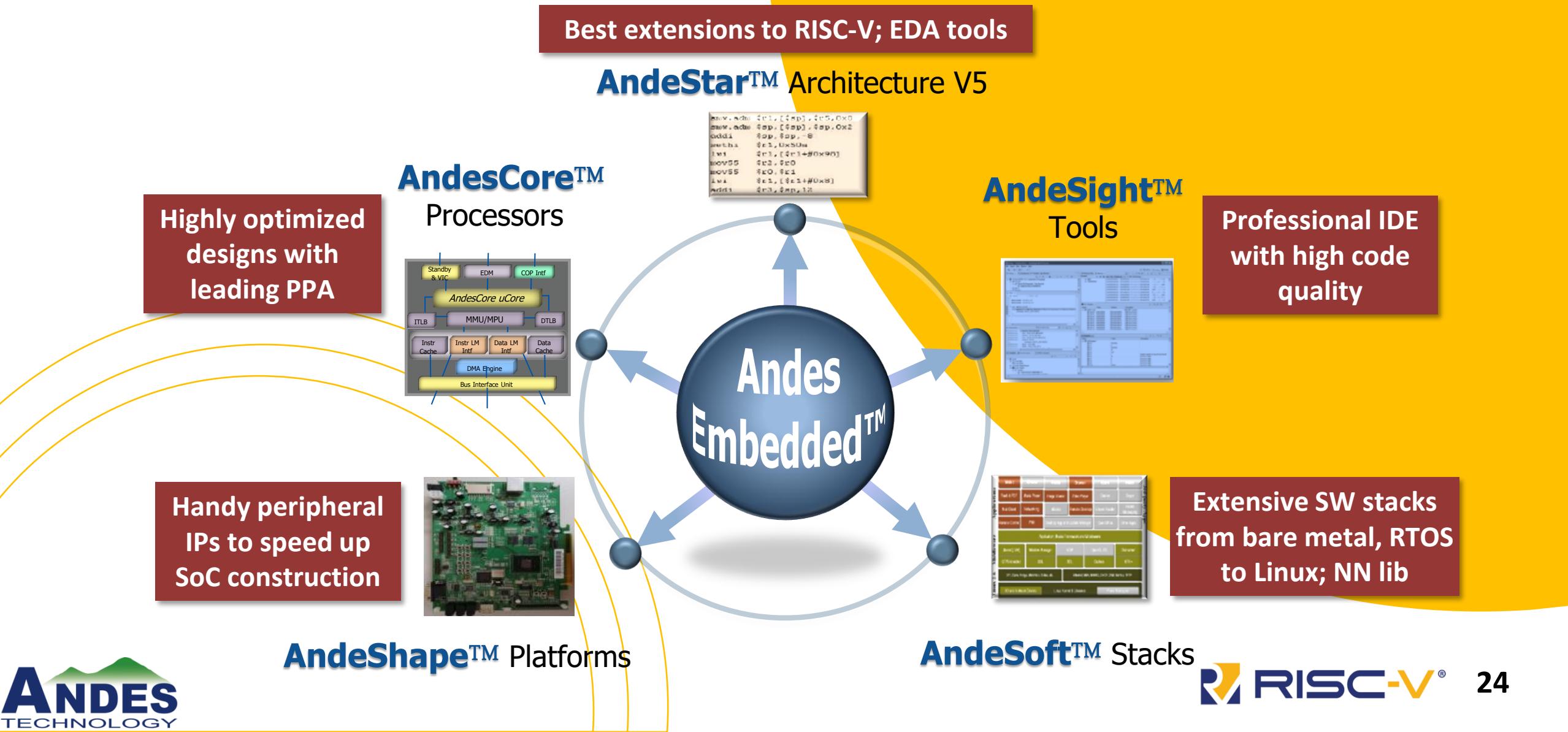


New Products and Ecosystems

<http://www.andestech.com>



Andes RISC-V Product Overview



Andes V5 Architecture for All Levels of Computing

AndeStar™ V5 CPUs



RV32/64



Andes Extension

N/D-series

N22 N(X)25 D25...

A-series

A(X)25 A(X)27 A(X)45
Multicore...

Vector

NX27V NX45V...

Conventional Computing Architecture

Leading PPA Embedded Processor

IoT, Sensing, Storage, Audio, GPS

High Performance and Power Efficient AP

5G, AI, Datacenter, Video Surveillance, Networking

Cray Style, Scalable Vector Processor

Datacenter, Server, Deep Learning

Domain Specific Architecture (DSA)



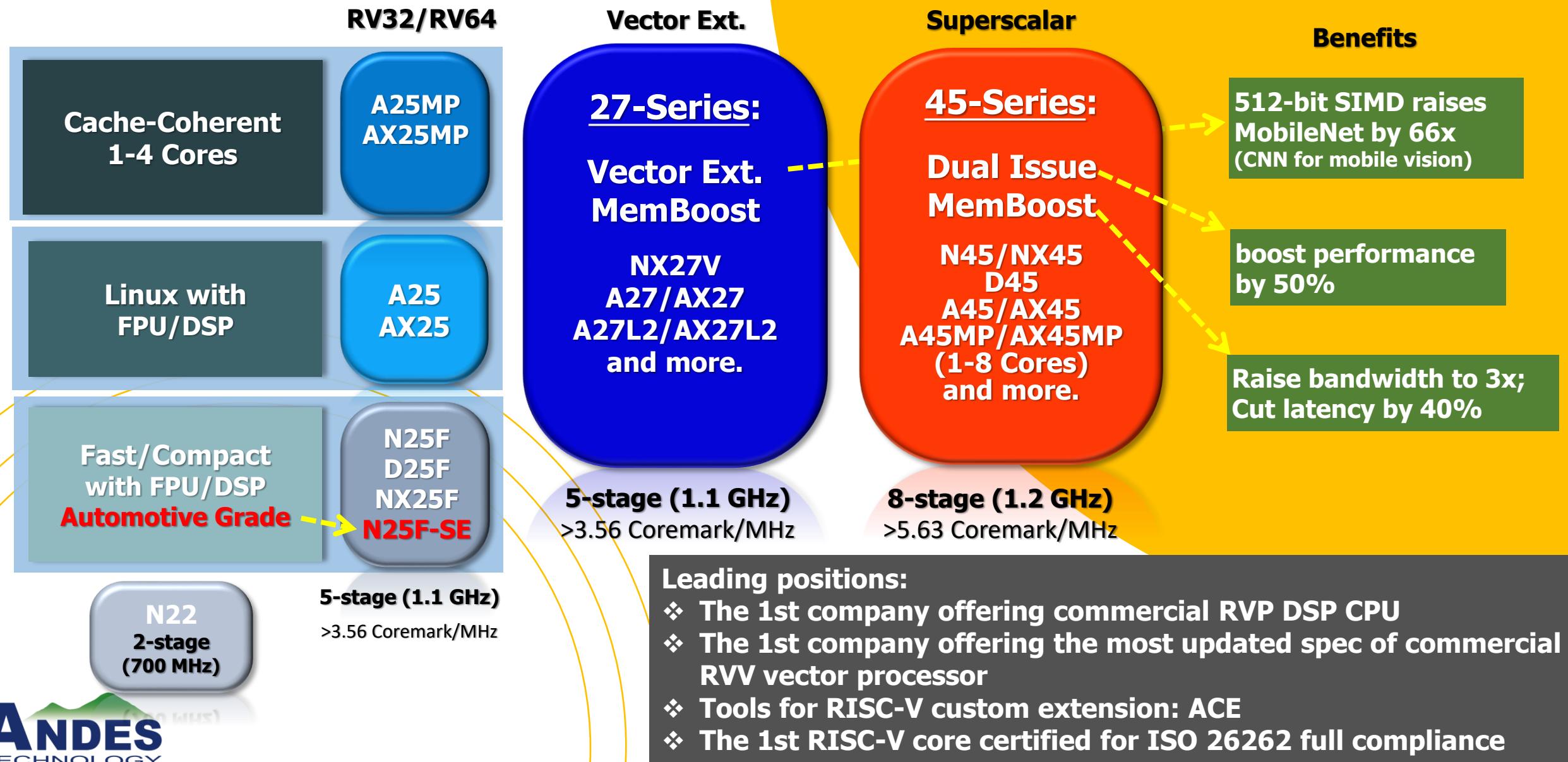
Define custom instruction to handle time critical codes

Andes Custom Extension

Better approach for accelerator /co-processor to do particular jobs

Automation Tool for the generation of toolchain, ISS, partial RTL and verification

Andes RISC-V Product Roadmap

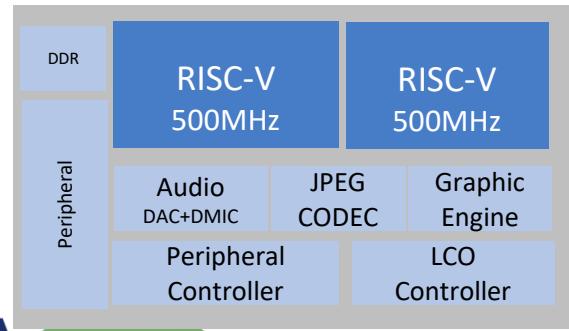


Powering Automotive Applications by Andes RISC-V

Instrument Cluster



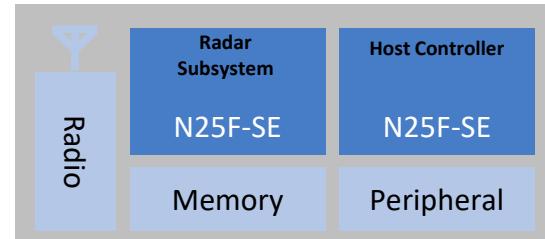
Clusters are evolving from analog meters and gauges to all-digital clusters. It offers an intuitive user interface to present this information in an ergonomic and easy-to-consume manner



Low Power Radar



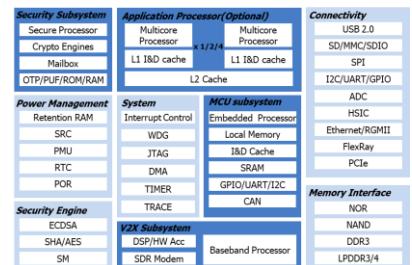
In-Cabin Radar SoC builds Driver Monitoring System and Occupant Detection – detect head movement and body language for indications that the driver is drowsy



ECU



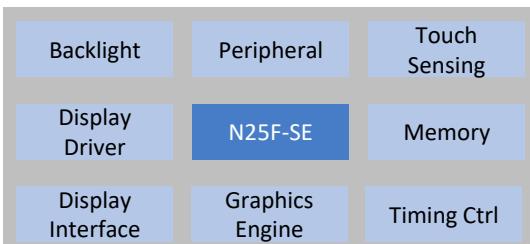
High-performance microcontrollers provide great computing power, safe control and rich multimedia capabilities



Touch & Display



Automotive TDDIs are designed to feature information integration, interactive entertainment, as well as the pursuit of stylish, large, and curved screen design.



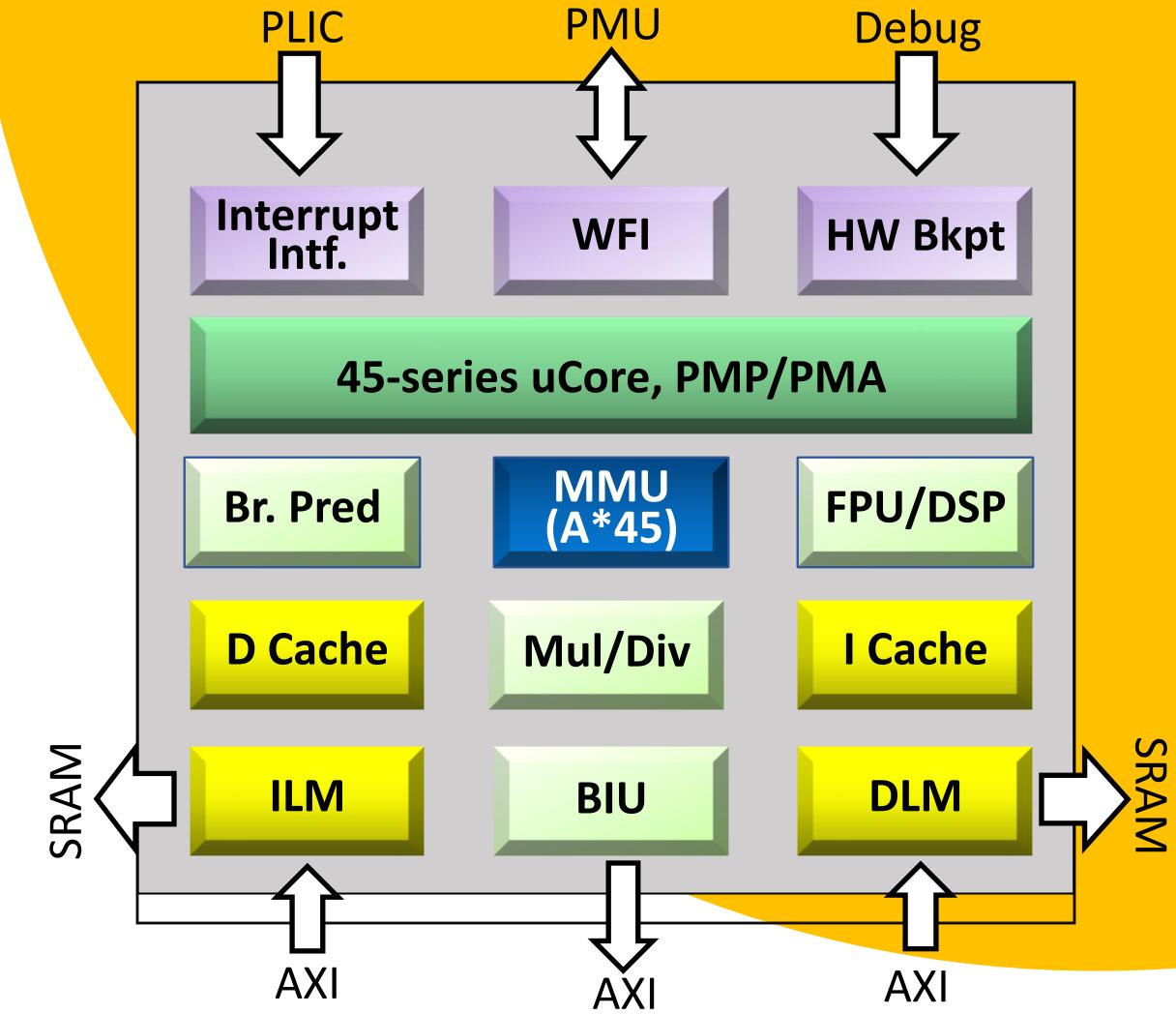
AndeCore™ 45-Series

32-bit AndesCore™ N45/D45/A45/A45MP

64-bit AndesCore™ NX45/AX45/AX45MP

AndesCore™ 45-Series Overview

- 8-stage In-Order Dual-Issue
- AndeStar™ V5 ISA:
 - RV*GCN (S/D FPU): All Series
 - RV*P-ext (DSP/SIMD): D45/A(X)45
 - MMU for Linux Applications: A(X)45
- MemBoost memory subsystem
- Low power dynamic branch prediction
- Unaligned data accesses
- Fast or small multiplier
- StackSafe™ (Andes Ext.)
- CoDense™ (Andes Ext.)
- Multi-core support: A(X)45MP
 - Up to 8 cores



AX45 Can Do More (vs. 64bit A-series)

Coremark/MHz



Dhrystone/MHz



■ A53

- 8-stage In-Order Dual Issue
- **Widely adopted by industries in many applications**

■ AX45

- 8-stage In-Order Dual Issue
- **Performance is better!**
 - Coremark/MHz: 1.35x
 - Dhrystone/MHz: 1.42x

Target Applications for 27 & 45-Series

- AI/Deep Learning
- AR/VR
- 5G



- Networking



- Storage



- Video Surveillance



- ADAS

- V2X (Vehicle to Everything)



- IVI (In-Vehicle-Infotainment)



Metaverse and more...

Bring Andes Strength to RISC-V Cores

Performance & Extensibility

- Leading PPA and code size
- Rich data processing in P, V, and ACE

Configurability

- Flexible configurations for rich features

Maturity

- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE



Concluding Remarks

<http://www.andestech.com>



A Trusted Computing Expert



Thank You

<http://www.andestech.com>

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