



Andes Technology Corp. Investor Conference Report



Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

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Company Overview

<http://www.andestech.com>



Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 260 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)
- EE Awards - “Taiwan-Product Award” & “Asia-Company Award” (2021)

Andes Mission

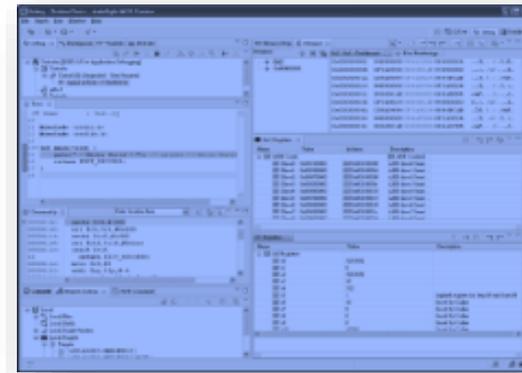
- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

Business Status Overview

- ❖ **250+** commercial licensees
 - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
 - **~600** license agreements signed
- ❖ AndeSight™ IDE:
 - **22,000+** installations
- ❖ Eco-system:
 - **500+** partners
- ❖ **10B+** Accumulative SoC Shipped



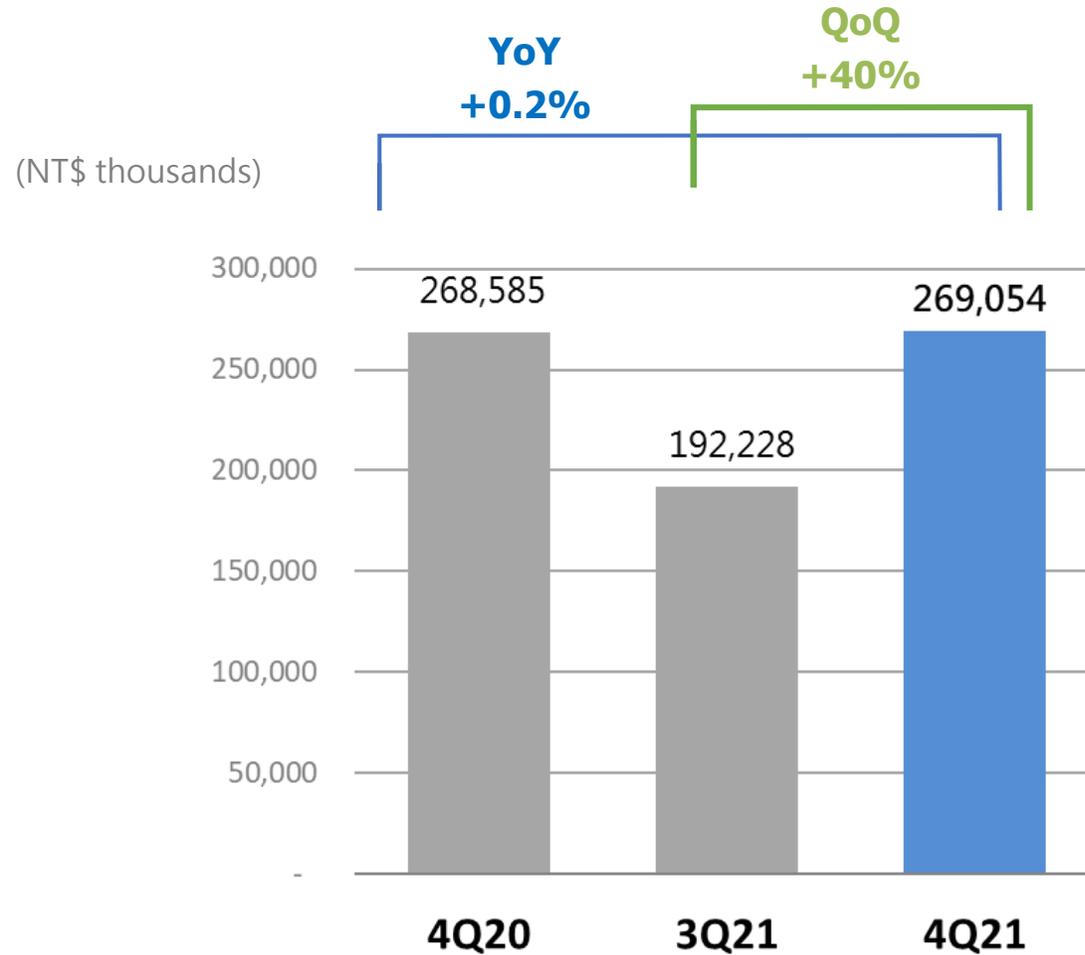


Operation Results

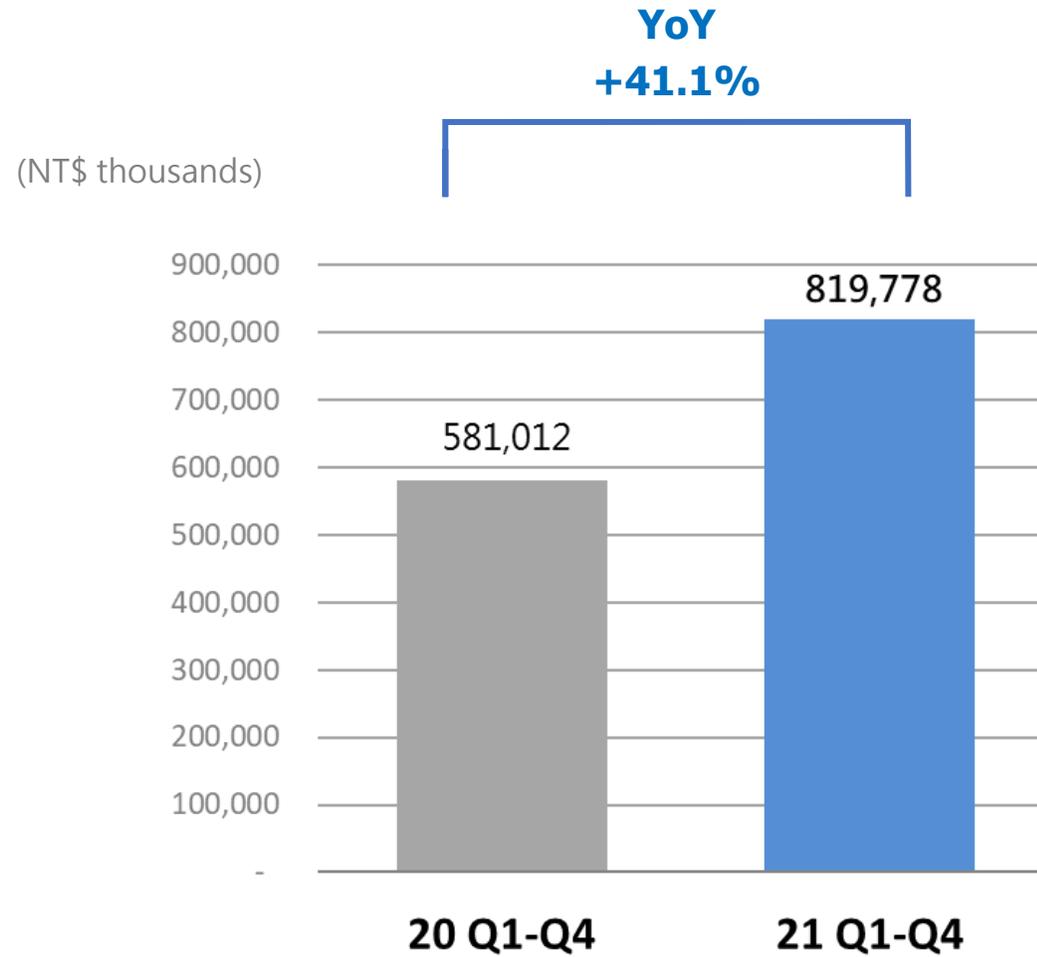
<http://www.andestech.com>



4Q21 Revenue Analysis



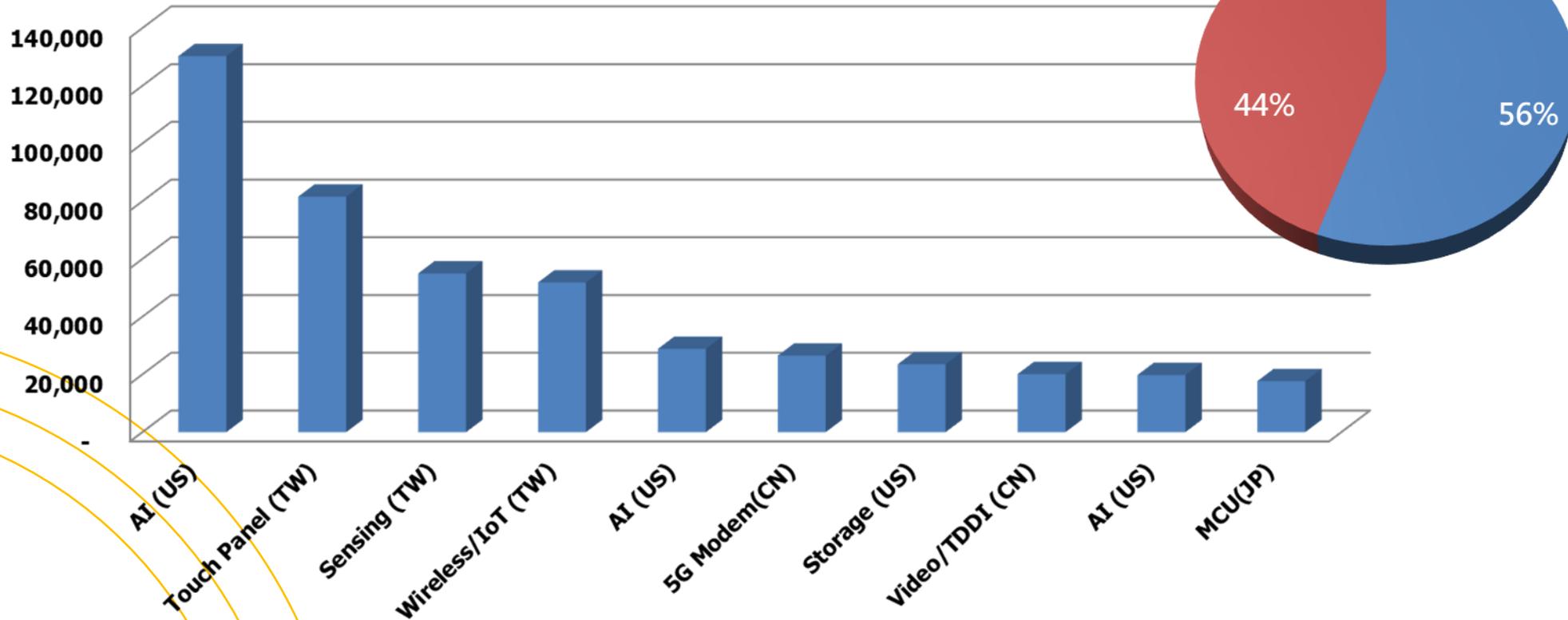
2021 Revenue Analysis



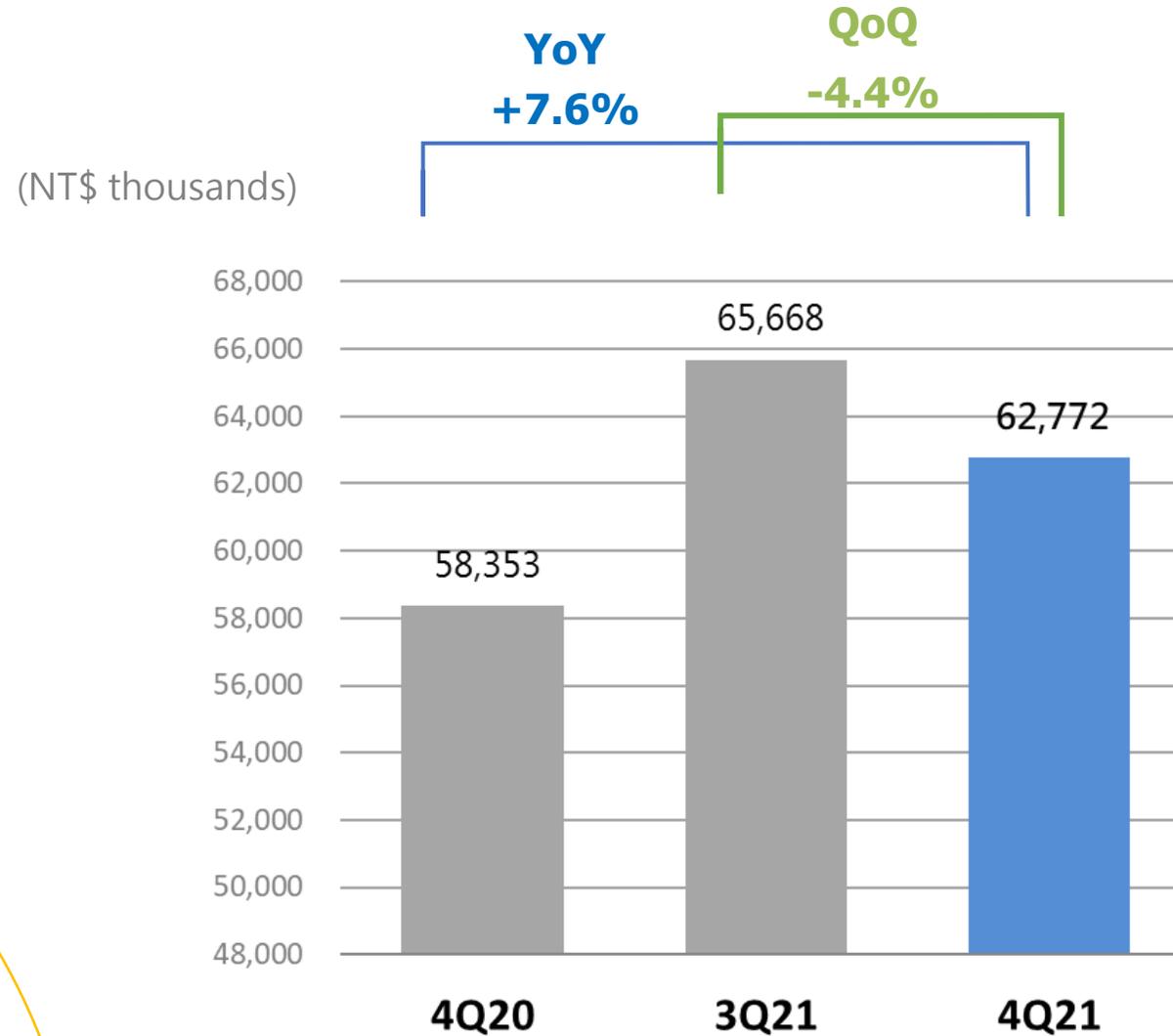
2021 Top 10 Customers Analysis by Revenue

(NT\$ thousands)

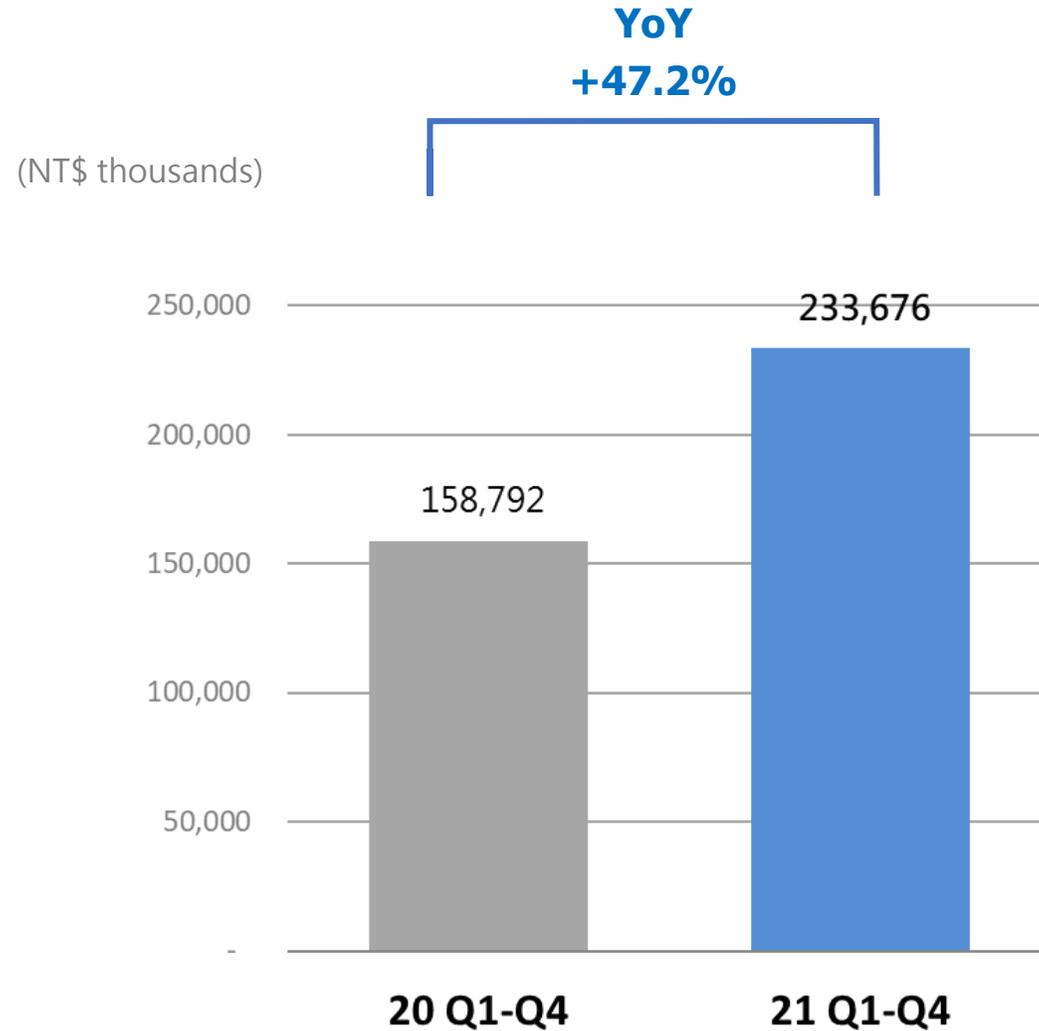
Top 10 Customer Contributed 56% Revenue



4Q21 Royalty Analysis



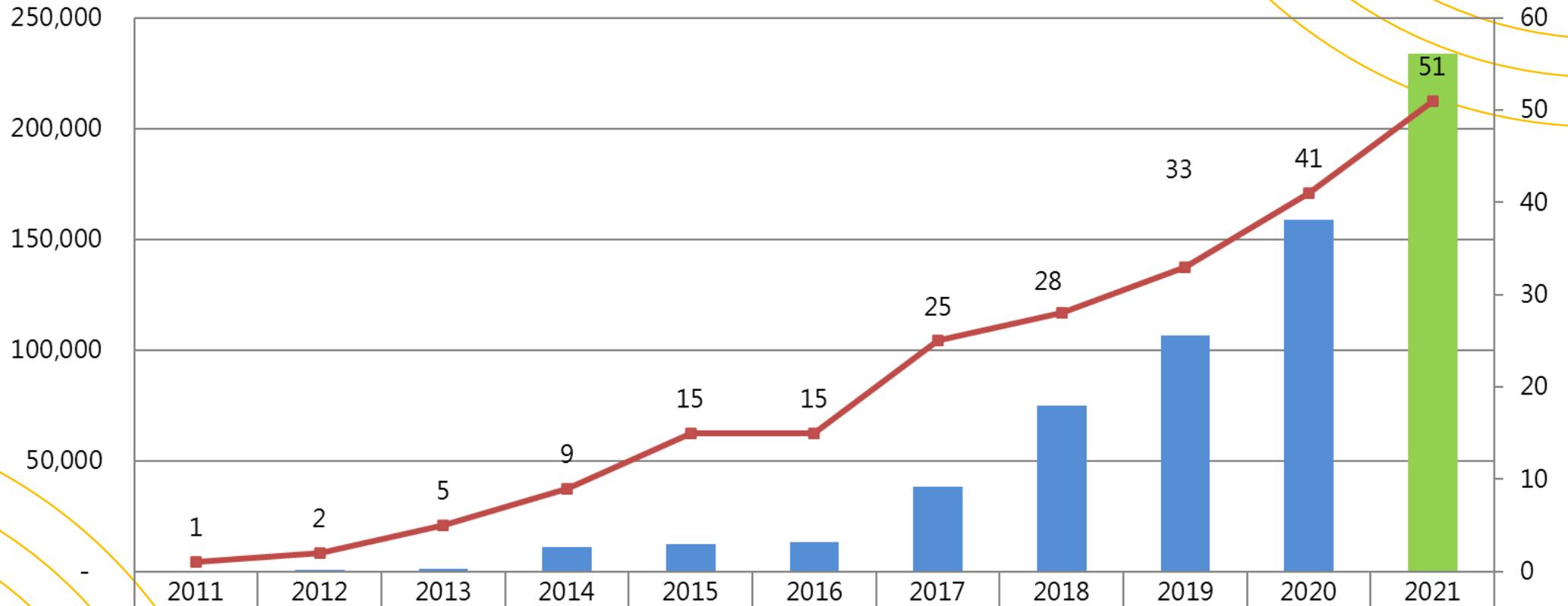
2021 Royalty Analysis



Royalty Analysis

(NT\$ thousands)

(Numbers)

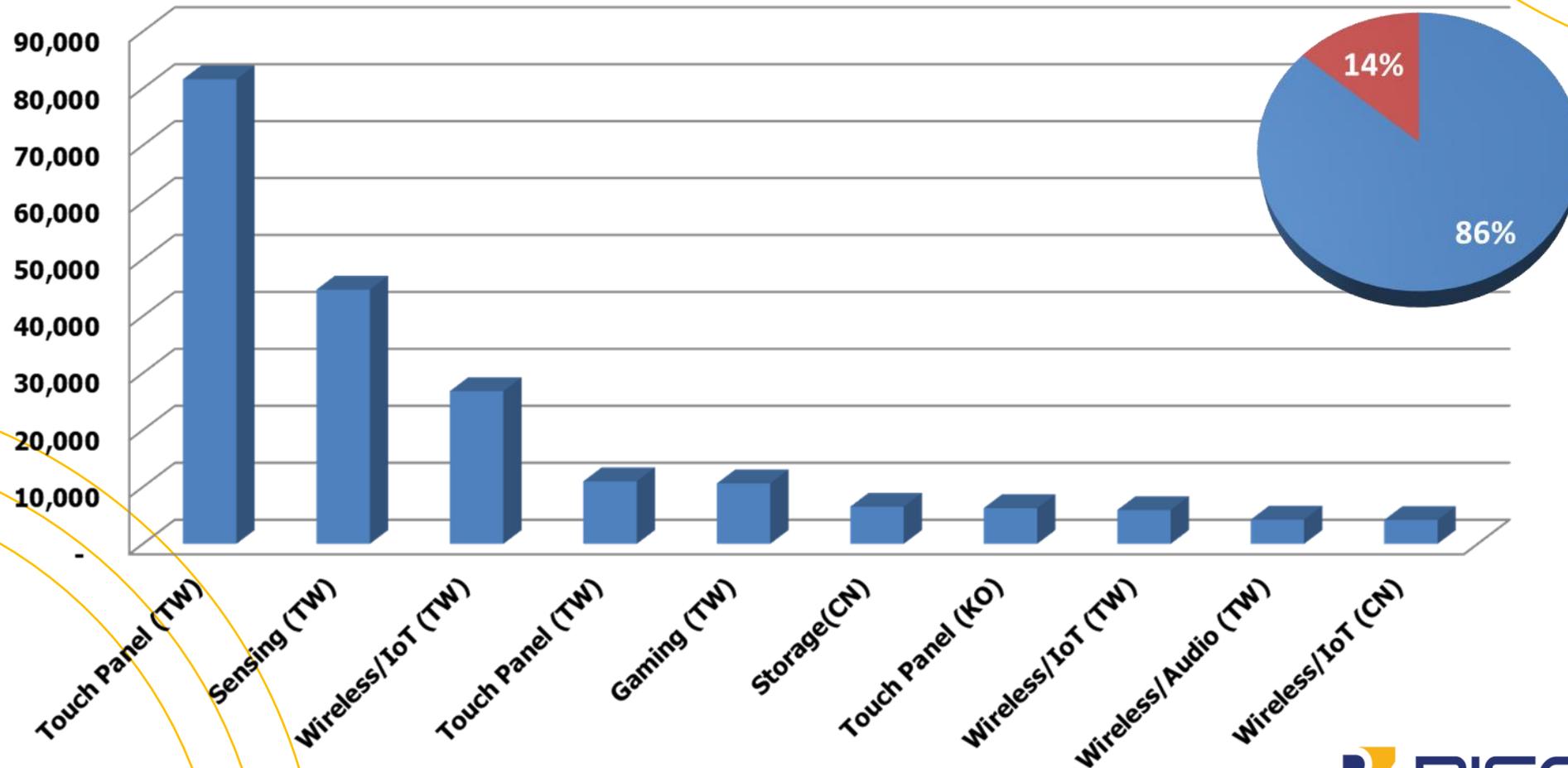


Royalty	445	660	1,285	10,819	12,232	13,320	38,287	74,953	106,716	158,792	233,676
Customer numbers	1	2	5	9	15	15	25	28	33	41	51

2021 Top 10 Customers Analysis by Royalty

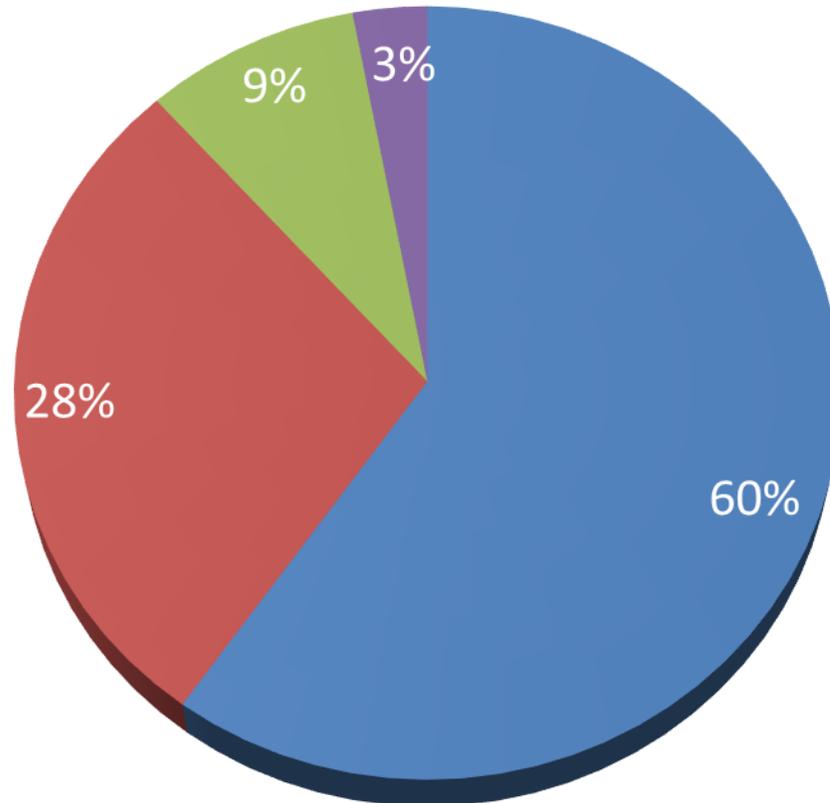
(NT\$ thousands)

Top 10 Royalty Customers
Contribution Analysis: 86%



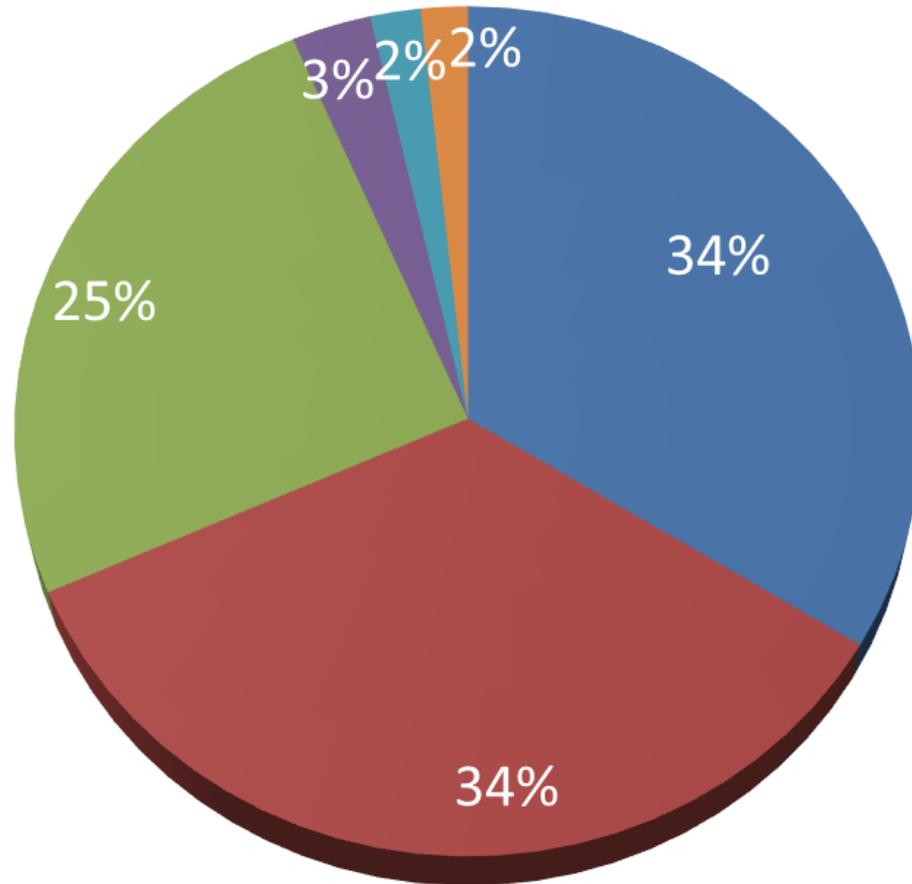
2021 Revenue Analysis by Payment Model

■ License Fee ■ Running Royalty ■ Maintenance & Others ■ Custom Computing Service



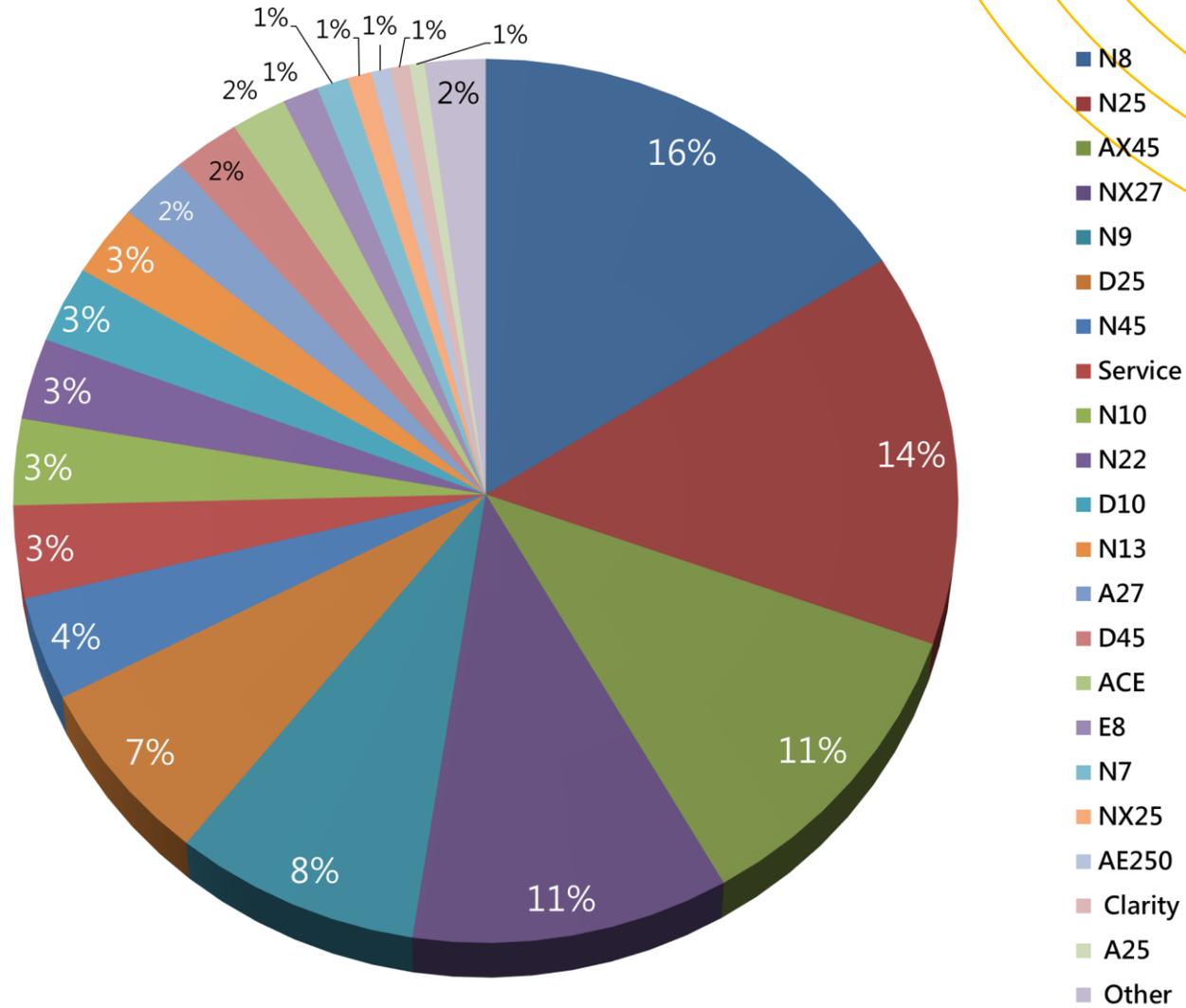
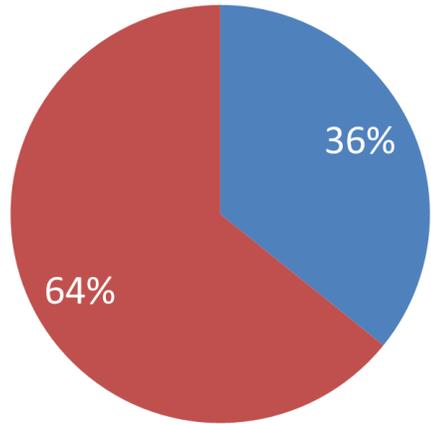
2021 Revenue Analysis by Region

■ Taiwan ■ China ■ USA ■ Japan ■ Europe ■ Korea



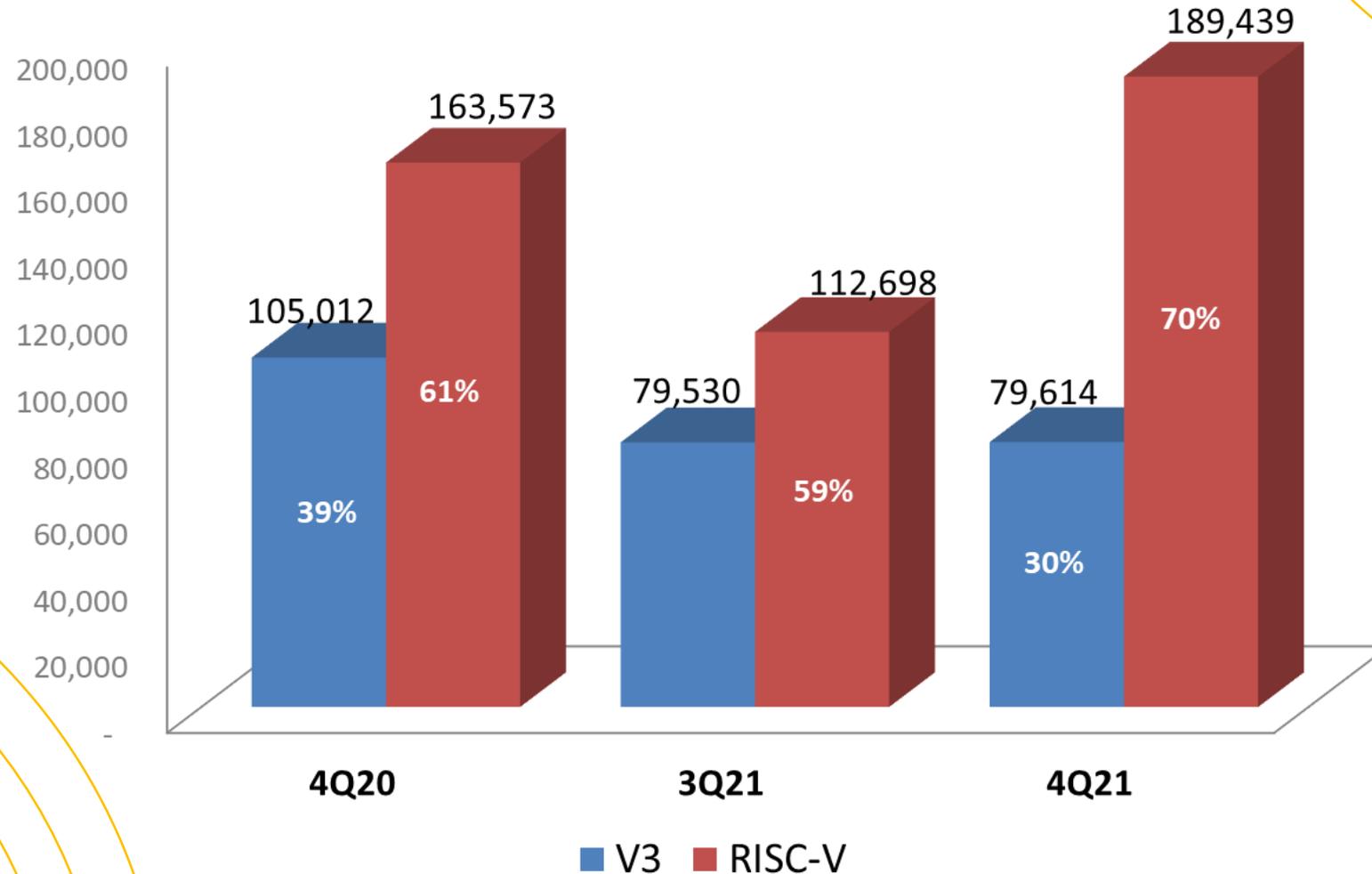
2021 Revenue Analysis by Product

V3 RISC-V



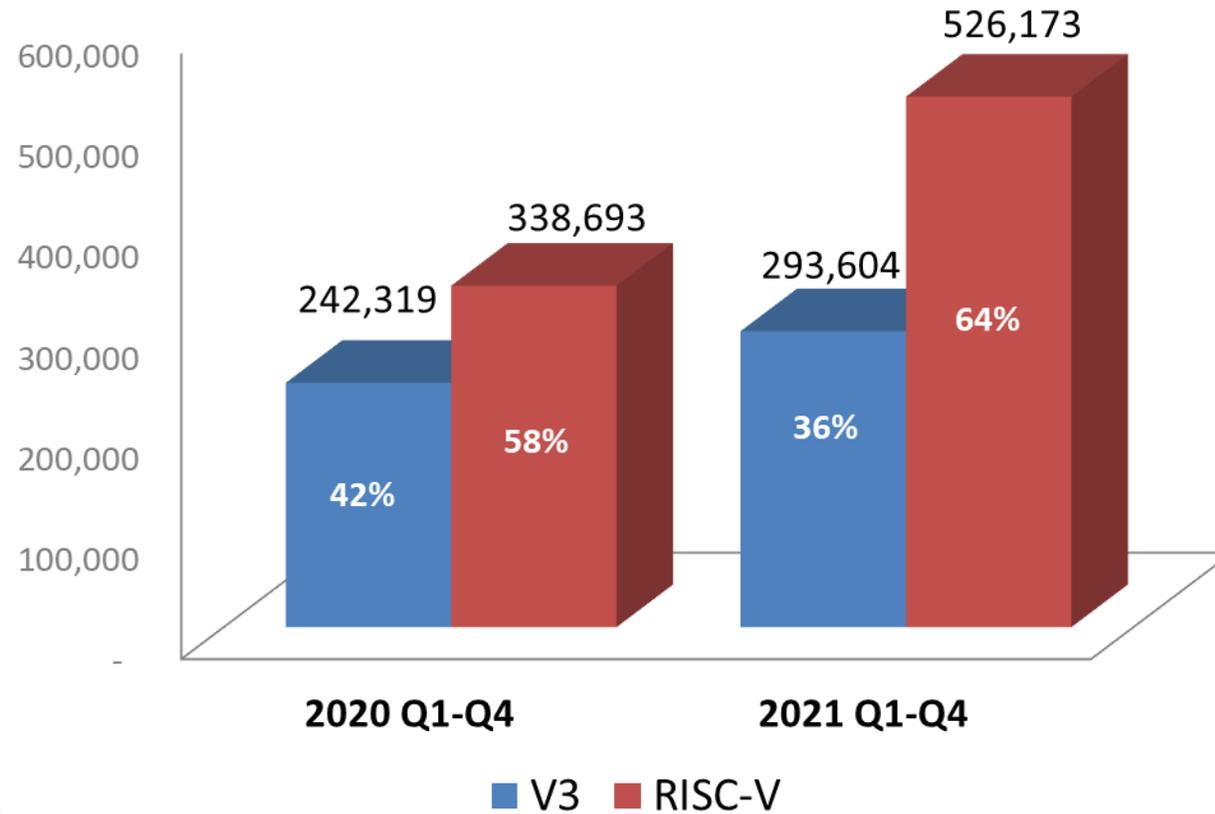
4Q21 Revenue Analysis - RISC-V

(NT\$ thousands)

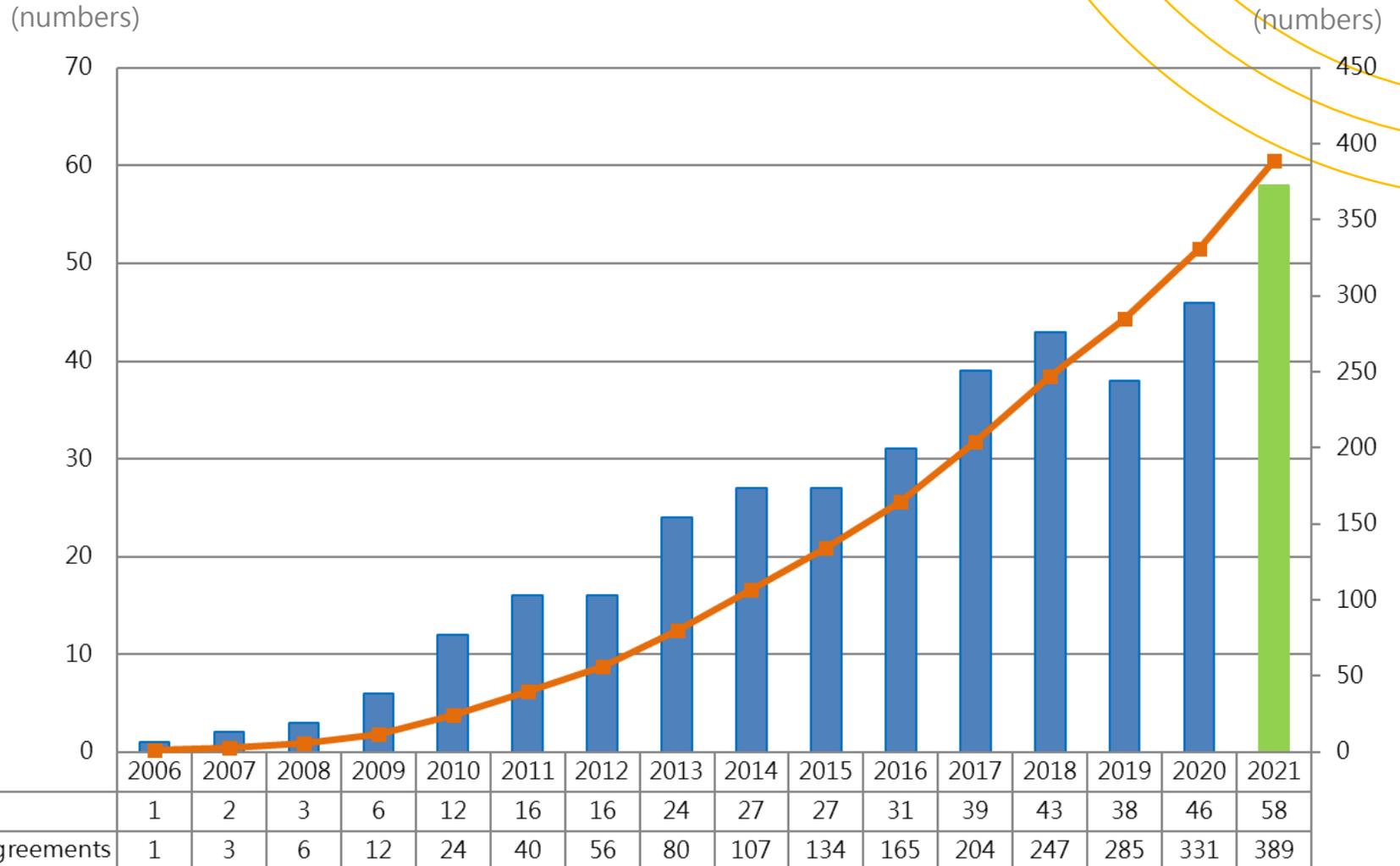


2021 Revenue Analysis - RISC-V

(NT\$ thousands)

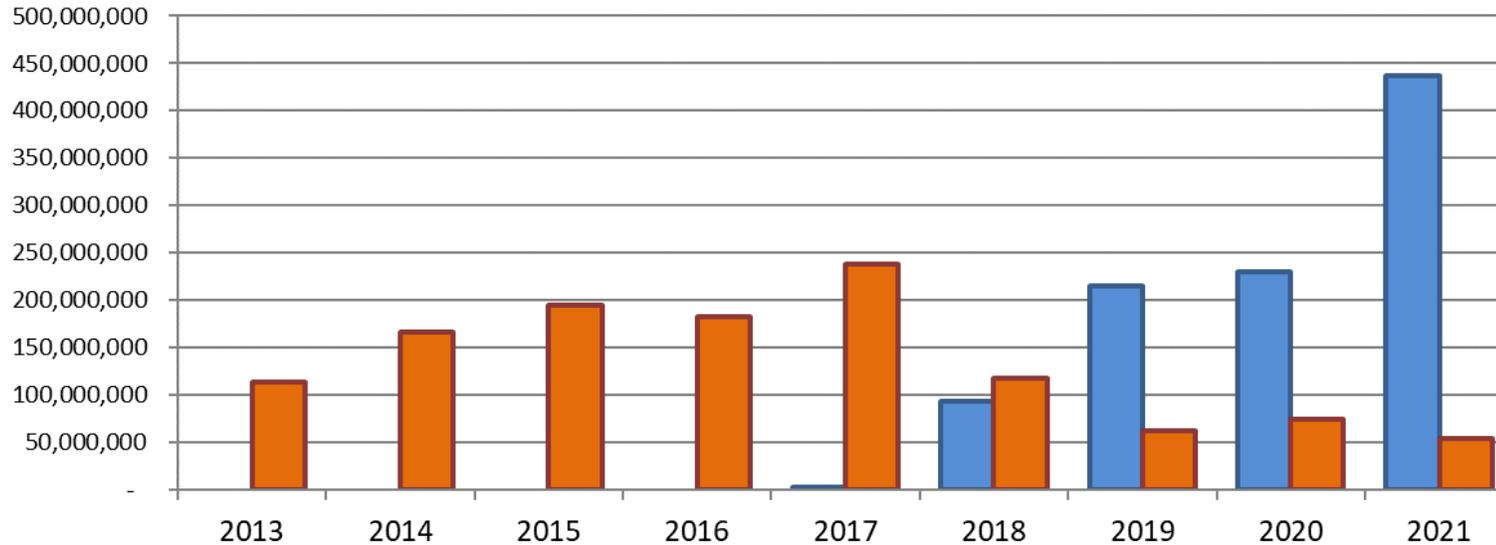


Historical Commercial Agreements

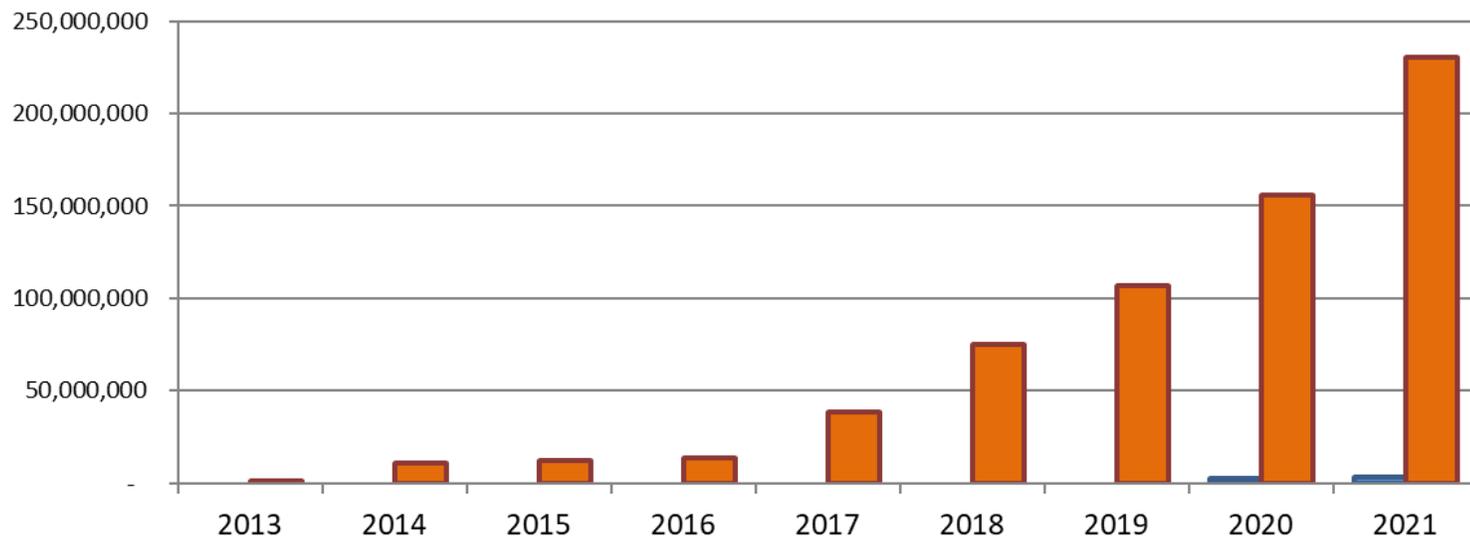


Historical Revenue Analysis

(NT\$)



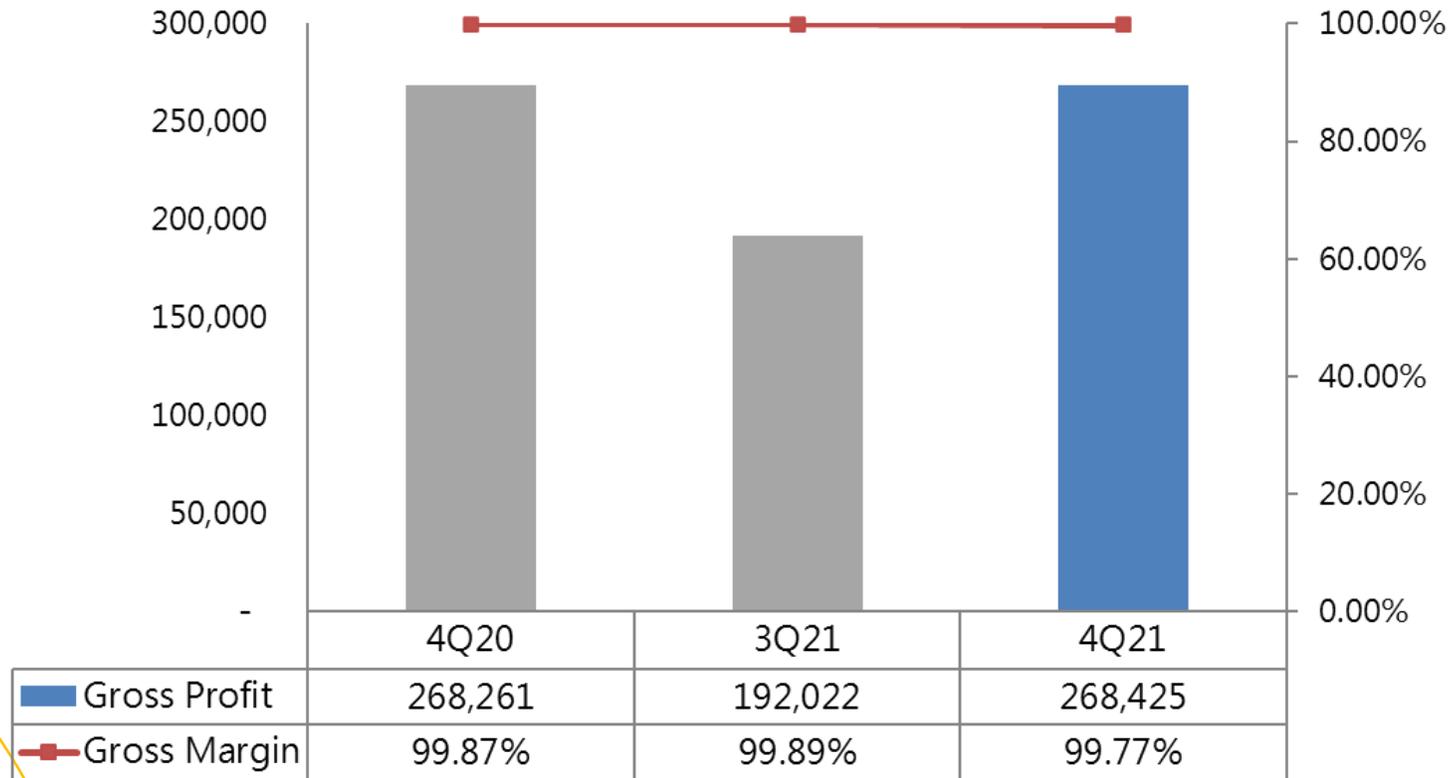
License



Royalty

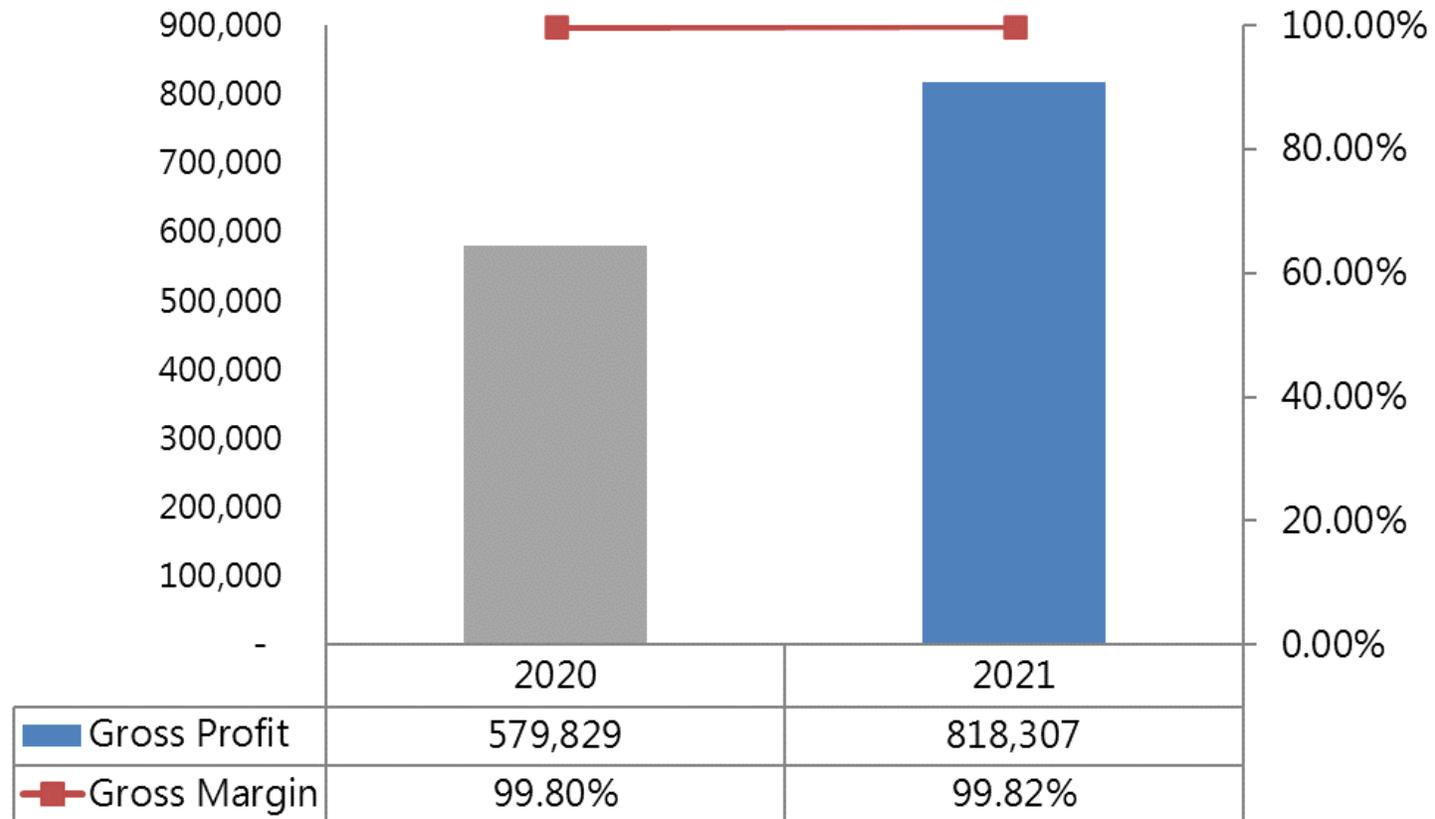
4Q21 Consolidated Gross Margin

(NT\$ thousands)

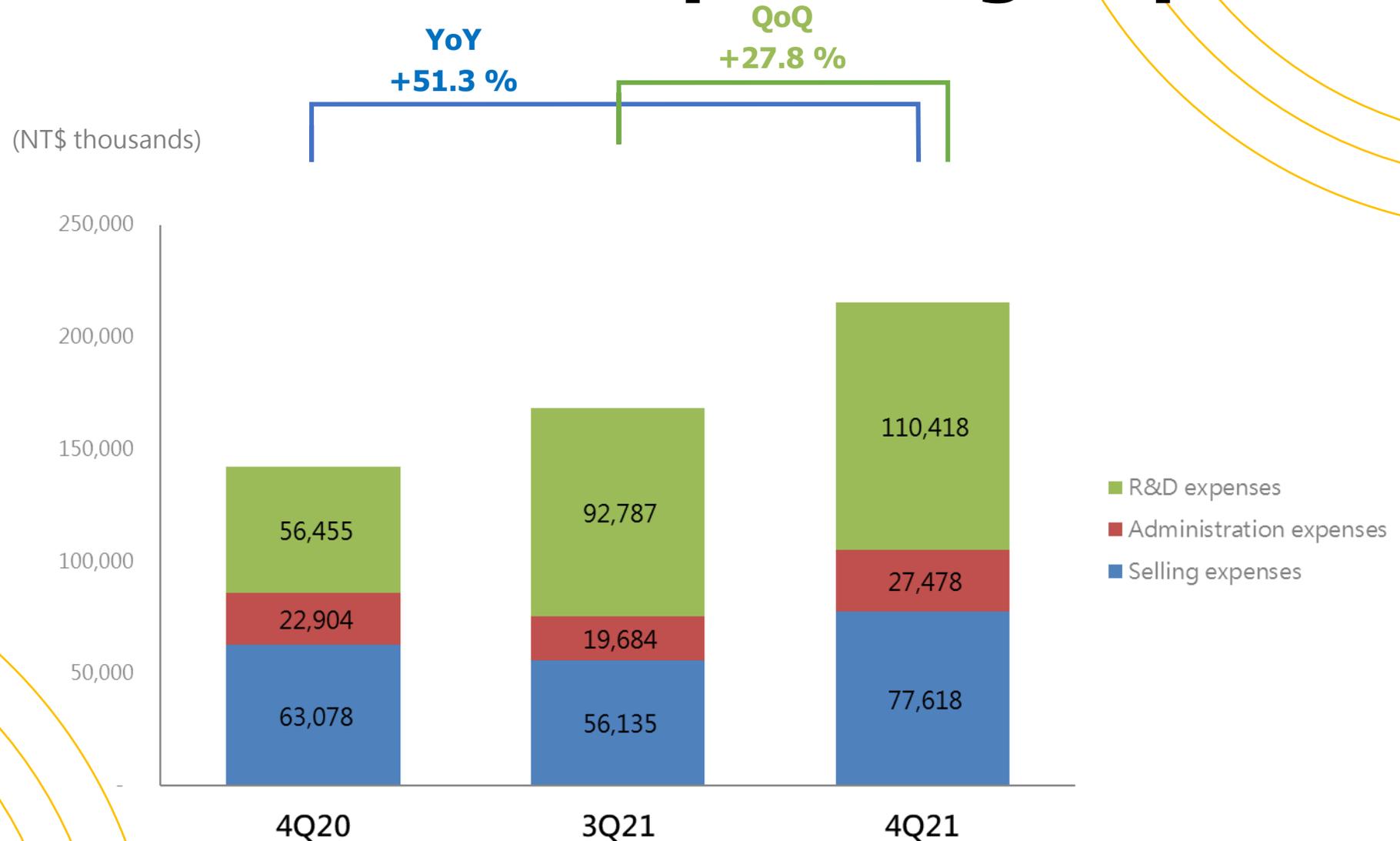


2021 Consolidated Gross Margin

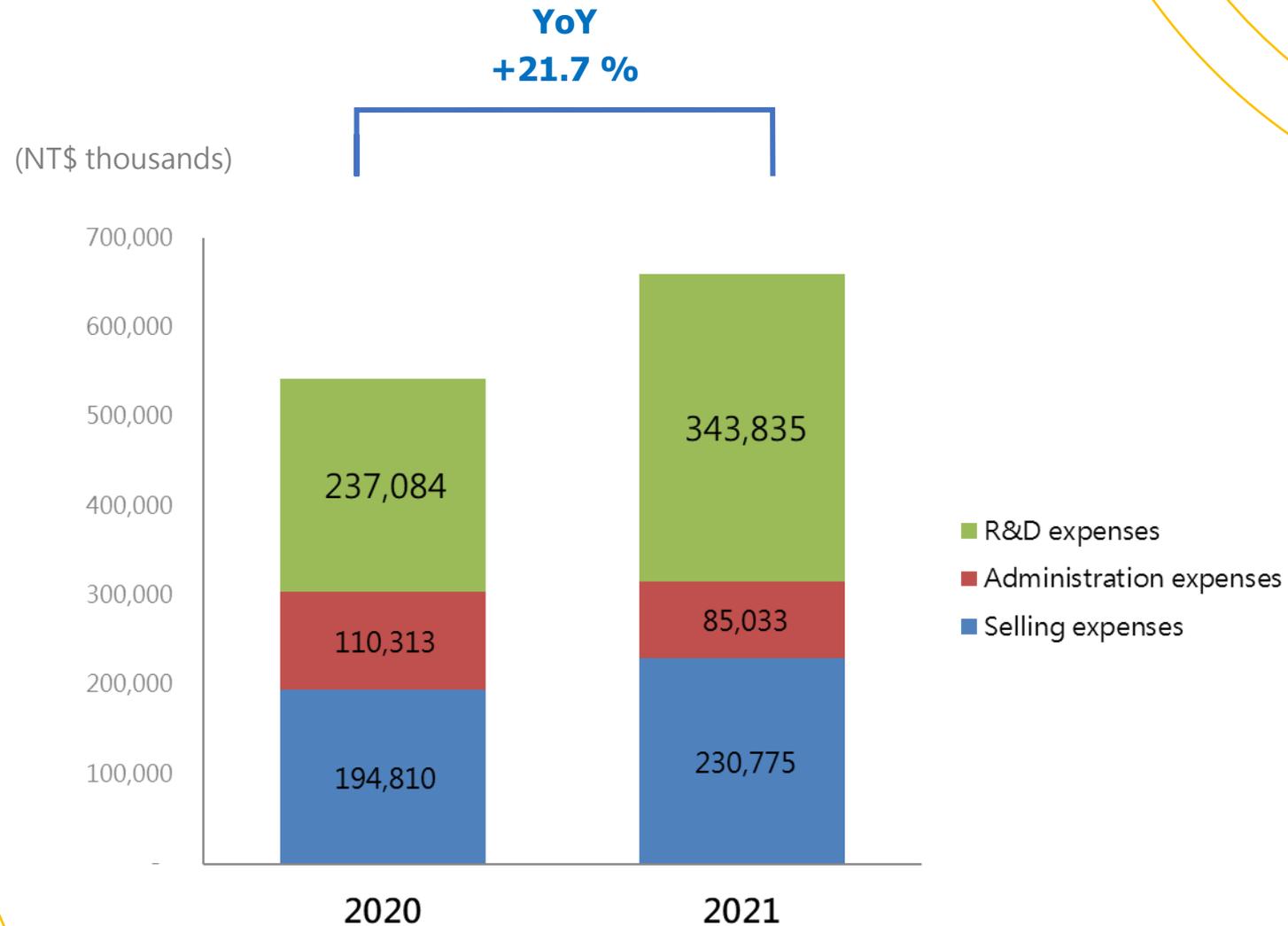
(NT\$ thousands)



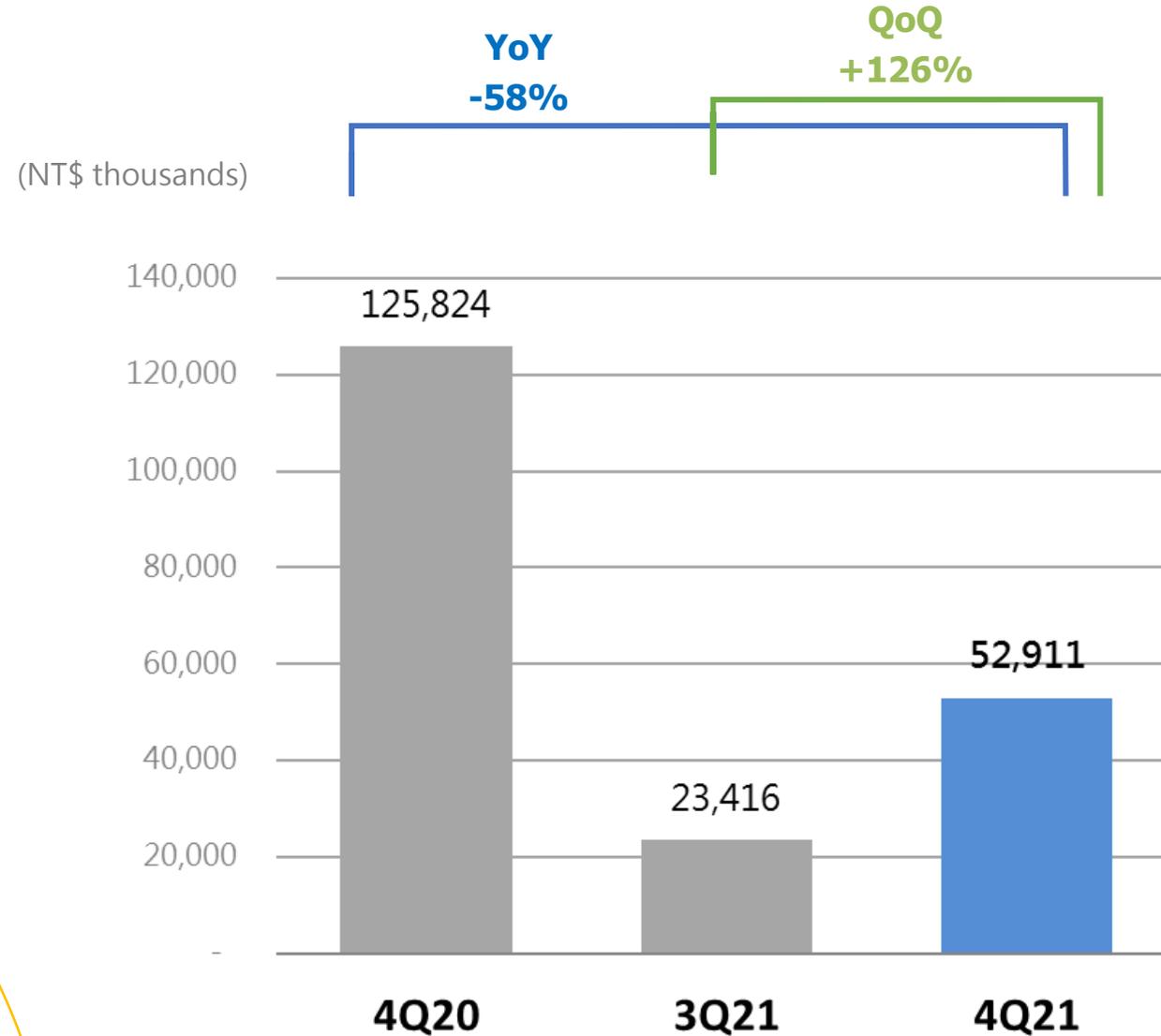
4Q21 Consolidated Operating Expenses



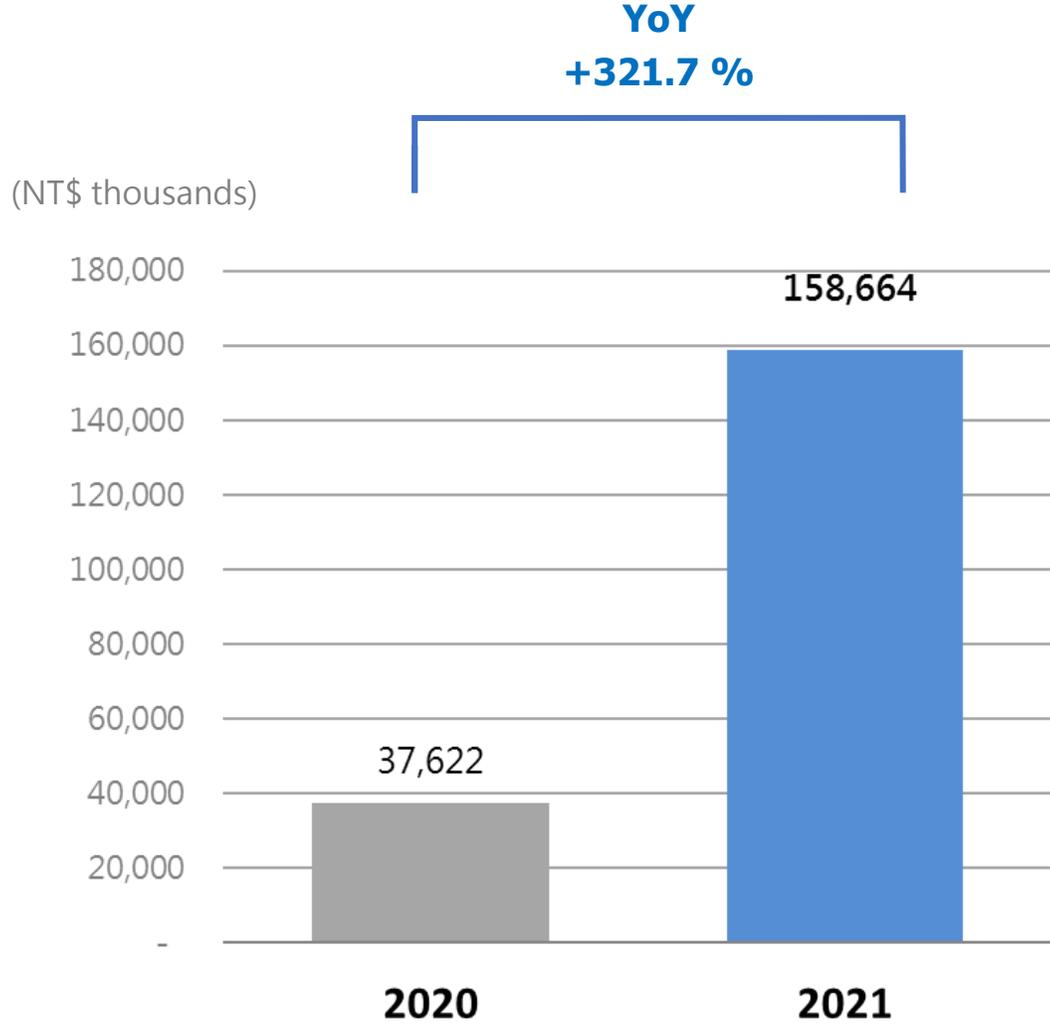
2021 Consolidated Operating Expenses



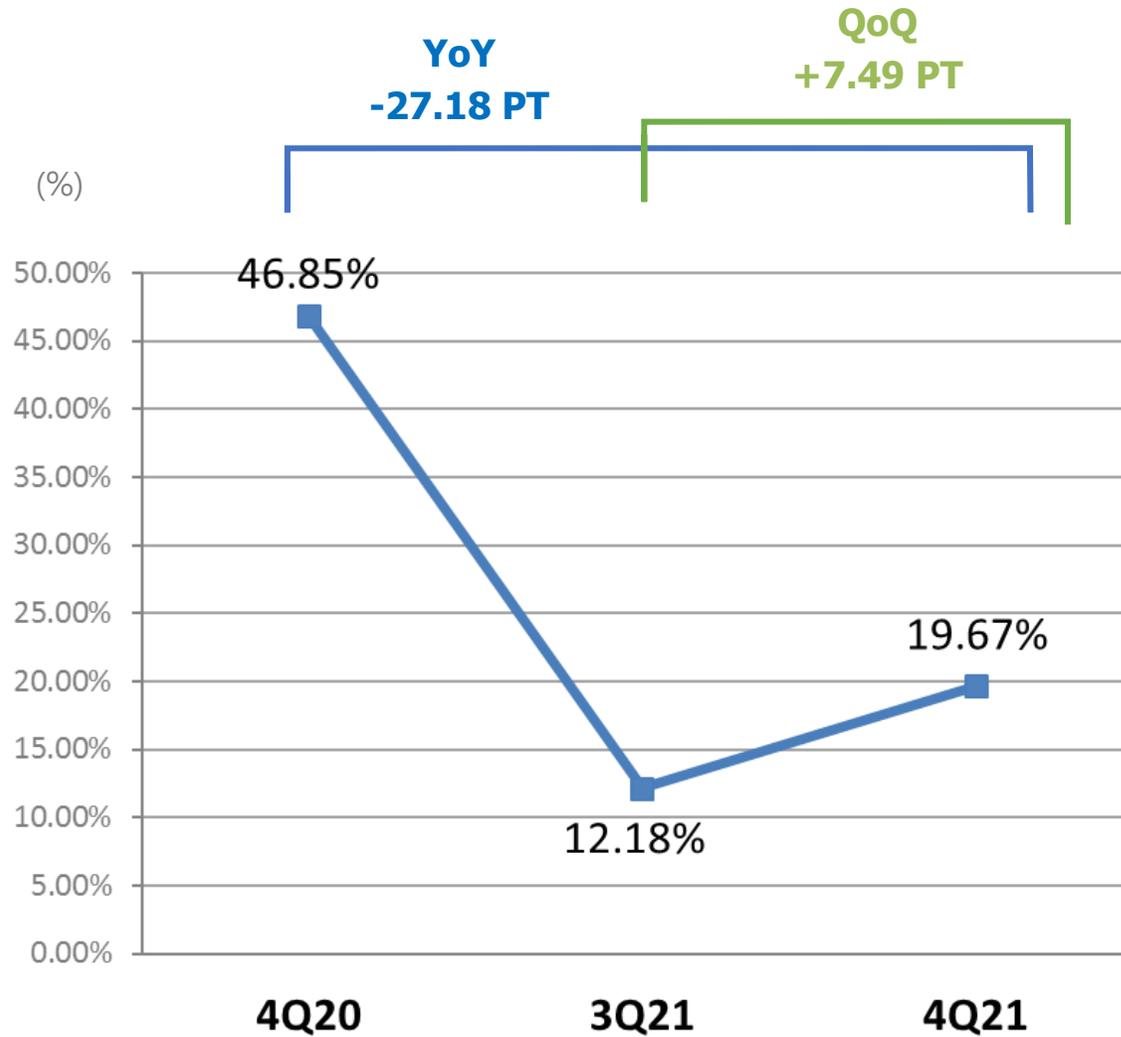
4Q21 Consolidated Operating Income



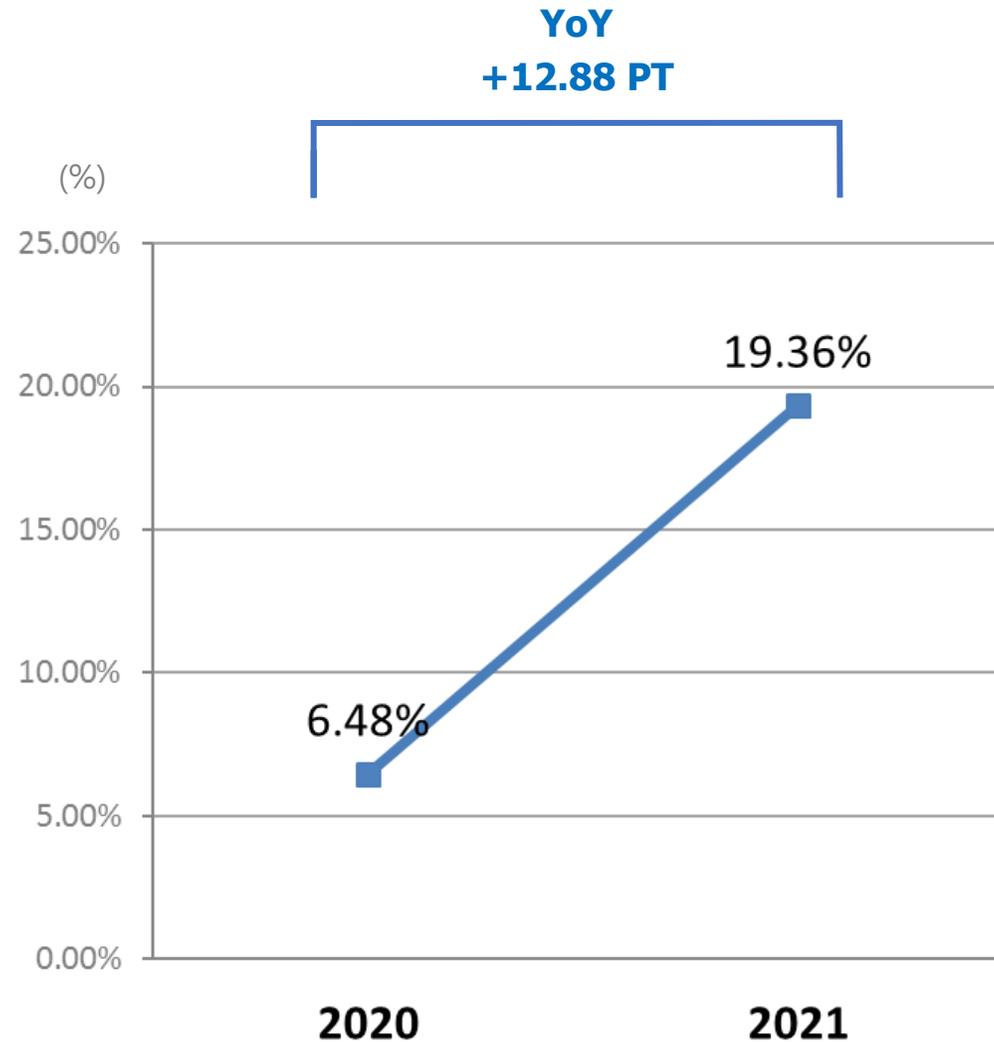
2021 Consolidated Operating Income



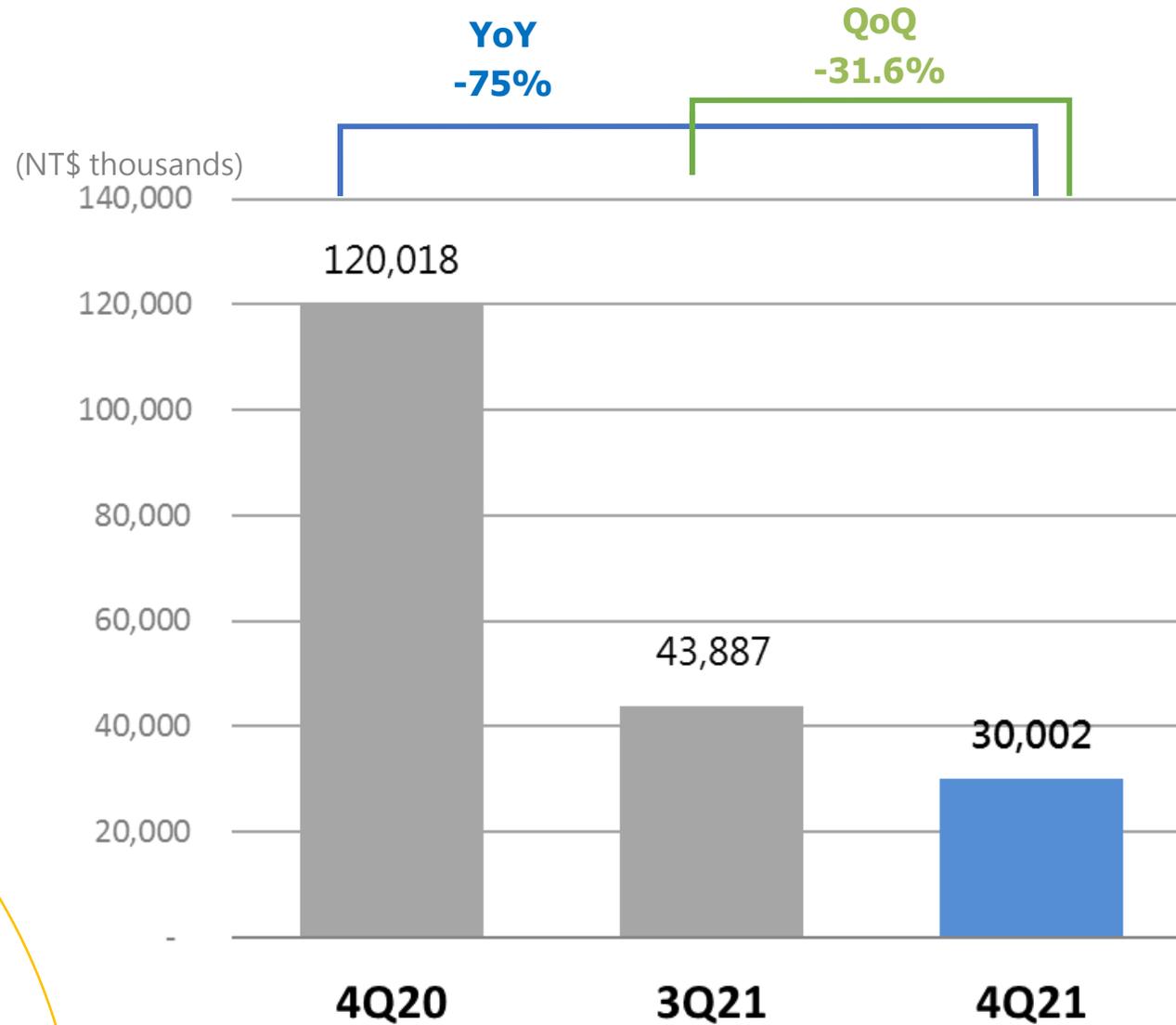
4Q21 Consolidated Operating Margin



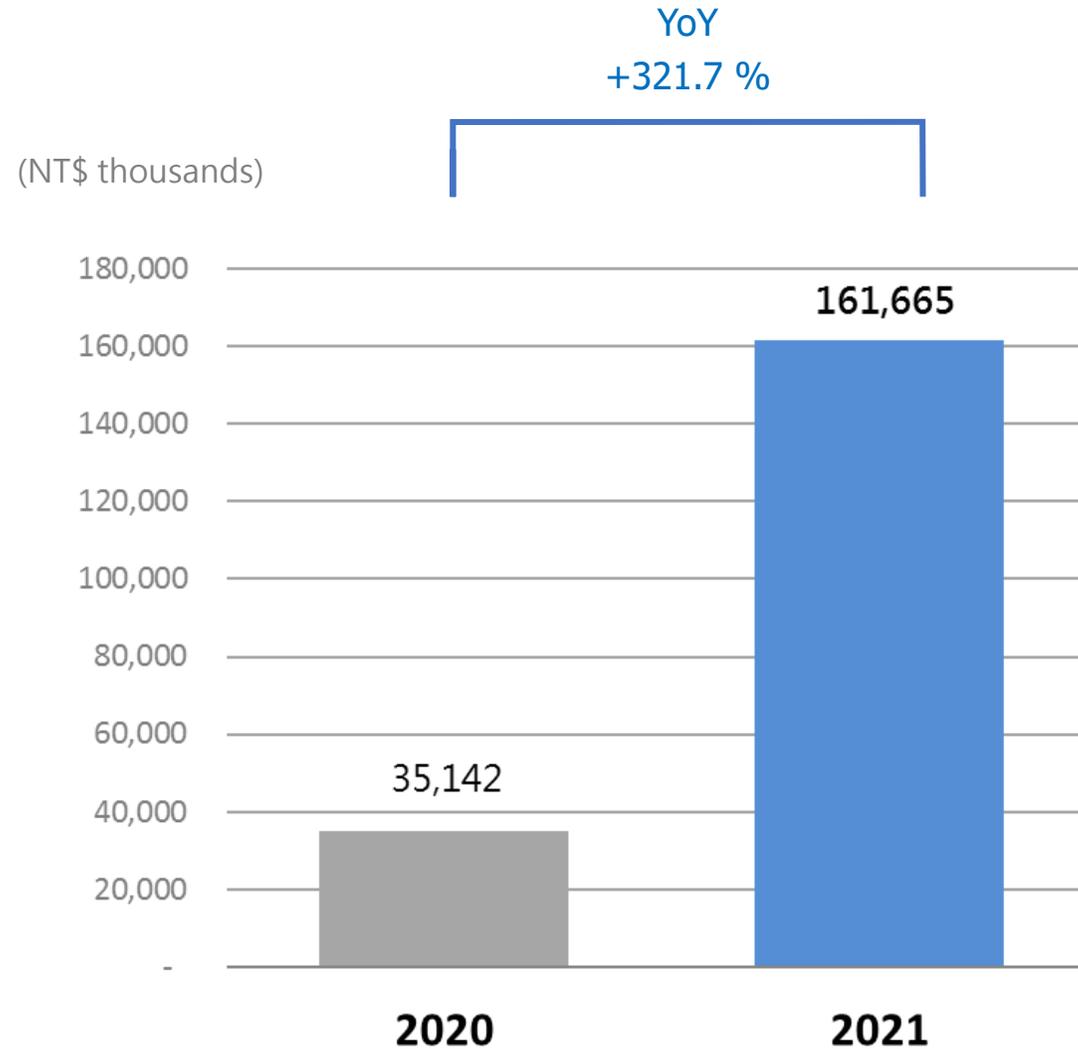
2021 Consolidated Operating Margin



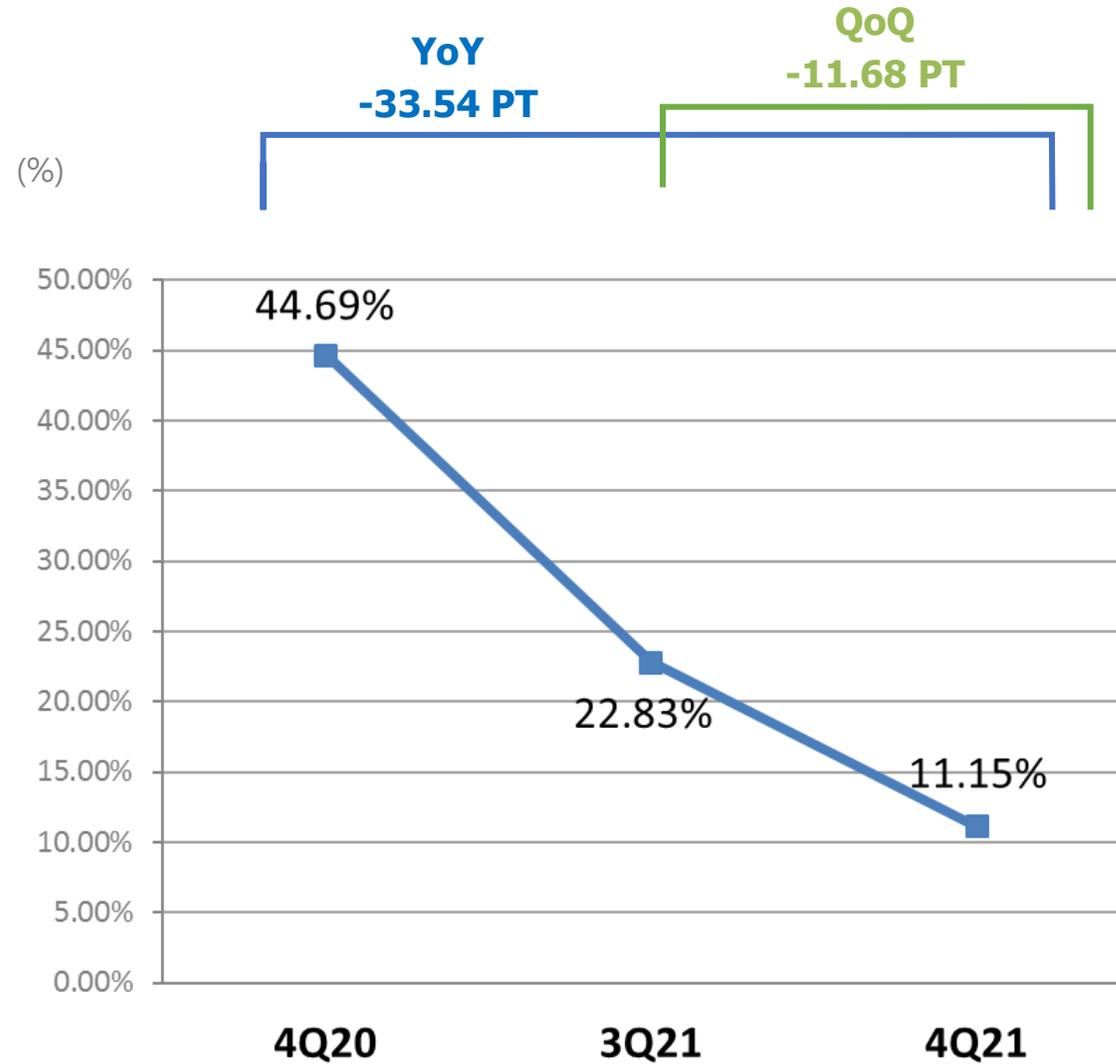
4Q21 Consolidated Net Income



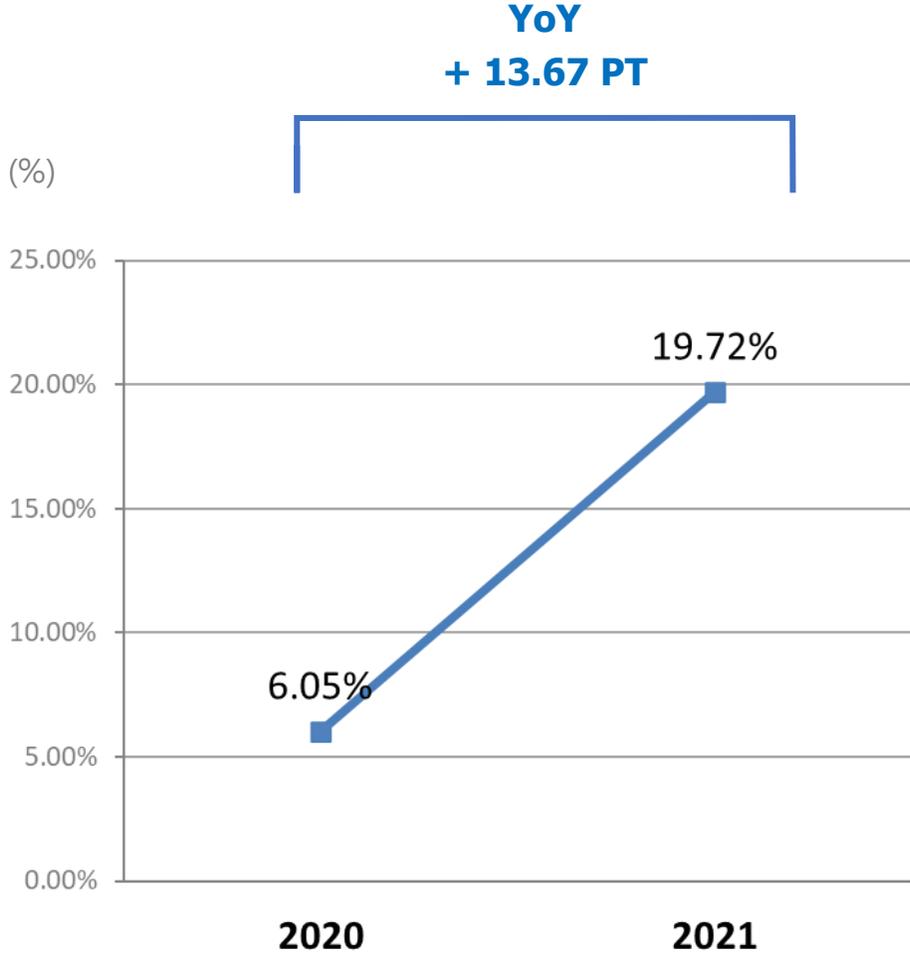
2021 Consolidated Net Income



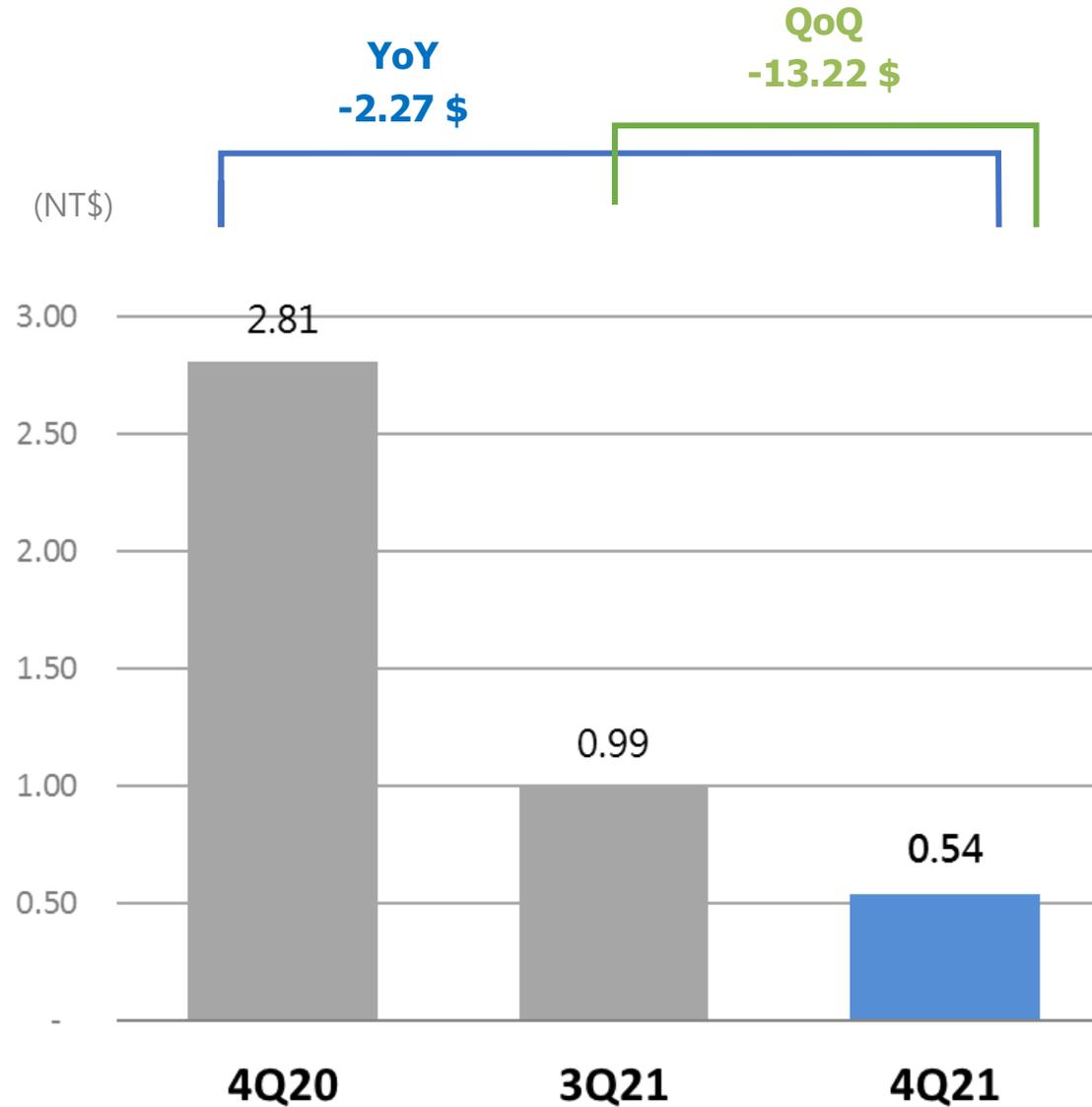
4Q21 Consolidated Net Profit Margin



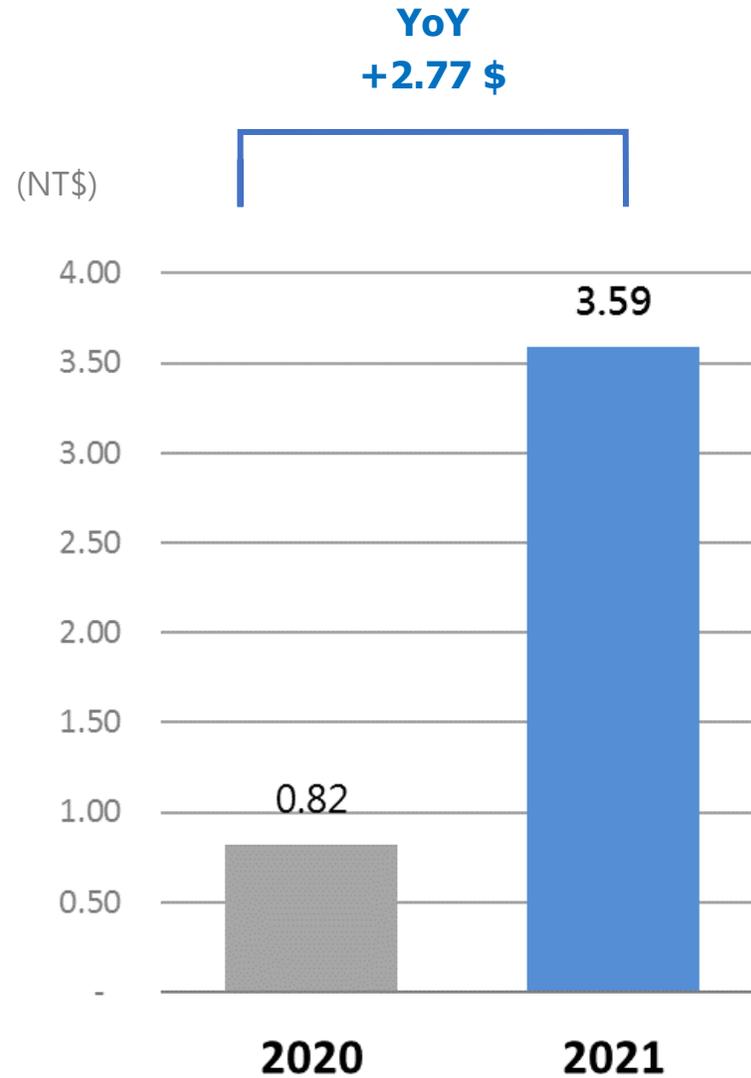
2021 Consolidated Net Profit Margin



4Q21 Consolidated EPS



2021 Consolidated EPS





Product Applications

<http://www.andestech.com>



Andes Updates

- ❖ A 17-year-old public CPU IP company
- ❖ 3B+ Andes-Embedded SoC annually in 2021



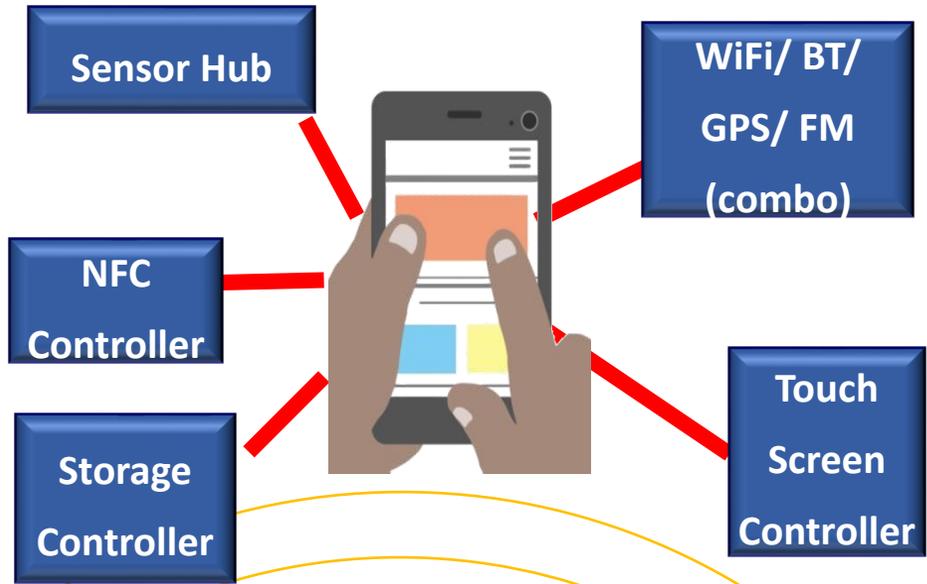
- ❖ A founding premier member of the RISC-V International
- ❖ An active role in RISC-V International & its extension task groups
 - RISC-V Board Director
 - Member of Technical Steering Committee
 - RISC-V Ambassador
 - Chair of P-extension (Packed DSP/SIMD) Task Group
 - Co-chair of Fast Interrupt Task Group
 - Vice Chair of TEE Task Group
- ❖ A major open source maintainer/contributor

The first slide is titled "GNU-Based Toolchains" and lists: binutils, GCC: May, 2017; glibc: February, 2018 (only supports rv64-based ISAs); newlib: August, 2017; and "Probably not a compiler bug". It features logos for SiFive, bluespec, and redhat, and the Andes Technology logo.

The second slide is titled "RISC-V LLVM Porting Effort" and lists: Alex Bradbury is in charge of RISC-V LLVM (Talk yesterday afternoon, Poster on Tuesday night); RV32IM(A)FD support upstream (Missing hard-float-calling convention, Missing 64-bit support, Missing compressed support); and Clang, Go, and OpenJDK have run code (First port in progress, Poster on Tuesday). It features logos for Andes Technology, lowRISC, and Berkeley.

The third slide is titled "RISC-V Linux Kernel Port" and lists: Linux: January, 2018 (Only RV64-based systems, Drivers are trickling in now). It features logos for Berkeley, SiFive, and Andes Technology, and includes a photo of a group of people at a conference.

Andes Embedded in Various Applications



Andes Embedded in Smart Phones



Smart Speakers:
WiFi IoT



Bike Sharing:
GPS Ctrl



X-Trail:
ADAS Ctrl



Switch:
Game Flash Ctrl



- ❖ In leading **machine learning computers** for datacenter
- ❖ In tier-one **switch routers** for datacenter
- ❖ Recent applications: **5G networking, WiFi 6/7, AI processors** (using Andes Custom Extension, ACE)

V5 Adoptions: From MCU to Datacenters

❖ Edge to Cloud

- ADAS
- AIoT
- Blockchain
- FPGA
- MCU
- Multimedia
- Security
- Wireless (BT/WiFi)
- Datacenter AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

❖ 40nm to 5nm

❖ Many in AI





New Products and Ecosystems

<http://www.andestech.com> 

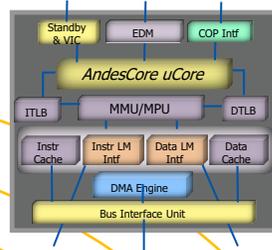
Andes RISC-V Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

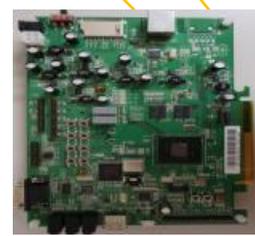
```
movw.adio $r1, [0], 0x00000000
movw.adio $r2, [0], 0x00000002
addi $r3, $r2, -8
swsh $r3, 0x5000
lwsh $r1, [0x1+0x0000]
movss $r2, $r0
movss $r0, $r1
lw $r1, [0x1+0x0000]
addi $r3, $r2, 12
```

AndesCore™
Processors



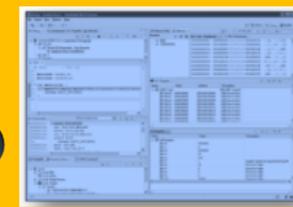
Highly optimized design with leading PPA

Handy peripheral IPs to speed up SoC construction



AndeShape™ Platforms

AndeSight™
Tools



Professional IDE with high code quality

AndeSoft™ Stacks



Extensive SW stacks from bare metal, RTOS to Linux

Andes V5 Architecture for All Levels of Computing

AndeStar™ V5 CPUs

RISC-V®



RV32/64

Andes Extension

Conventional Computing Architecture

Domain Specific Architecture (DSA)

N/D-series

N22 N(X)25 D25...

Leading PPA Embedded Processor

IoT, Sensing, Storage, Audio, GPS



Define custom instruction to handle time critical codes

A-series

A(X)25 A(X)27 A(X)45
Multicore...

High Performance and Power Efficient AP

5G, AI, Datacenter, Video Surveillance, Networking

Andes Custom Extension

Better approach for accelerator /co-processor to do particular jobs

Vector

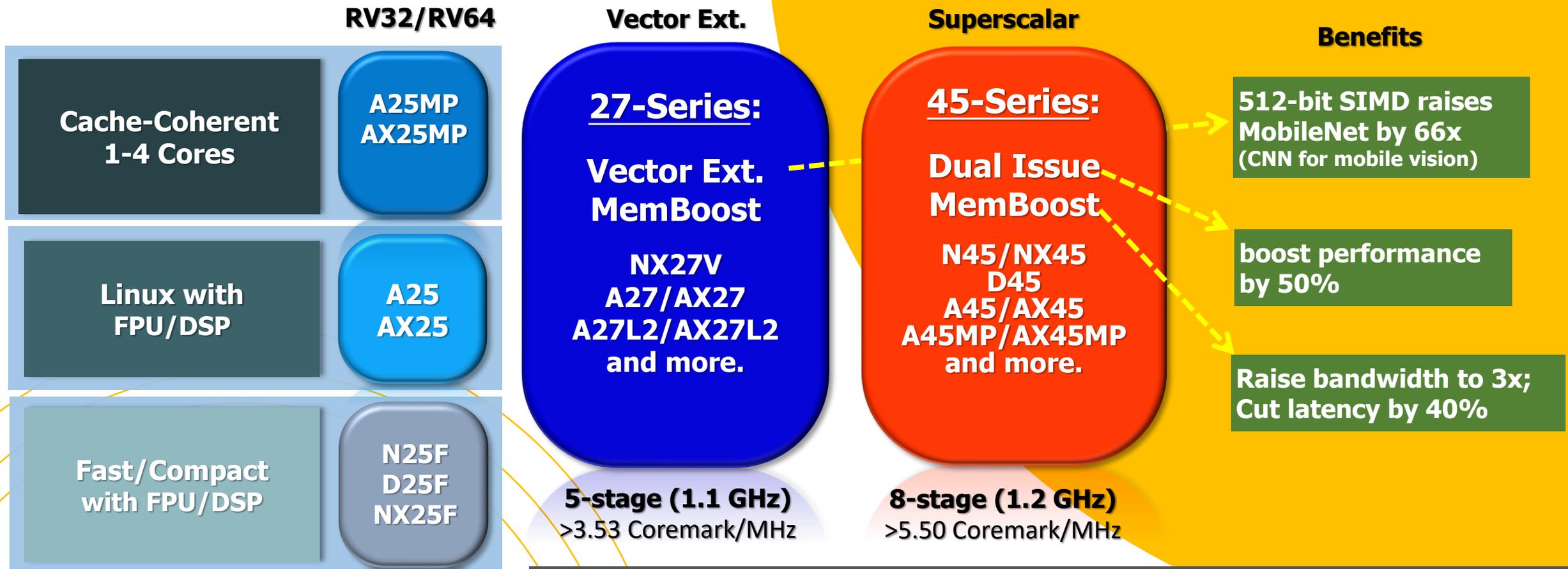
NX27V NX45V...

Cray Style, Scalable Vector Processor

Datacenter, Server, Deep Learning

Automation Tool for the generation of toolchain, ISS, partial RTL and verification

Andes RISC-V Product Roadmap



N22
2-stage
(700 MHz)

5-stage (1.1 GHz)
>3.53 Coremark/MHz

Leading positions:

- ❖ The first company offering commercial RVP DSP CPU
- ❖ The first company offering the most updated spec of commercial RVV Vector processor
- ❖ Tools for RISC-V custom extension expansion: ACE

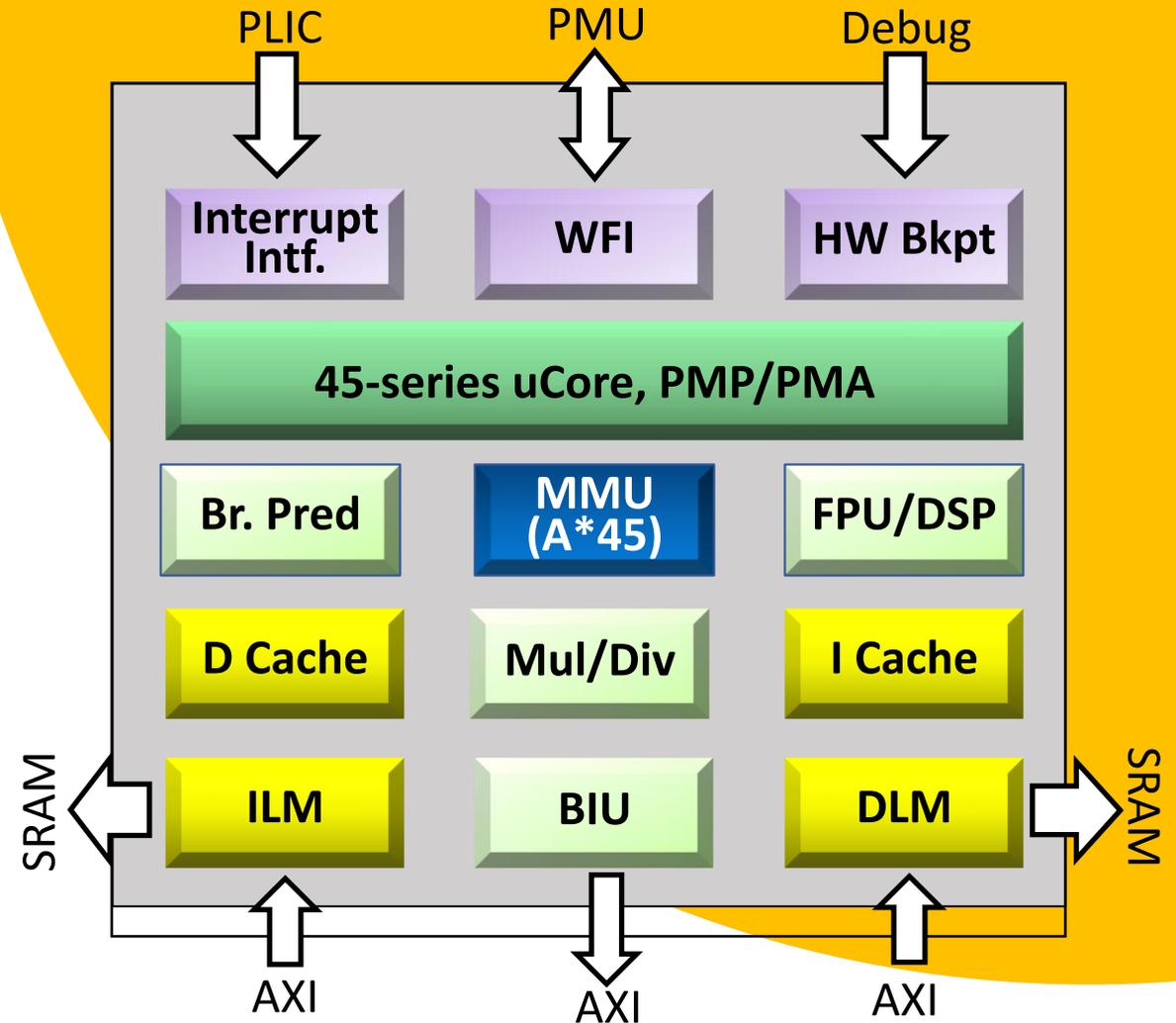
AndeCore™ 45-Series

32-bit AndesCore™ N45/D45/A45/A45MP

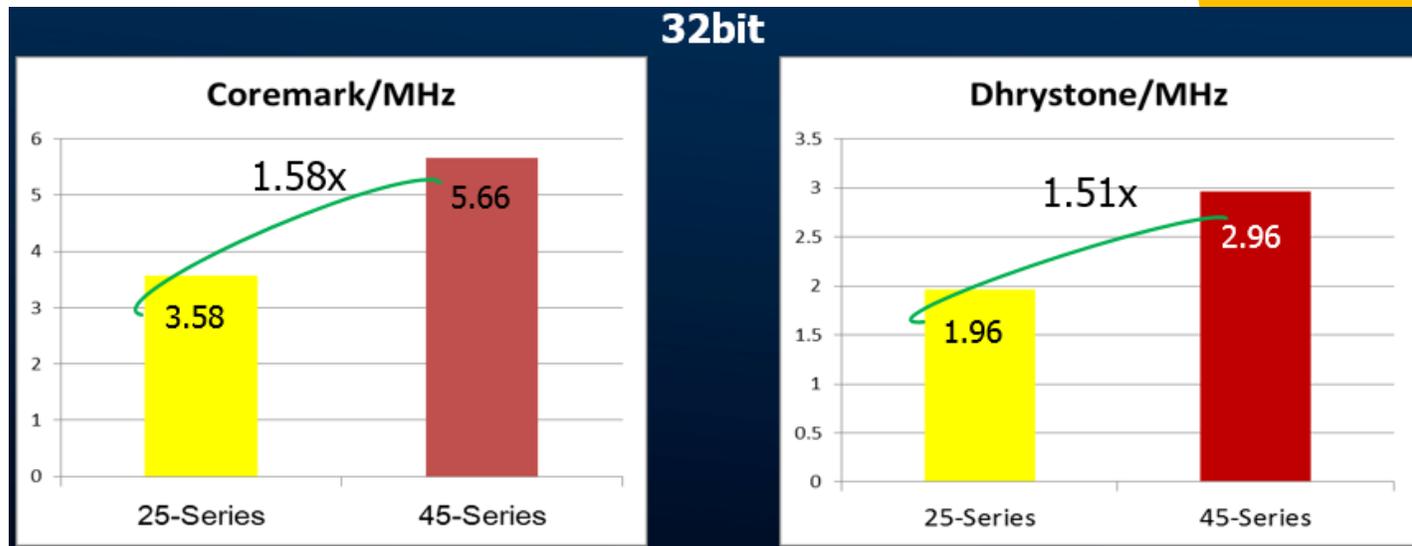
64-bit AndesCore™ NX45/AX45/AX45MP

AndesCore™ 45-Series Overview

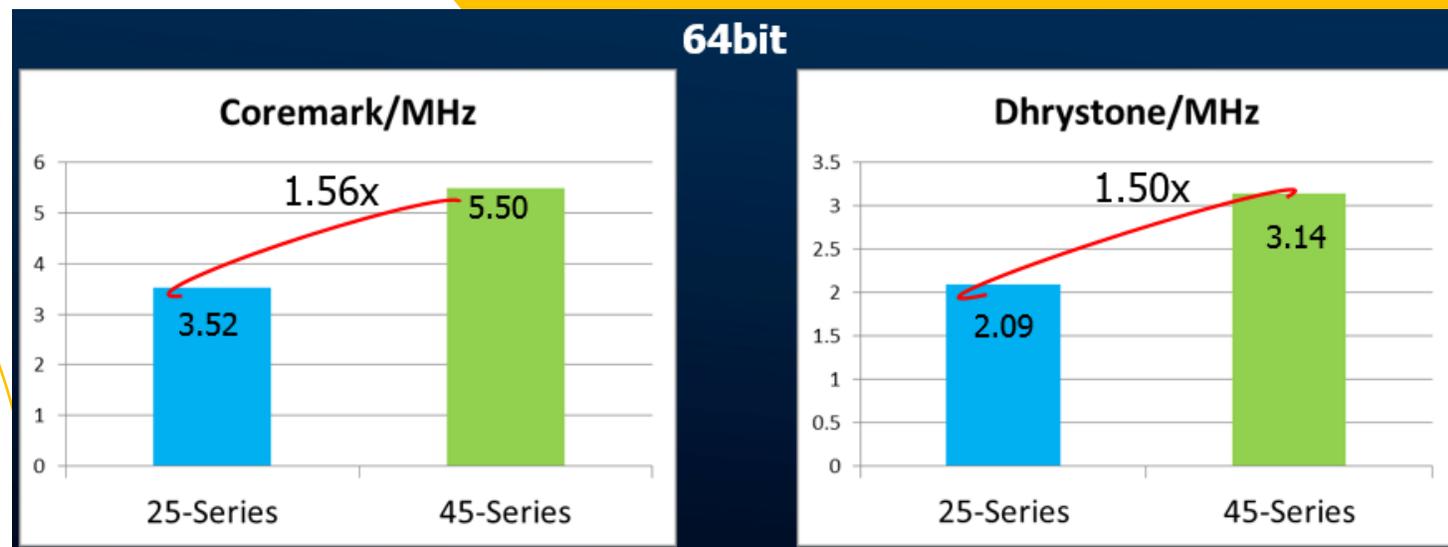
- 8-stage In-Order Dual-Issue
- AndeStar™ V5 ISA:
 - RV*GCN (S/D FPU): All Series
 - RV*P-ext (DSP/SIMD): D45/A(X)45
 - MMU for Linux Applications: A(X)45
- MemBoost memory subsystem
- Low power dynamic branch prediction
- Unaligned data accesses
- Fast or small multiplier
- StackSafe™ (Andes Ext.)
- CoDense™ (Andes Ext.)
- Multi-core support: A(X)45MP
 - up to 8 cores



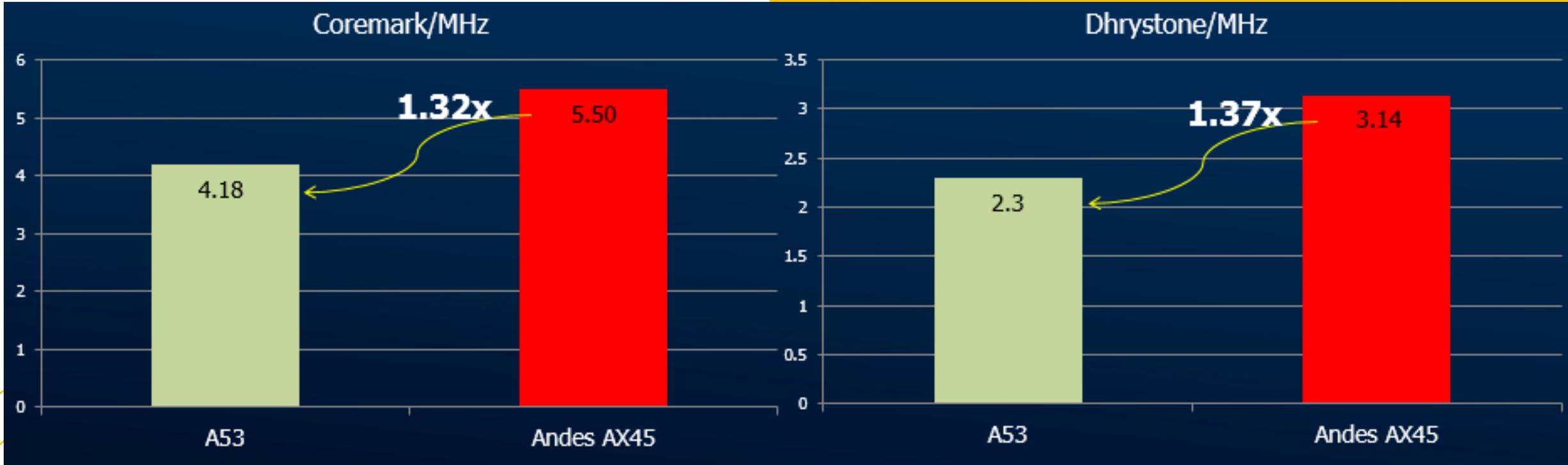
AndesCore™ 45 vs. 25 Series Performance Enhancement



- **> 1.5X** Coremark & Dhrystone performance enhancement, compared with single-issue 25 series



AX45 Can Do More (vs. 64bit A-series)



■ A53

- 8-stage In-Order Dual Issue
- **Widely adopted by industries in many applications**

■ AX45

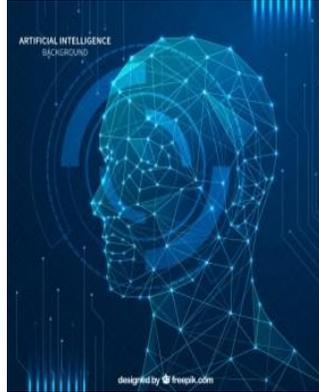
- 8-stage In-Order Dual Issue
- **Performance is better!**
 - Coremark/MHz: 1.32x
 - Dhrystone/MHz: 1.37x

Target Applications for 27 & 45-Series

■ AI/Deep Learning

■ AR/VR

■ 5G



■ Video Surveillance

■ ADAS



■ Networking



■ V2X (Vehicle to Everything)



■ IVI (In-Vehicle-Infotainment)

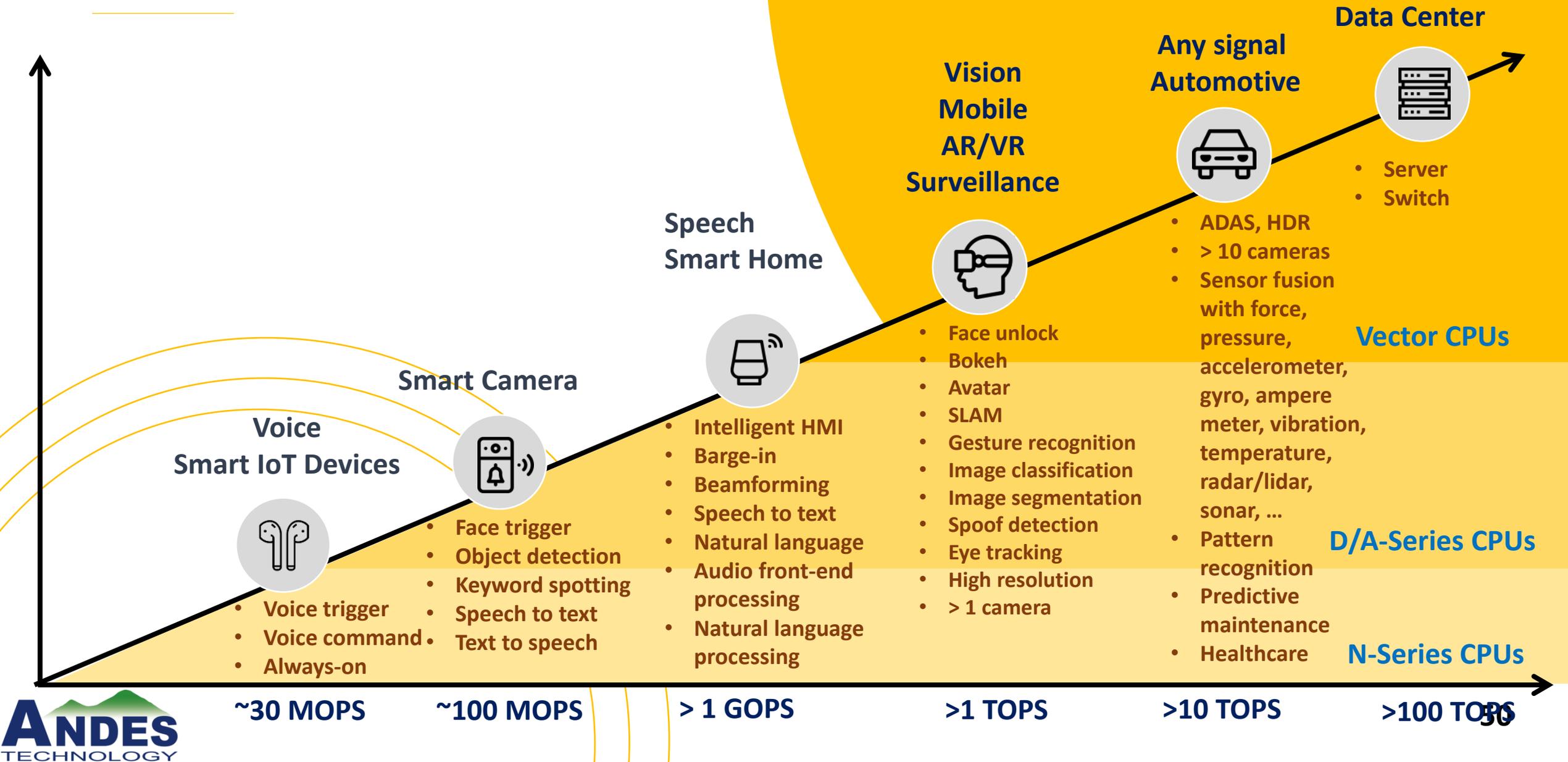


■ Storage



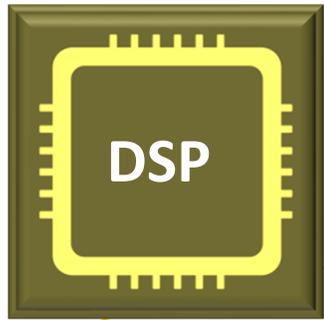
Metaverse and more...

Andes RISC-V Processors Fit in Emerging Applications

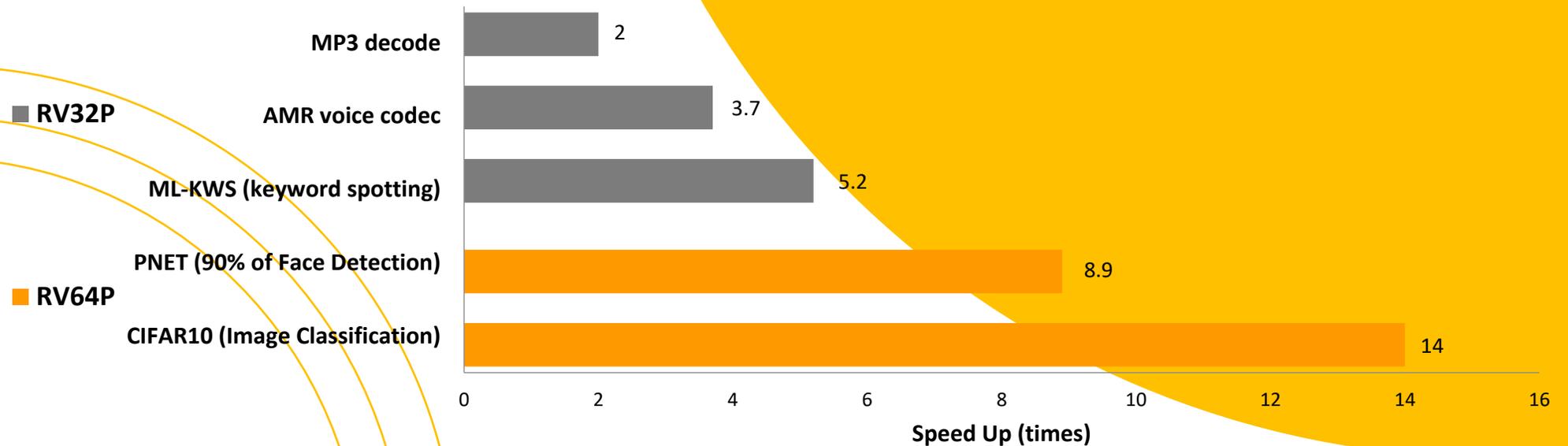


RISC-V DSP Extension

- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads

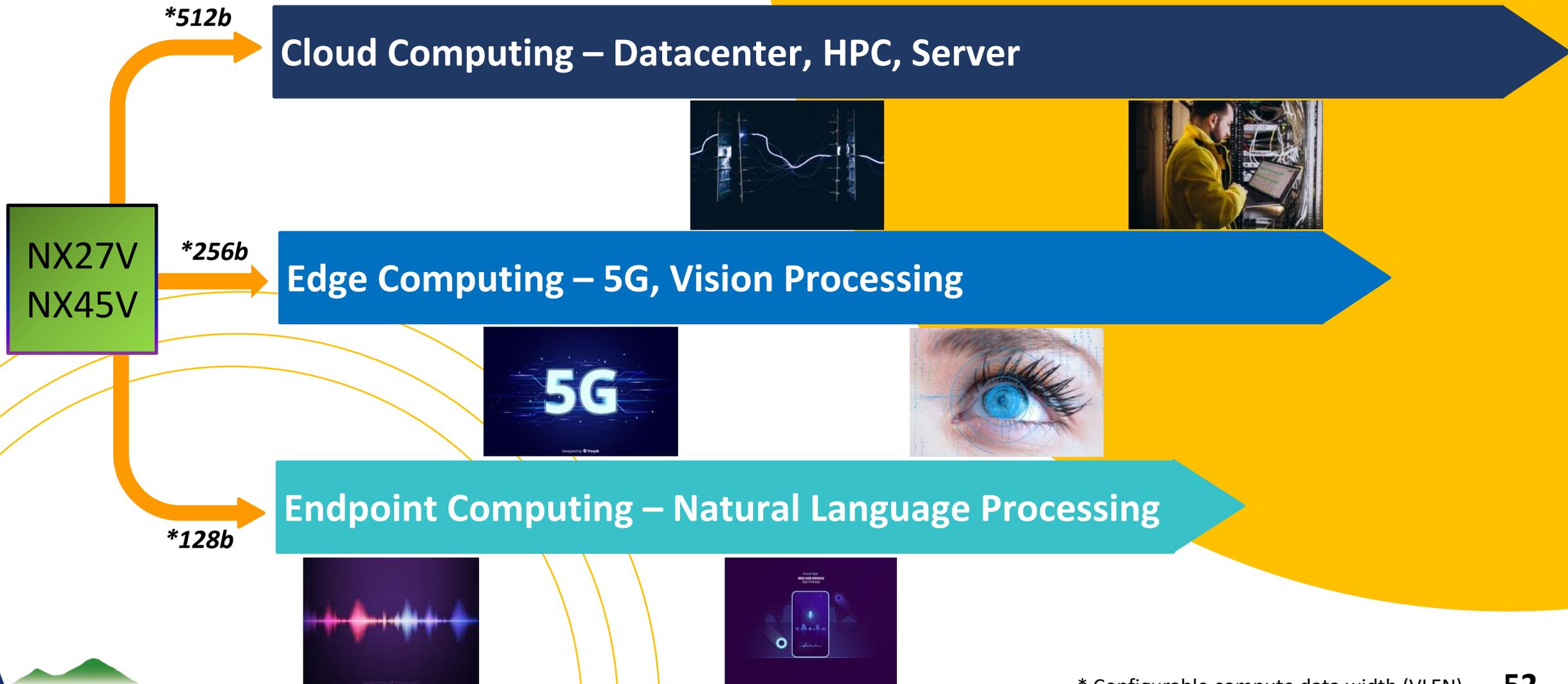


Real world speedup using P-Extension



❖ Increase power efficiency to your DSP applications

Andes Vector Processors: One for All Implementations



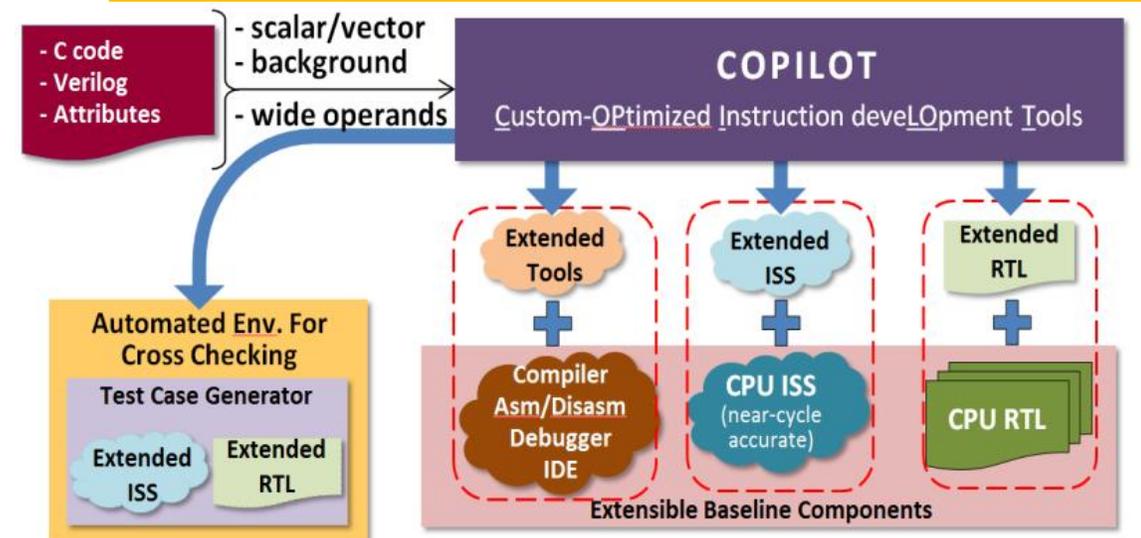
Andes Custom Extension



- ❖ ACE unlocks RISC-V's Potential of DSA
 - Define ACE instruction to handle time critical codes
 - Another approach to co-processor or accelerators

❖ All-in-one **COPILOT** development environment

- Automation tool and ease of use
- Extensions are easy to re-use, can be used as a library



Taking RISC-V Cores to Next Level

❖ Andes is the world-leading supplier shipping the commercial RISC-V cores to market with the support of

P-Extension

- D25, D45, A(X)25(MP), A(X)27(L2), A(X)45(MP)

V-Extension

- NX27V, NX45V

Custom-Extension

(w/ ACE* support)

- Entire 25, 27, 45 series

Bring Andes Strength to RISC-V Cores

Performance & Extensibility

- Leading PPA and code size
- Rich data processing in P, V, and ACE

Configurability

- Flexible configurations for rich features

Maturity

- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE

Aggressive in RISC-V Community

Foundation Task Groups (partial list)



- ❖ Contributing hardware architecture extensions
 - Chair of the P-extension (Packed SIMD/DSP) Task Group
 - Co-chair of Fast Interrupts Task Group
 - Closely reviewing activities of other Task Groups

Andes Helps Strengthen RISC-V Ecosystem

- ❖ More choices for customers are good
- ❖ Andes works closely with partners to grow RISC-V ecosystem



Andes Position in RISC-V



Complete product portfolio

Reliable RISC-V core IP vendor

Extreme low power consumption, high computing efficiency

World's leading P-, V- and Custom-Ext. Capable RISC-V cores

Professional custom computing service

Concluding Remarks

A Trusted Computing Expert

Andes Technology

Successfully rolled out new series of RISC-V cores (w/ leading P-, V- and Custom-Ext.), custom computing service and FreeStart program to extend more oppty.

Aggressively involved in RISC-V International new technology development, contributing and leveraging RISC-V eco-system.

Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry

Thank You

<http://www.andestech.com>

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