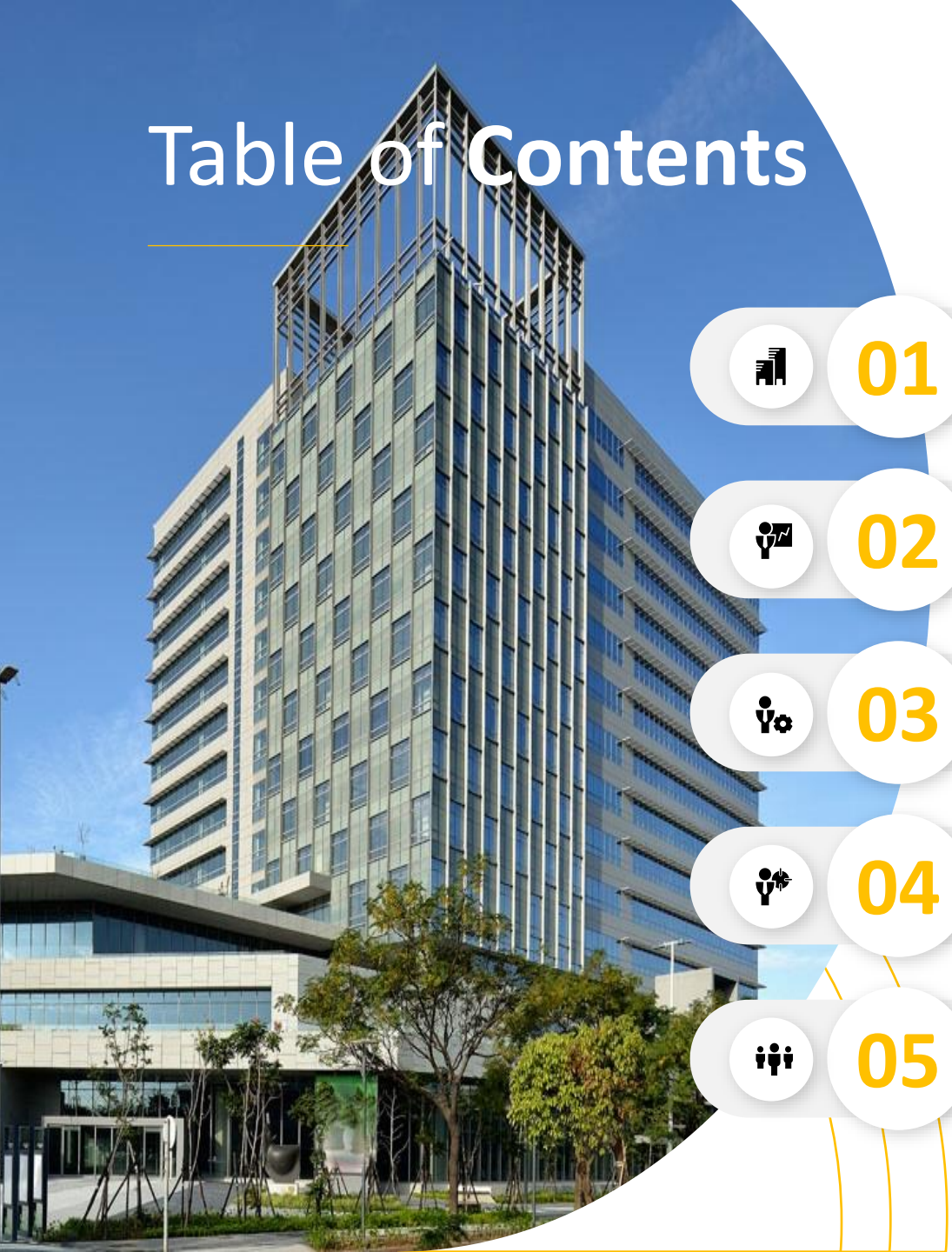
Andes Technology Corp.
Investor Conference Report

ANDES TECHNOLOGY

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.



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Company Overview

http://www.andestech.com

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Over 240 people; 80% are engineers.
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- Al Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)
- Hsinchu Science Park Innovation Award - AndesCore™ NX27V (2020)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

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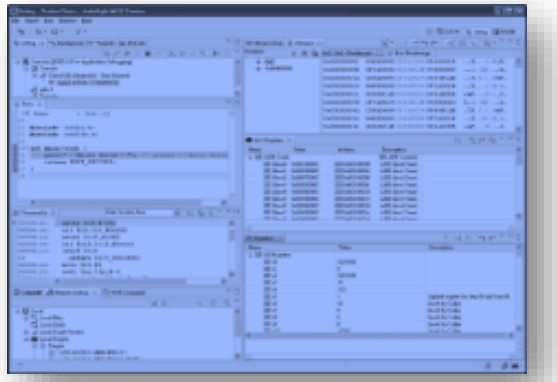
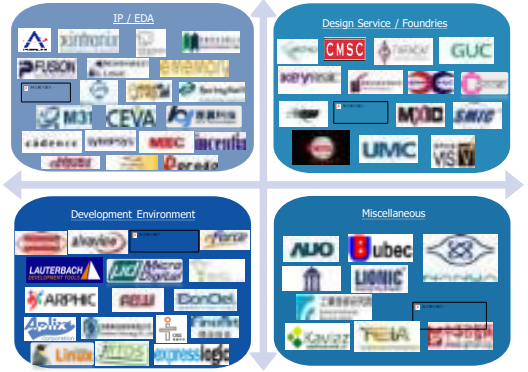
Business Status Overview

- **200+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **500+** license agreements signed
- AndeSight™ IDE:
  - **21,000+** installations
- Eco-system:
  - **500+** partners
- **8B+** Accumulative SoC Shipped





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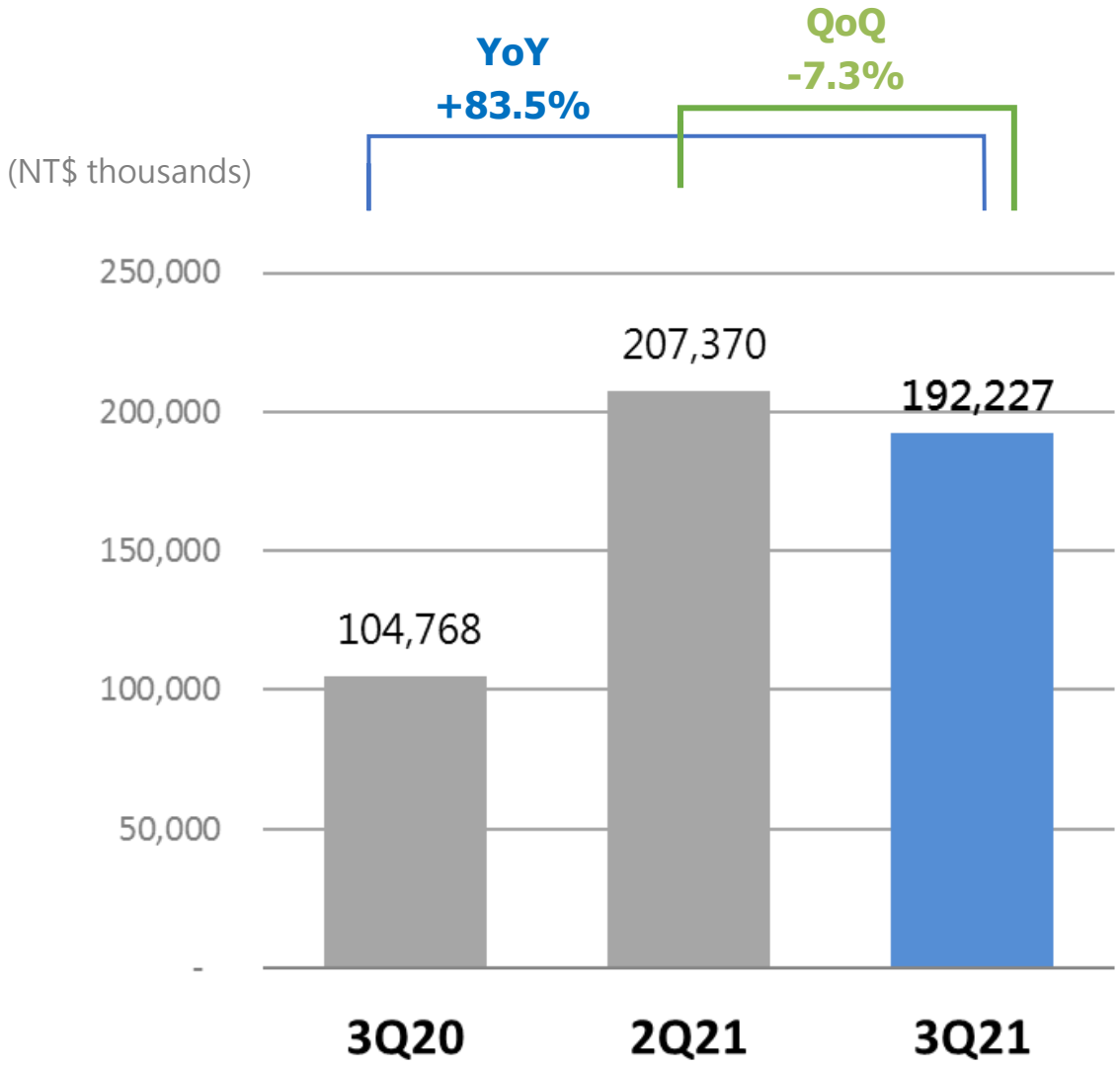
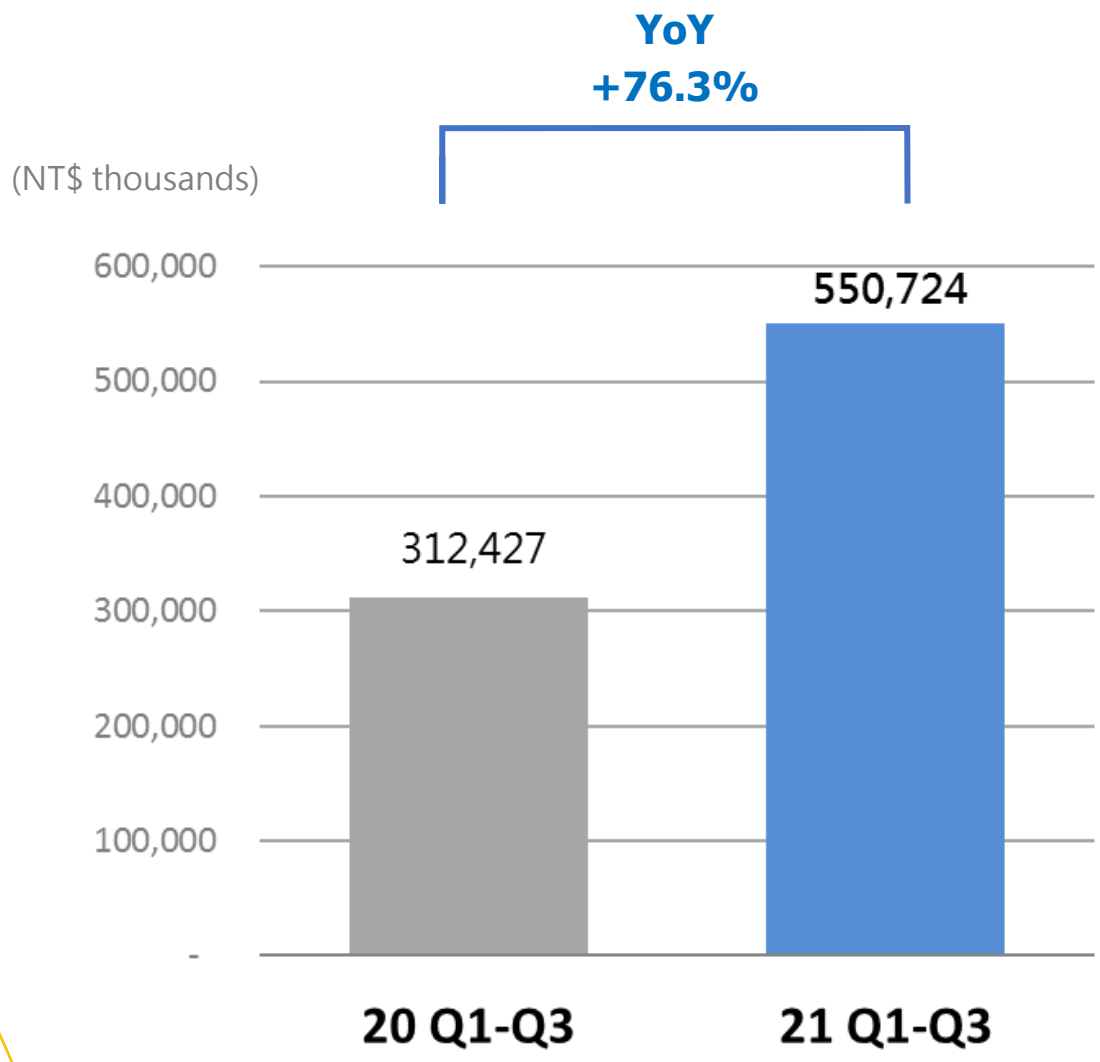
Operation Results

http://www.andestech.com

3Q21 Revenue Analysis

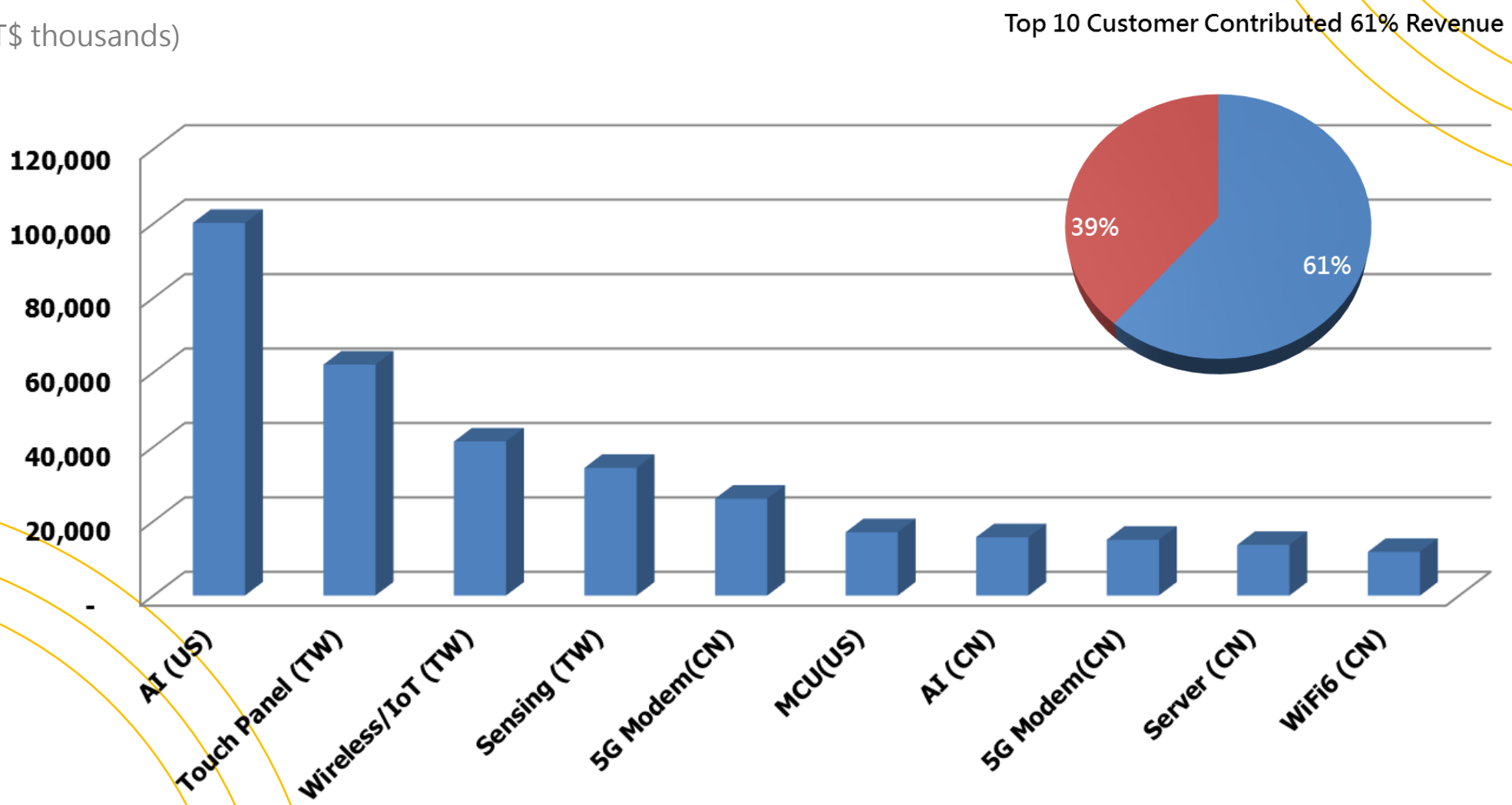


21Q1-Q3 Revenue Analysis

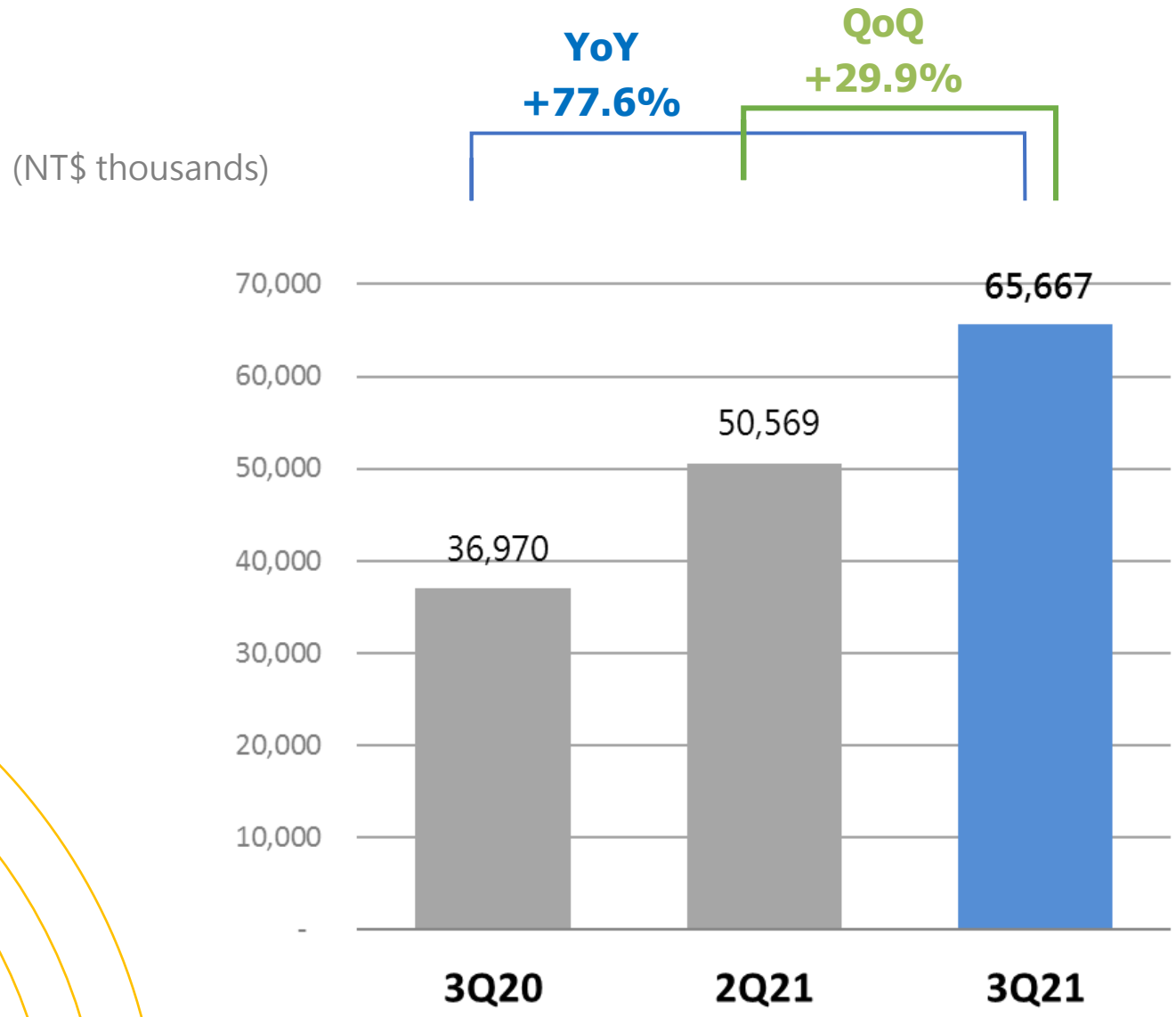


21Q1-Q3 Top 10 Customers Analysis by Revenue

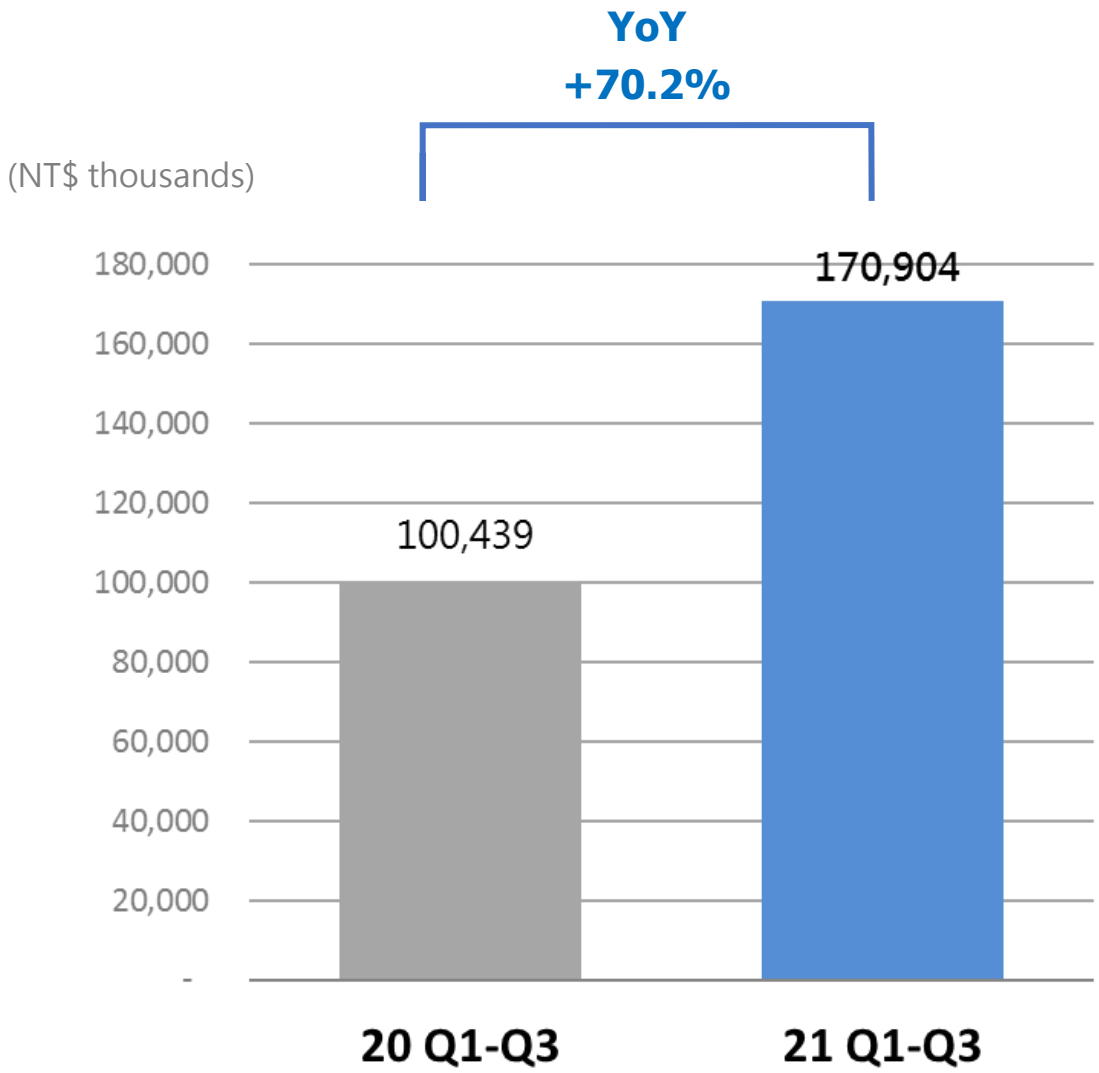
(NT$ thousands)



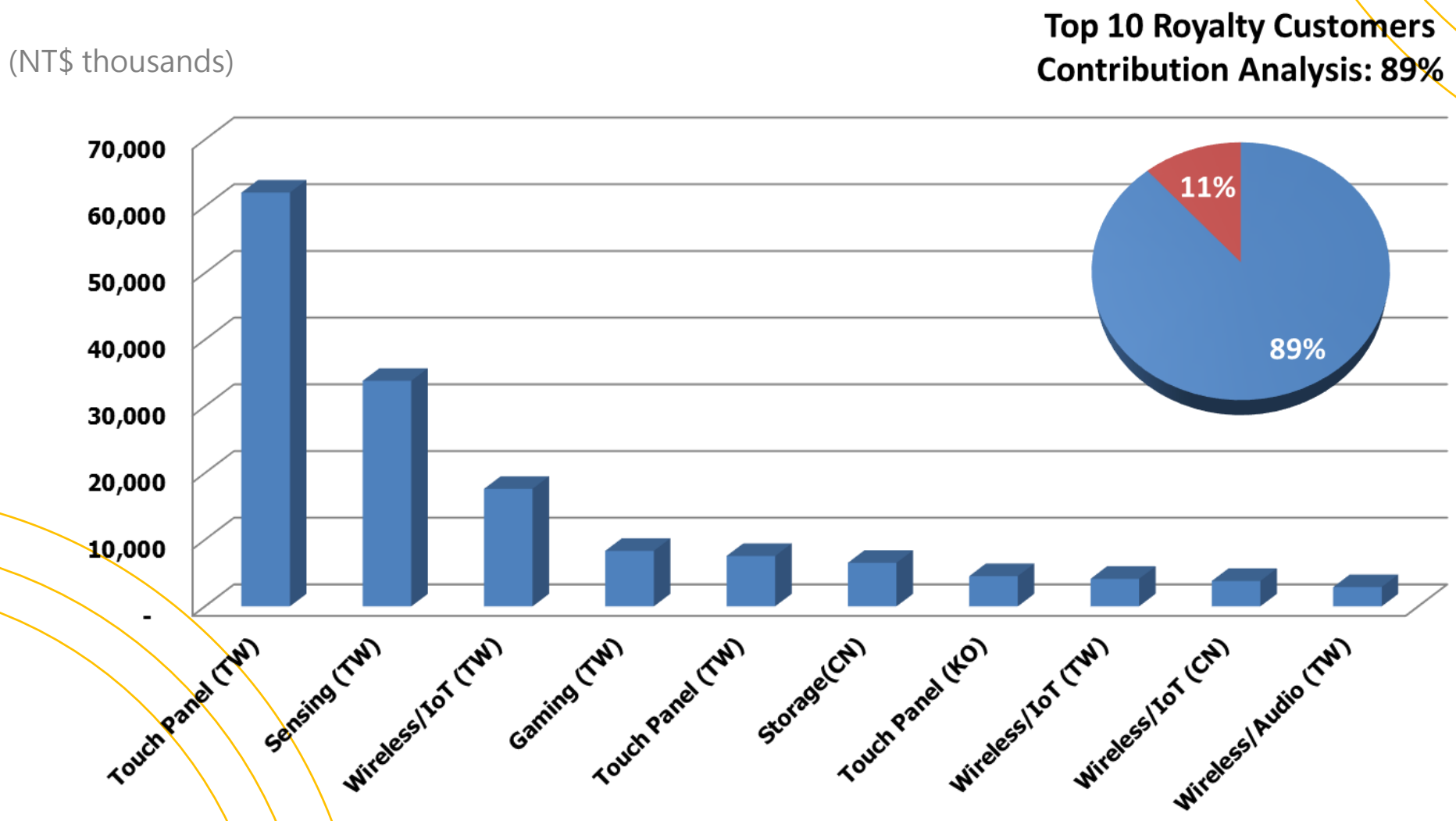
3Q21 Royalty Analysis



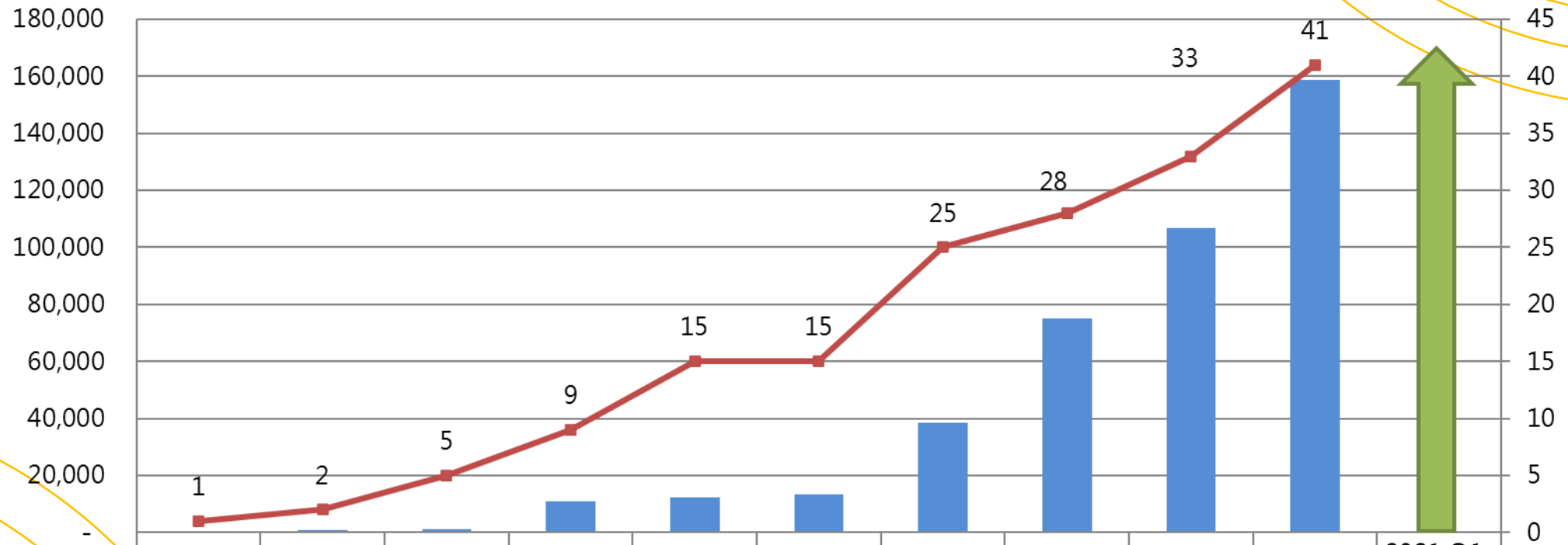
21Q1-Q3 Royalty Analysis



21Q1-Q3 Top 10 Royalty Contributors Analysis by Application

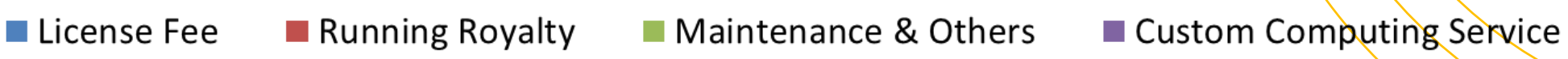


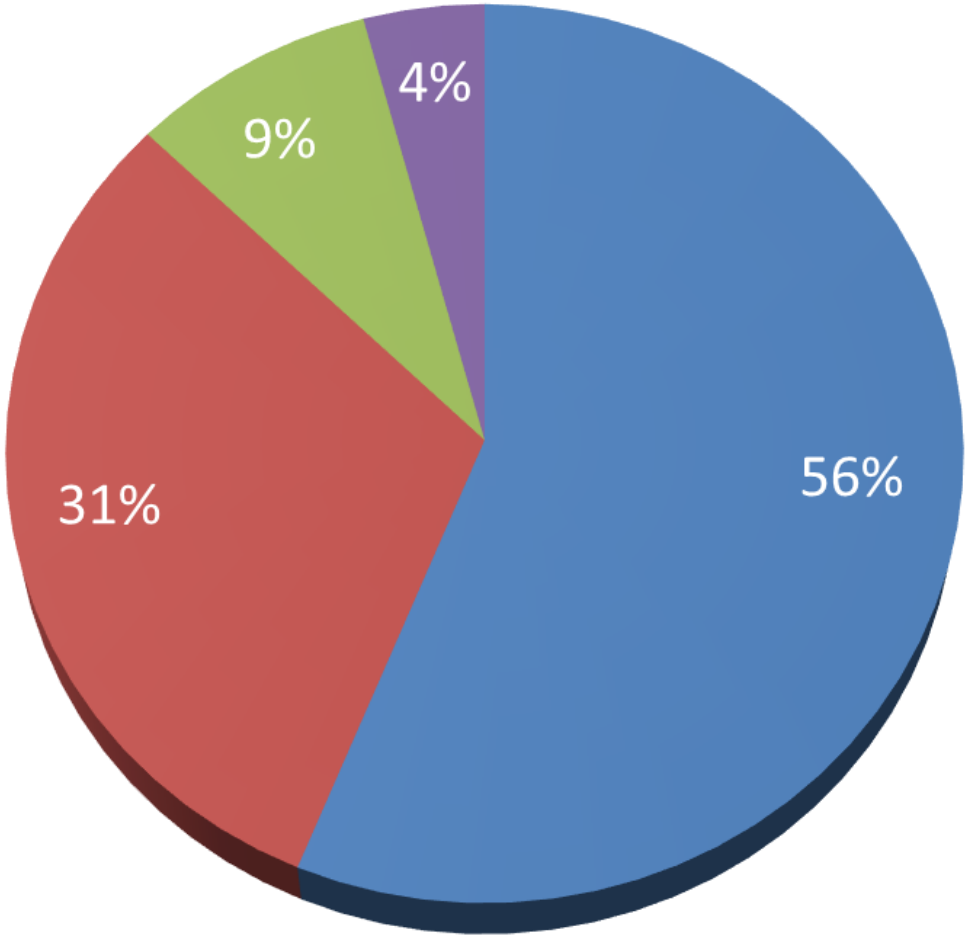
Royalty Analysis



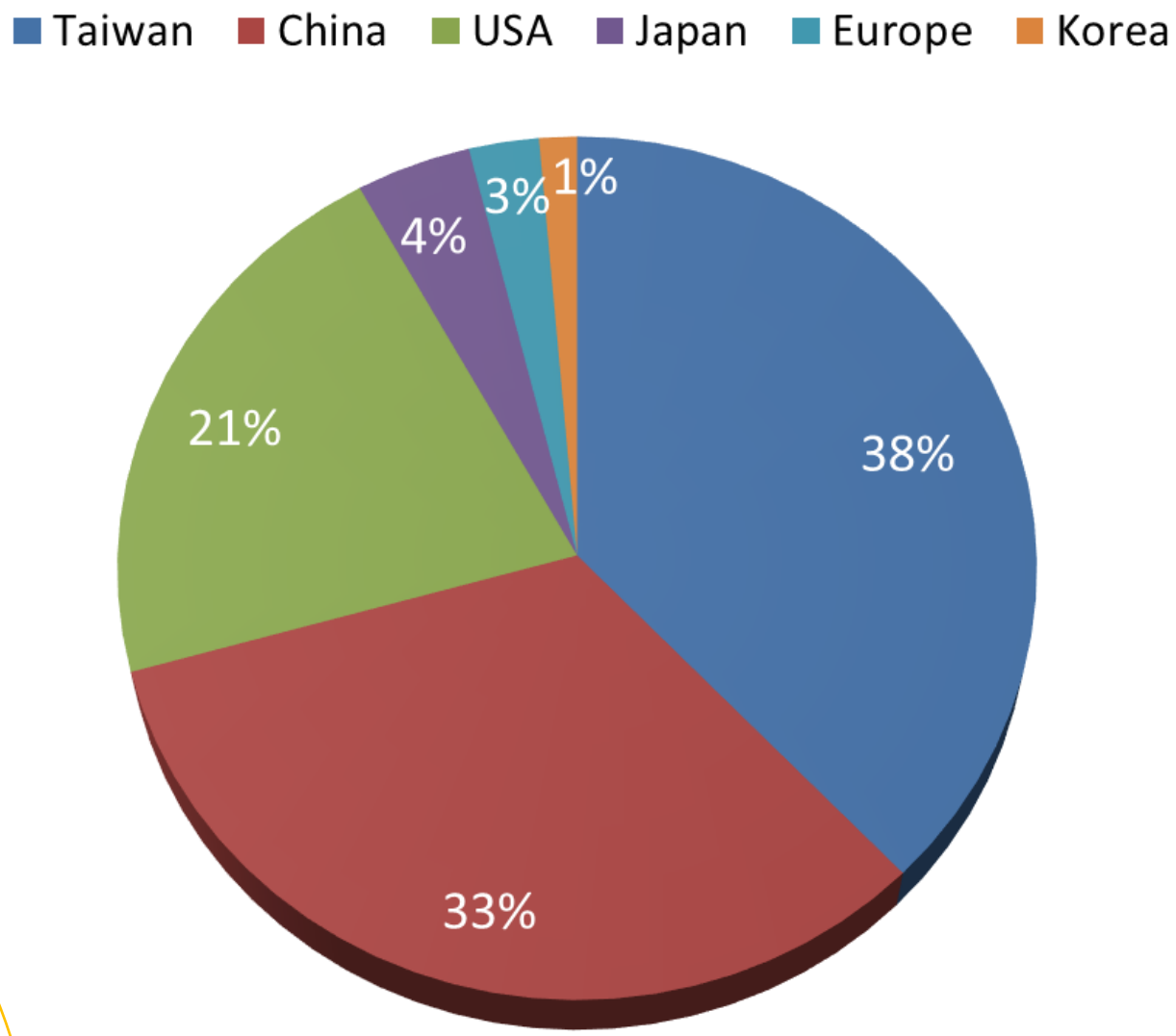
	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021 Q1-Q3
Royalty	445	660	1,285	10,819	12,232	13,320	38,287	74,953	106,716	158,792	170,904
Customer numbers	1	2	5	9	15	15	25	28	33	41	

21Q1-Q3 Revenue Analysis by Payment Model

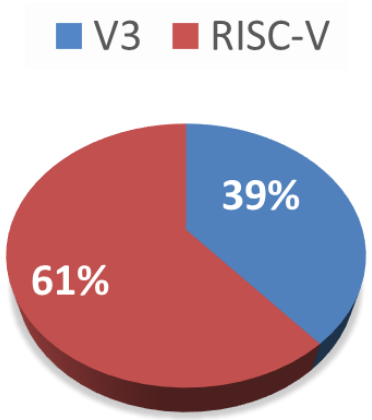


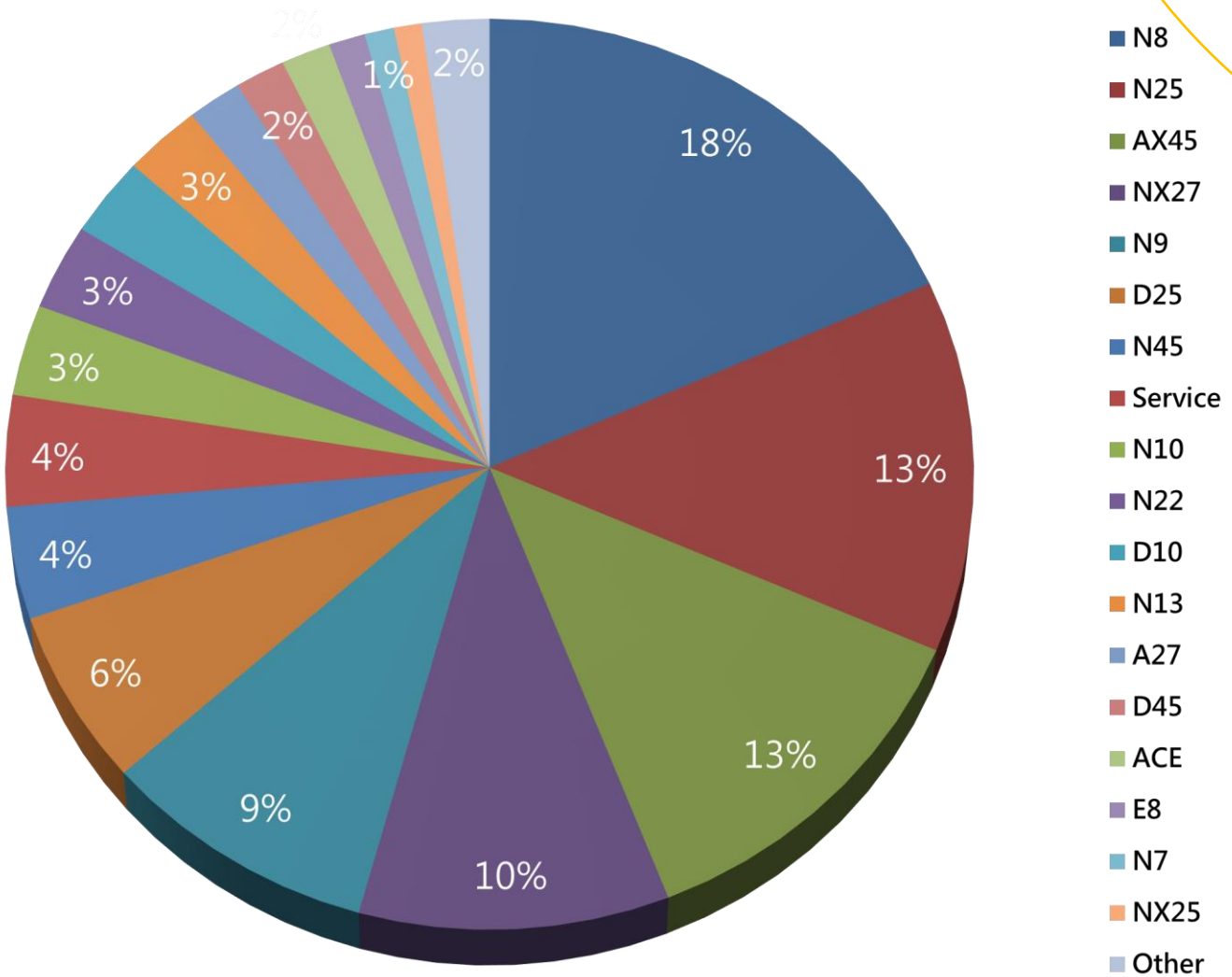


21Q1-Q3 Revenue Analysis by Region



21Q1-Q3 Revenue Analysis by Product





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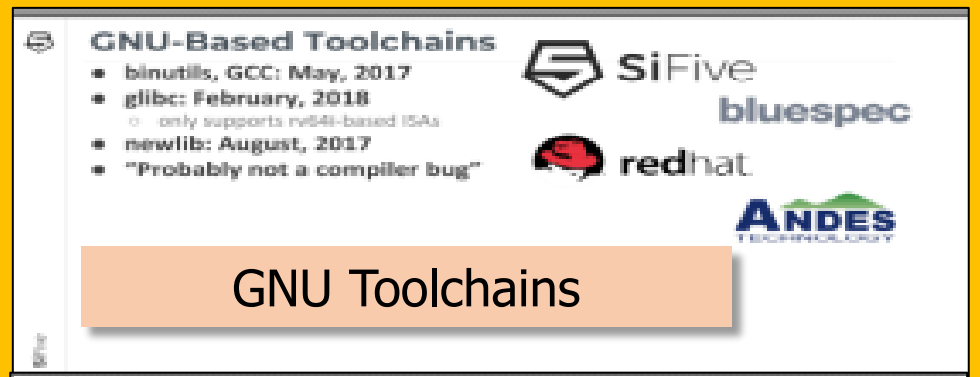
Product Applications

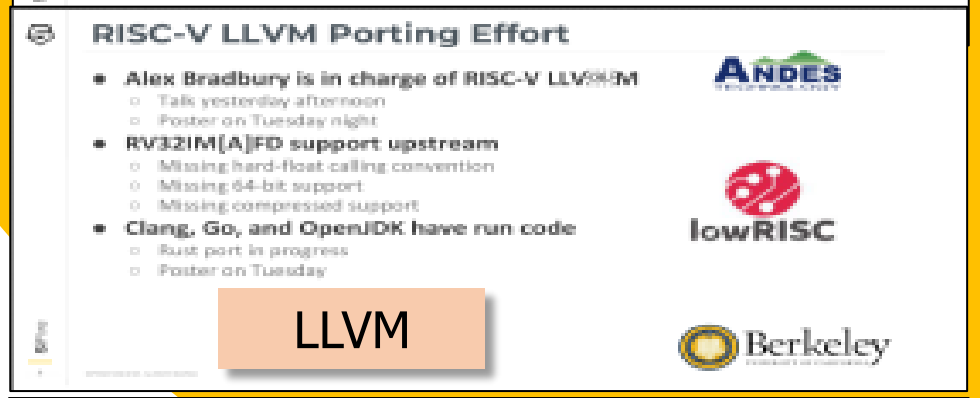
http://www.andestech.com

Andes Updates

- A **16**-year-old public CPU IP company
- **2B+** Andes-Embedded SoC annually in 2020

- A **founding premier** member of the RISC-V International
- An active role in RISC-V International & its extension task groups
  - **RISC-V Board Director**
  - **Member of Technical Steering Committee**
  - RISC-V Ambassador
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group
  - Vice Chair of TEE Task Group
- A major open source maintainer/contributor





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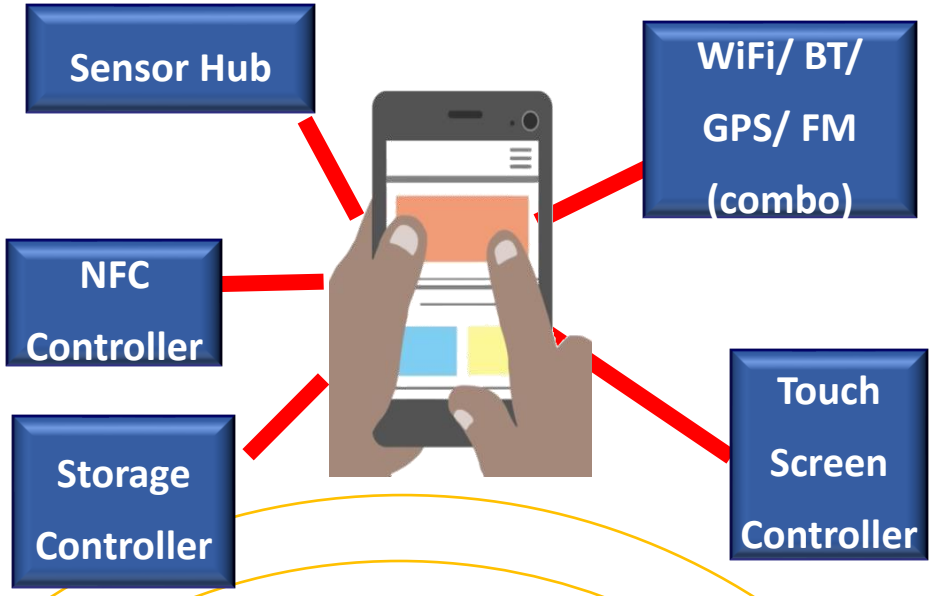
Andes Embedded in Various Applications



Andes Embedded in Smart Phones

Smart Speakers: WiFi IoT

Bike Sharing: GPS Ctrl

X-Trail: ADAS Ctlr

Switch: Game Flash Ctlr

- In leading **machine learning computers** for datacenter
- In tier-one **switch routers** for datacenter
- Recent applications: **5G networking, WiFi 6/7, AI processors** (using Andes Custom Extension, ACE)

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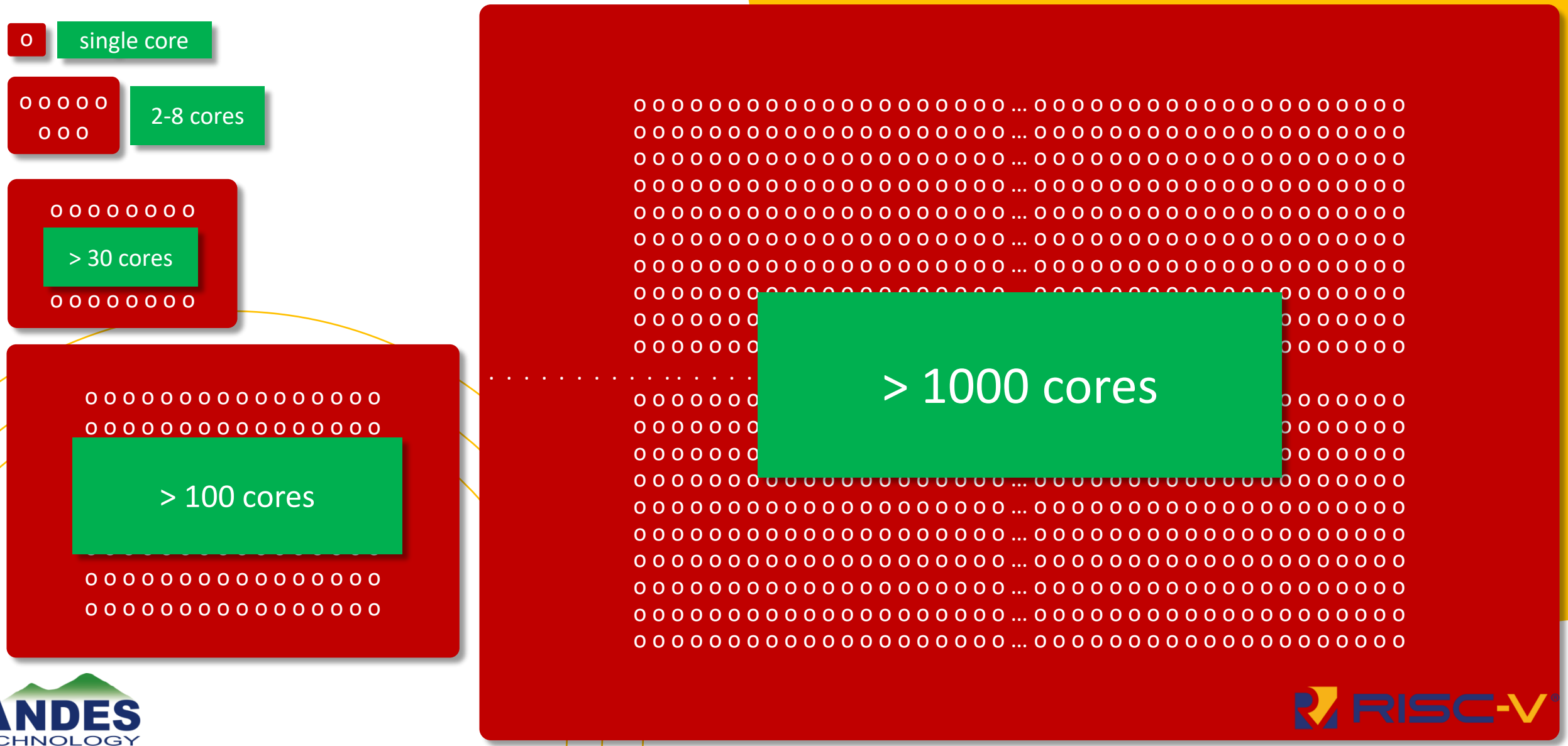
V5 Adoptions: From MCU to Datacenters

- **Edge to Cloud**
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)
- **40nm to 5nm**
- **Many in AI**

- Datacenter AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

Andes RISC-V Cores Adopted in SoC



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RISC-V

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New Products and Ecosystems

http://www.andestech.com

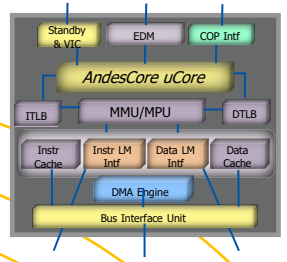
Andes RISC-V Product Overview

Best extensions to RISC-V

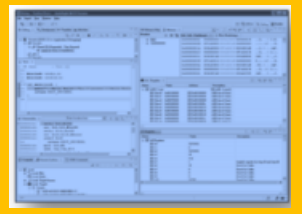
AndeStar™ Architecture V5

AndesCore™ Processors

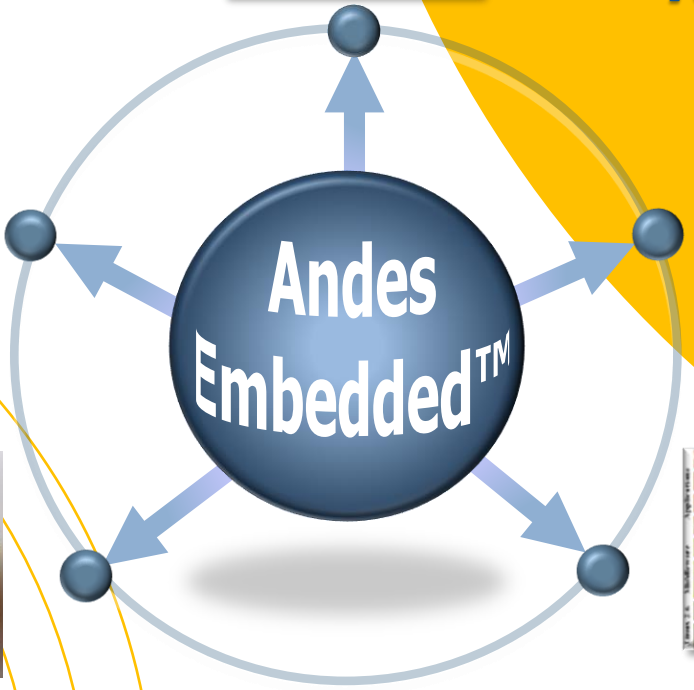
Highly optimized design with leading PPA



AndeSight™ Tools



Professional IDE with high code quality



Handy peripheral IPs to speed up SoC construction

AndeShape™ Platforms

Extensive SW stacks from bare metal, RTOS to Linux

AndeSoft™ Stacks

Andes V5 Architecture for All Levels of Computing

AndeStar™ V5 CPUs	Conventional Computing Architecture	Domain Specific Architecture (DSA)
RISC-V RV32/64 / ANDES TECHNOLOGY Andes Extension		
N/D-series N22 N(X)25 D25…	**Leading PPA Embedded Processor** IoT, Sensing, Storage, Audio, GPS	 Andes Custom Extension
A-series A(X)25 A(X)27 A(X)45 Multicore…	**High Performance and Power Efficient AP** 5G, AI, Datacenter, Video Surveillance, Networking	
Vector NX27V NX45V…	**Cray Style, Scalable Vector Processor** Datacenter, Server, Deep Learning	

- Define custom instruction to handle time critical codes
- Better approach for accelerator /co-processor to do particular jobs
- Automation Tool for the generation of toolchain, ISS, partial RTL and verification

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Andes RISC-V Product Roadmap

RV32/RV64

Cache-Coherent 1-4 Cores	A25MP AX25MP
Linux with FPU/DSP	A25 AX25
Fast/Compact with FPU/DSP	N25F D25F NX25F

5-stage (1.1 GHz)

N22
2-stage
(700 MHz)

Vector Ext.

27-Series:

Vector Ext.
MemBoost

NX27V
A27/AX27
A27L2/AX27L2
and more.

5-stage (1.1 GHz)

Superscalar

45-Series:

Dual Issue
MemBoost

N45/NX45
D45/DX45
A45/AX45
A45MP/AX45MP
and more.

8-stage (1.2 GHz)

Benefits

512-bit SIMD raises MobileNet by 66x
(CNN for mobile vision)

boost performance by 50%

Raise bandwidth to 3x; Cut latency by 40%

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RISC-V®

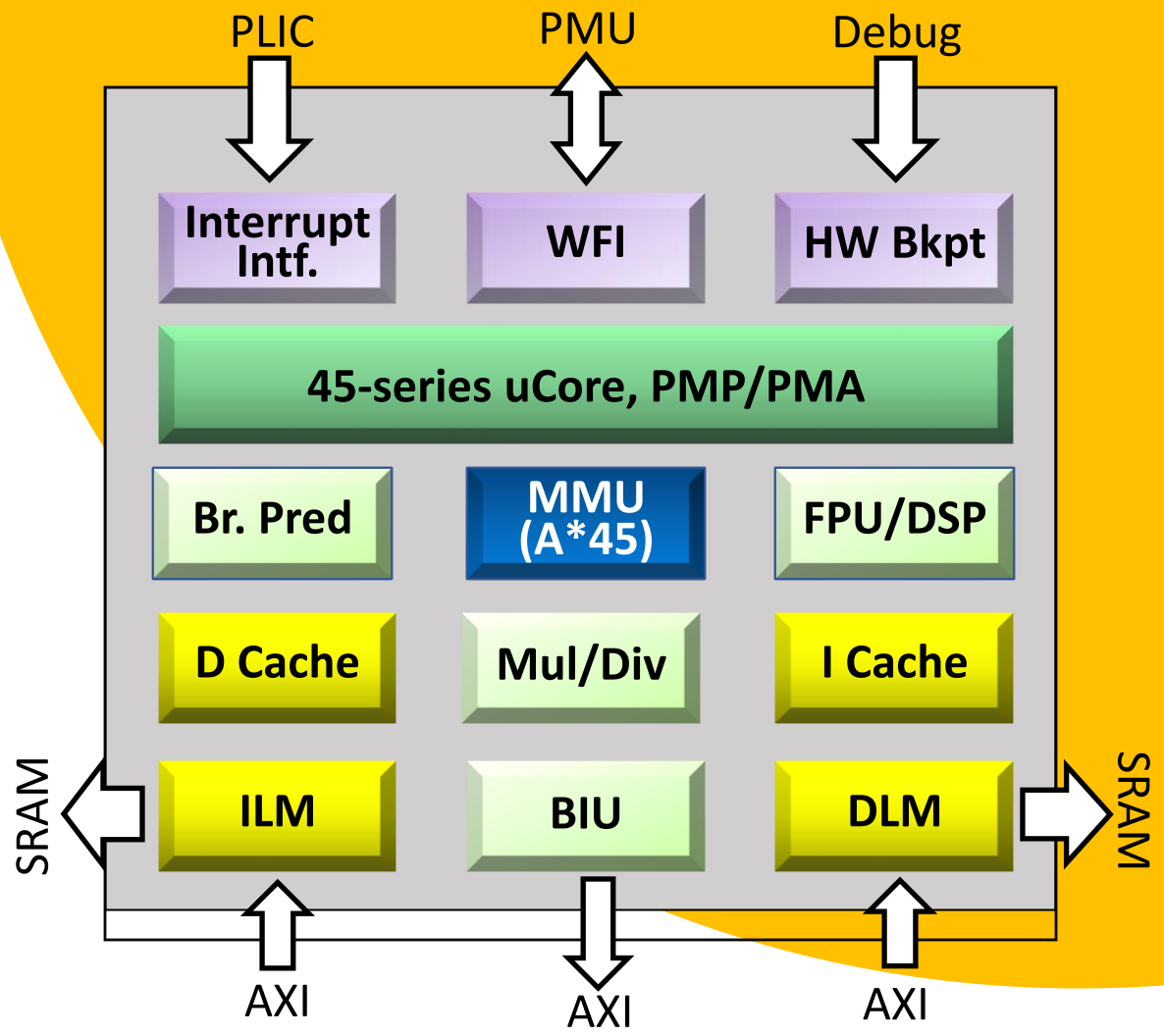
AndeCore™ 45-Series

32-bit AndesCore™ N45/D45/A45/A45MP

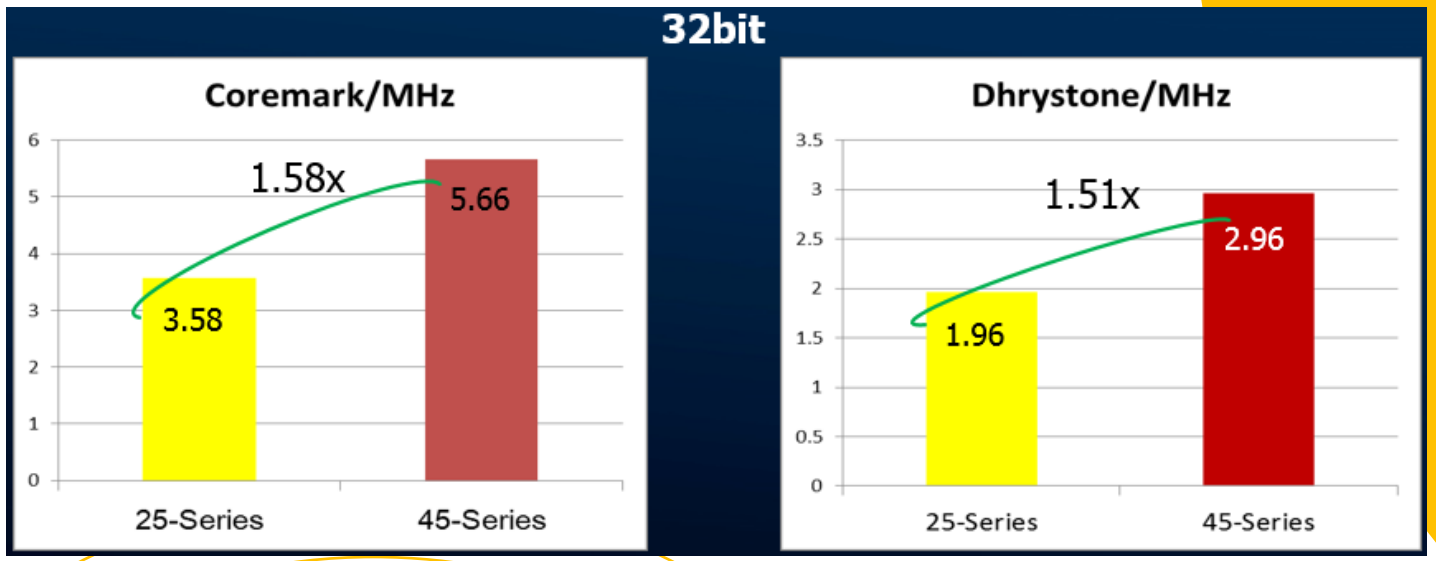
64-bit AndesCore™ NX45/AX45/AX45MP

AndesCore™ 45-Series Overview

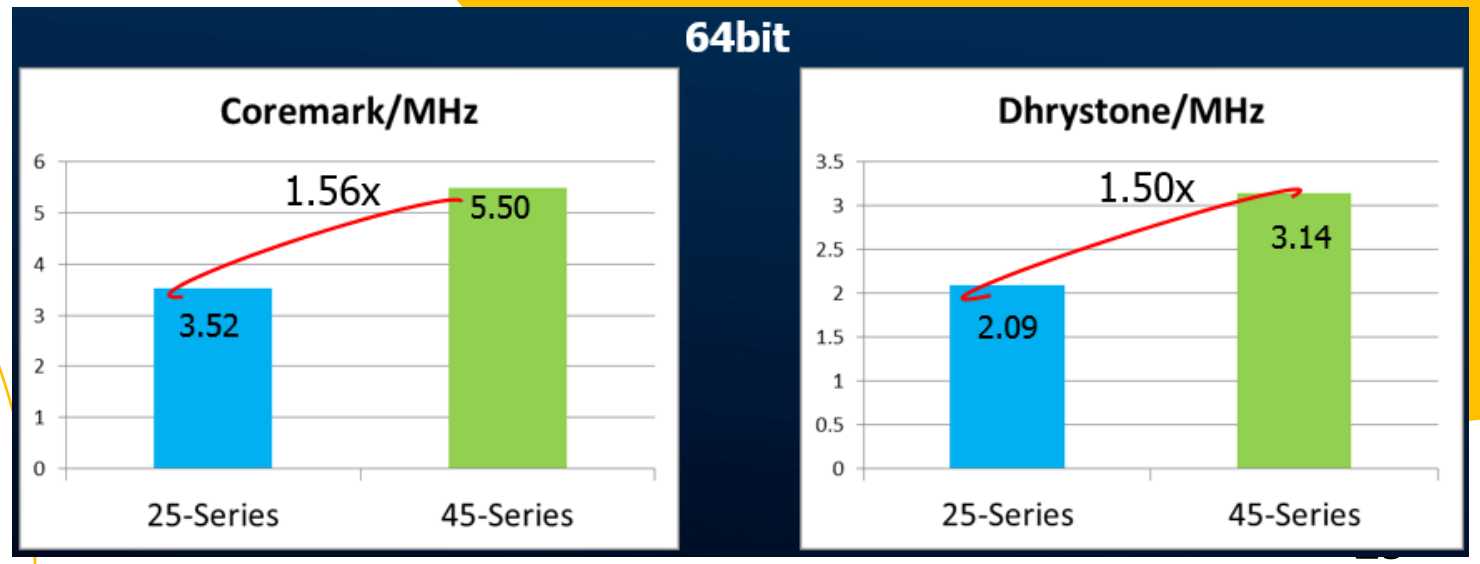
- 8-stage In-Order Dual-Issue
- AndeStar™ V5 ISA:
  - RV*GCN (S/D FPU): All Series
  - RV*P-ext (DSP/SIMD): D45/A(X)45
  - MMU for Linux Applications: A(X)45
- MemBoost memory subsystem
- Low power dynamic branch prediction
- Unaligned data accesses
- Fast or small multiplier
- StackSafe™ (Andes Ext.)
- CoDense™ (Andes Ext.)
- Multi-core support: A(X)45MP



AndesCore™ 45 vs. 25 Series Performance Enhancement



- **> 1.5X** Coremark & Dhrystone performance enhancement, compared with single-issue 25 series



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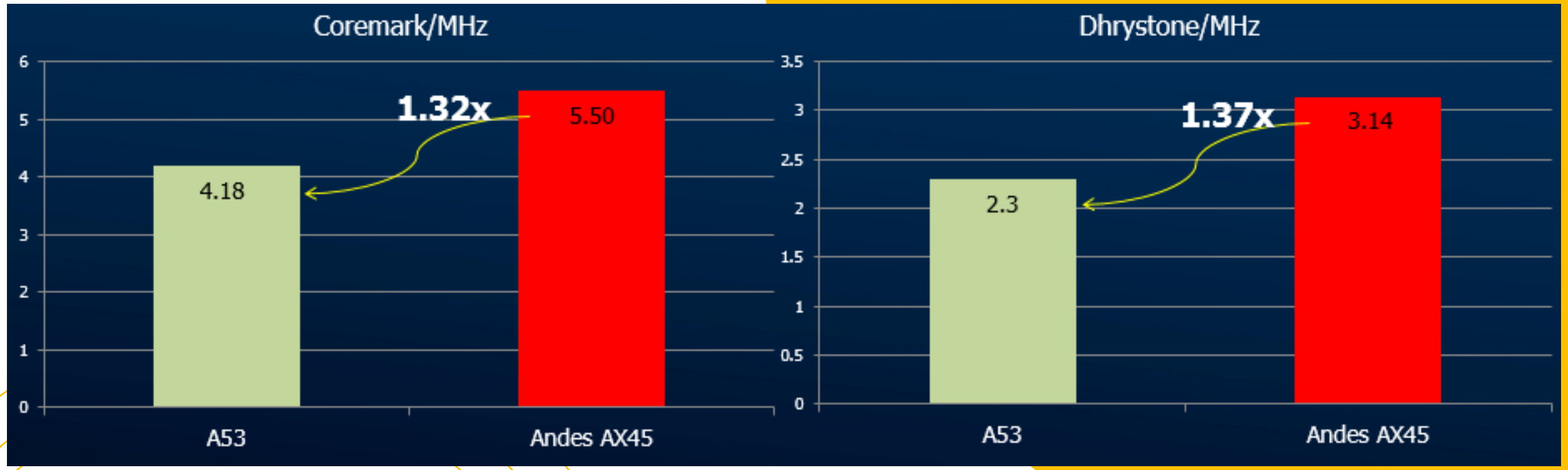
AX45 Can Do More (vs. 64bit A-series)



- **A53**
  - 8-stage In-Order Dual Issue
  - **Widely adopted by industries in many applications**

- **AX45**
  - 8-stage In-Order Dual Issue
  - **Performance is better!**
    - **Coremark/MHz: 1.32x**
    - **Dhrystone/MHz: 1.37x**

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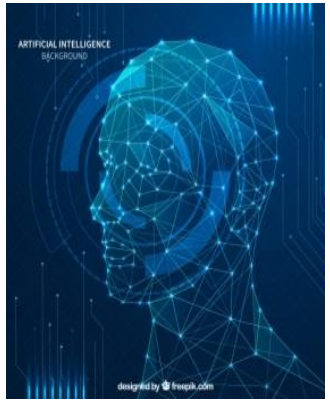
Target Applications of 27 & 45-Series

- AI/Deep Learning
- AR/VR
- 5G



- Networking

- Storage

- Video Surveillance

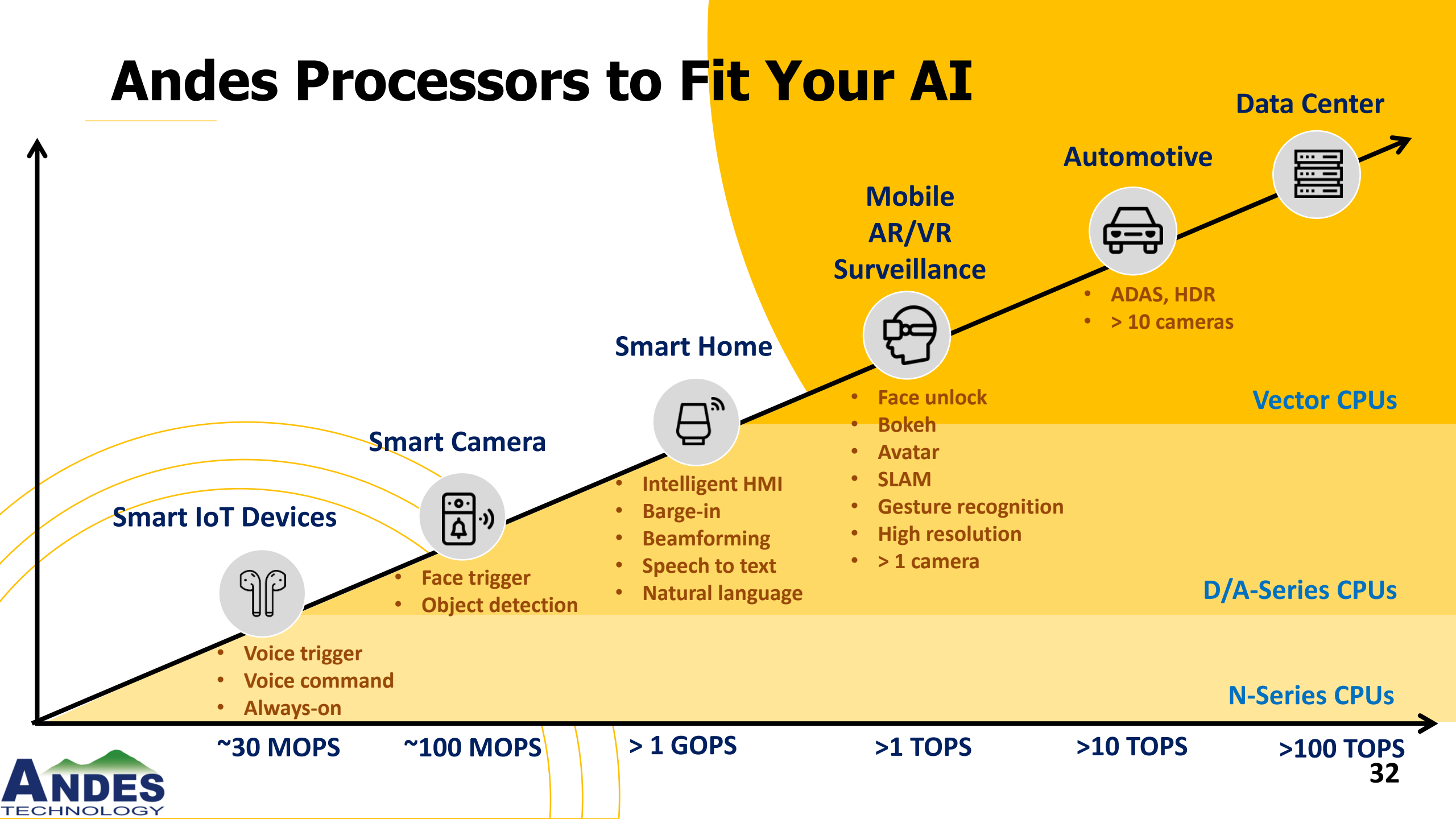
- ADAS

- V2X (Vehicle to Everything)

- IVI (In-Vehicle-Infotainment)

… and More!

Andes Processors to Fit Your AI



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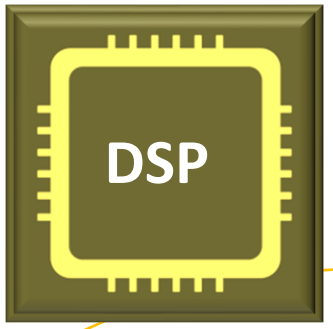
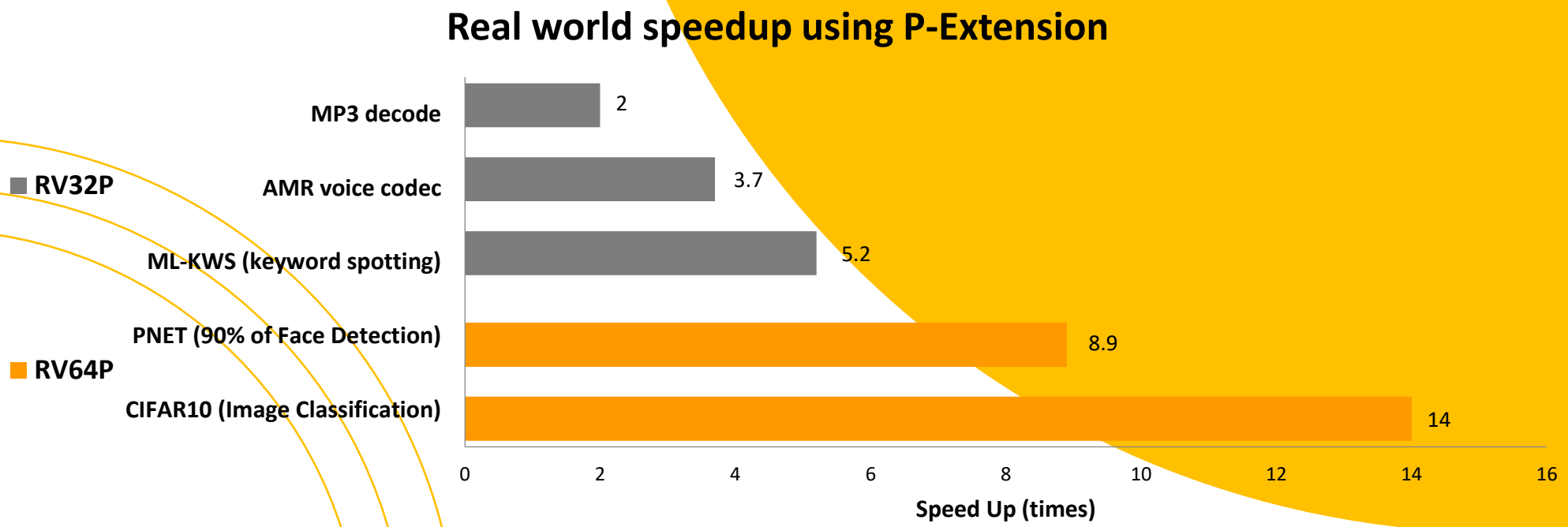
RISC-V DSP Extension

- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads





❖ Increase power efficiency to your DSP applications

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NX27V One Vector for All Implementations

NX27V

*512b → Cloud Computing – Datacenter, HPC, Server

*256b → Edge Computing – 5G, Vision Processing

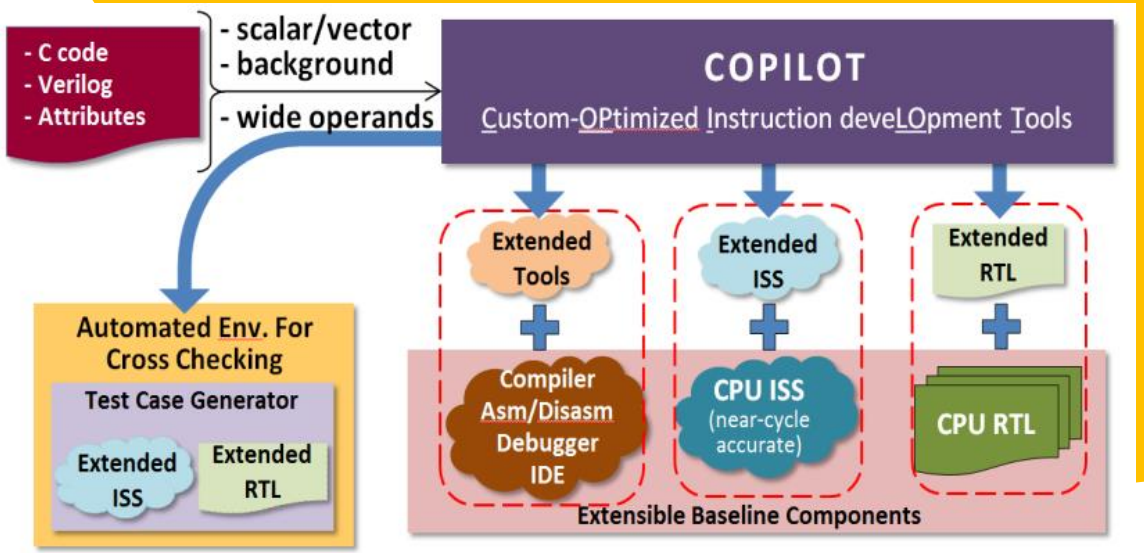
*128b → Endpoint Computing – Natural Language Processing

* Configurable compute data width (VLEN)

Andes Custom Extension

- ❖ ACE unlocks RISC-V's Potential of DSA
  - Define ACE instruction to handle time critical codes
  - Another approach to co-processor or accelerators

- ❖ All-in-one **COPILOT** development environment
  - Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library



Taking RISC-V Cores to Next Level

- Andes is the *world-leading* supplier shipping the commercial RISC-V cores to market with the support of

P-Extension	• D25, D45, A(X)25(MP), A(X)27(L2), A(X)45(MP)
V-Extension	• NX27V, NX45V
Custom-Extension (w/ ACE* support)	• Entire 25, 27, 45 series

*: Andes Custom Extension

Bring Andes Strength to RISC-V Cores

Performance & Extensibility

- Leading PPA and code size
- Rich data processing in P, V, and ACE

Configurability

- Flexible configurations for rich features

Maturity

- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE

Aggressive in RISC-V Community

Foundation Task Groups (partial list)

- Contributing hardware architecture extensions
  - Chair of the P-extension (Packed SIMD/DSP) Task Group
  - Co-chair of Fast Interrupts Task Group
  - Vice Chair of TEE Task Group
  - Closely reviewing activities of other Task Groups

Andes Helps Strengthen RISC-V Ecosystem

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem

Andes Position in RISC-V

- Complete product portfolio
- Reliable RISC-V core IP vendor
- Extreme low power consumption, high computing efficiency
- World's leading P-, V- and Custom-Ext. Capable RISC-V cores
- Professional custom computing service

Two Ecosystems: Andes and Knect.me

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knectme™

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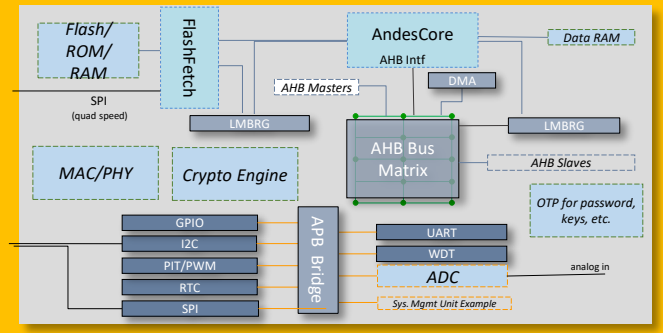
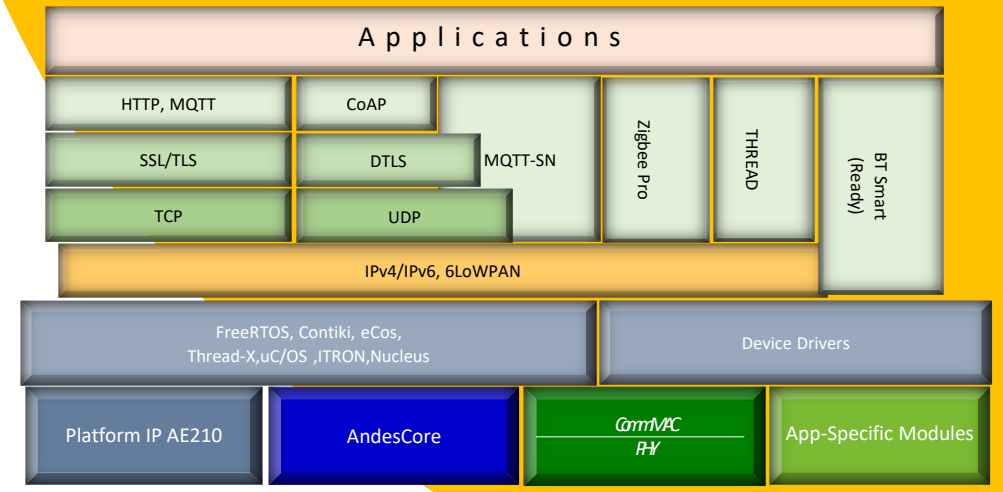
Knect.me™ Ecosystem

- **Built up the community *to* help developing IoT products**
  - To knect solutions for silicon IP's, SW stacks, tools, applications, systems and products
  - Including
    - SoC IP Platforms
    - Software Stack
    - Development Boards
    - Development Tools
- **Forms a IoT League**
  - To knect chip vendors, partners, application developers, system vendors





FreeStart Program

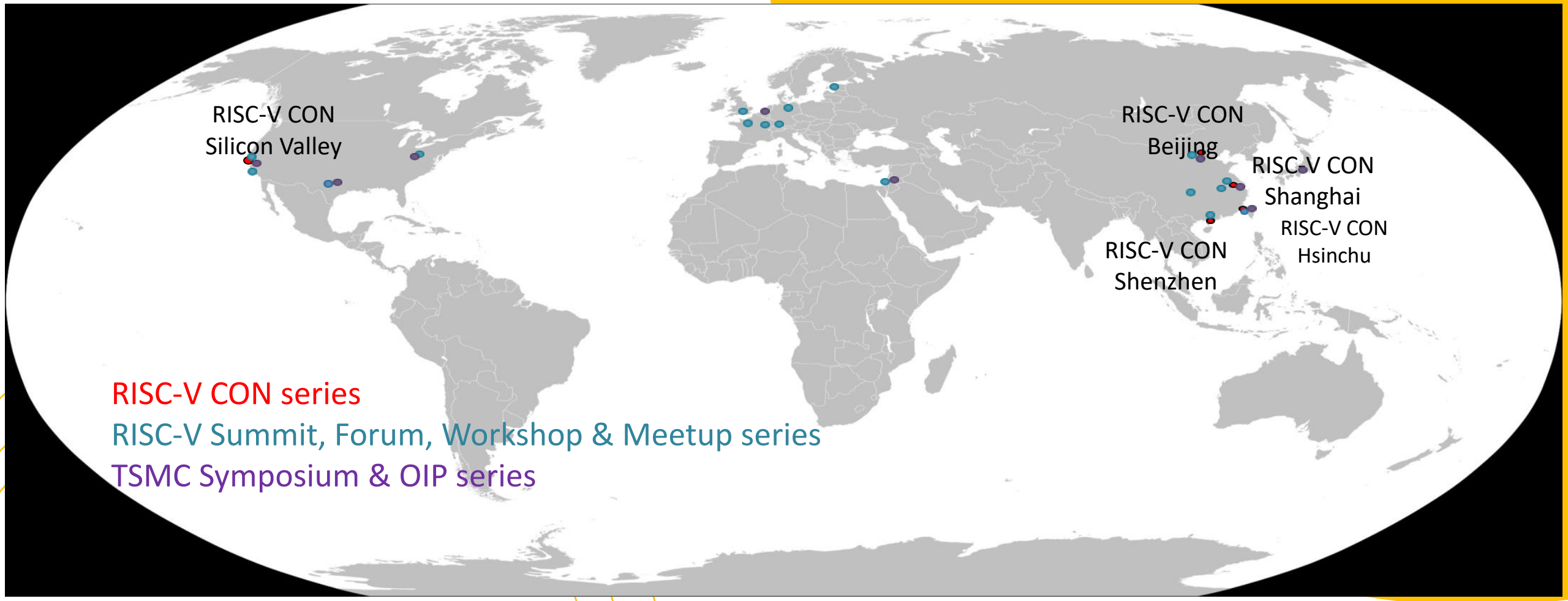
- **FreeStart Evaluation Program (FSEP)**
  - For all RISC-V enthusiasms and educator/researcher
  - Fixed-Configuration N22 RTL
  - Sign simple evaluation agreement directly on website

- **FreeStart Mass-production Program (FSMP)**
  - For industrial and academy mass production
  - Full-configuration N22 RTL
  - License fee: $0; only running royalty is required when mass production

- **Support Package (FSSP)**
  - For all
  - $20K for 1st year, including
    - 1 year e-service
    - FreeStart AE250 RTL
    - Corvette F1 FPGA board

For more info., please visit
www.andestech.com

Event Promotion



RISC-V Summit in San Jose

2020: Diamond Sponsor

Concluding Remarks

http://www.andestech.com

A Trusted Computing Expert

Successfully rolled out new series of RISC-V cores (w/ leading P-, V- and Custom-Ext.), custom computing service and FreeStart program to extend more oppty.

Aggressively involved in RISC-V International new technology development, contributing and leveraging RISC-V eco-system.

Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry

Thank You

http://www.andestech.com

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RISC-V®