Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
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01. Company Overview
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Company Overview

http://www.andestech.com
• Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
• Well-established high technology IPO company
• Just over 210 people; 80% are engineers.
• EETimes' Silicon 60 Hot Startups to Watch (2012)
• TSMC OIP Award “Partner of the Year” for New IP (2015)
• Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
• AI Global Media Award “Most Outstanding Embedded Processor IP Supplier– 2020”

Andes Mission

• Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

• Smart and Green electronic devices
• Cloud Computing and Internet of Things and Machine Learning
Business Status Overview

- **200+** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
  - **400+** license agreements signed

- **AndeSight™ IDE:**
  - **17,000+** installations

- **Eco-system:**
  - **150+** partners

- **6B+** Accumulative SoC Shipped
Operation Results

http://www.andestech.com
Agreement Growth Analysis

IP agreements

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Accumulated IP agreements

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1Q-3Q20 Revenue Analysis

YoY -13.6%

(NT$ thousands)

2019 Q1-Q3: 361,647
2020 Q1-Q3: 312,427

Revenue Comparison for 2019 Q1-Q3 and 2020 Q1-Q3
3Q20 Revenue Analysis

YoY -18.1%  
QoQ +2.9%

(NT$ thousands)

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<th>Quarter</th>
<th>Revenue (NT$ thousands)</th>
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<td>127,851</td>
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<td>2Q20</td>
<td>101,797</td>
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<td>3Q20</td>
<td>104,768</td>
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Royalty Analysis

- **Royalty**
  - 2011: 445
  - 2012: 660
  - 2013: 1,285
  - 2014: 10,819
  - 2015: 12,232
  - 2016: 13,320
  - 2017: 38,287
  - 2018: 74,953
  - 2019: 106,716
  - Q1-Q3 2020: 100,439

- **Customer numbers**
  - 2011: 1
  - 2012: 2
  - 2013: 5
  - 2014: 9
  - 2015: 15
  - 2016: 15
  - 2017: 25
  - 2018: 28
  - 2019: 33
  - Q1-Q3 2020: 33
1Q-3Q20 Revenue Analysis by Payment Model

- License Fee: 36%
- Running Royalty: 32%
- Custom Computing Service: 21%
- Maintenance & Others: 11%
1Q-3Q20 Revenue Analysis by Region

Taiwan: 42%
USA: 28%
China: 23%
Korea: 5%
Europe: 1%
Japan: 1%
1Q-3Q20 Revenue Analysis by Product

- **V3**: 44%
- **RISC-V**: 34%
- **Custom Computing**: 22%

**Other Products**:
- **N8**: 23%
- **Customized IP**: 14%
- **D25**: 13%
- **N9**: 10%
- **N25**: 10%
- **Service**: 8%
- **AX25**: 6%
- **N10**: 5%
- **N13**: 2%
- **N7**: 2%
- **ACE**: 1%
- **AndeSight**: 1%
- **EVB**: 1%
- **OTHERS**: 1%

**Total Revenue**

![Pie Chart](Image)
3Q20 Revenue Analysis - RISC-V

(NT$ thousands)

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<td>54.0%</td>
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V3  RISC-V  Custom Computing
Andes Updates

- A 15-year-old public CPU IP company
- $1.5B+$ Andes-Embedded SoC annually in 2019

- A founding premier member of the RISC-V International
- An active role in RISC-V International & its extension task groups:
  - RISC-V Board Director
  - Vice Chair of Technical Steering Committee
  - RISC-V Ambassador
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group

- A major open source maintainer/contributor
Andes Embedded in Various Applications

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter
- Recent applications: 5G networking, 802.11ax, AI processors (using Andes Custom Extension, ACE)
V5 Adoptions: From MCU to Datacenters

- **Edge to Cloud**
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)

- **40nm to 7nm**
- **Many in AI**

- Datacenter AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells
Andes RISC-V Cores Adopted in SoC

- Single core
- 2-8 cores
- > 30 cores
- > 100 cores
- > 1000 cores
Andes RISC-V Product Overview

AndesStar™ Architecture V5

Best extensions to RISC-V

AndesCore™ Processors

Highly optimized design with leading PPA

AndesShape™ Platforms

Handy peripheral IPs to speed up SoC construction

AndesSoft™ Stacks

Professional IDE with high code quality

AndeSight™ Tools

Extensive SW stacks from bare metal, RTOS to Linux

Andes Embedded™

AndesCore™ uCore

Instr LM

Intf

Data LM

Intf

Standby

& VIC

COP Intf

ITLB

MMU/MPU

DTLB

Instr Cache

Data Cache

DMA Engine

EDM

Highly optimized design with leading PPA

Handy peripheral IPs to speed up SoC construction

Extensive SW stacks from bare metal, RTOS to Linux

Best extensions to RISC-V
Product Lines
Andes RISC-V Product Roadmap

**27-Series:**
- Vector Ext. MemBoost
- NX27V
- A27/AX27 and more.

**45-Series:**
- Dual Issue MemBoost
- N45/NX45
- D45/DX45
- A45/AX45 and more.

**Benefits**
- 512-bit SIMD raises MobileNet by 30x (CNN for mobile vision)
- Boost performance by 50%
- Raise bandwidth to 3x; Cut latency by 40%

**Applications:**
- AIOT, Comm., ML/DL, Multimedia, Networking, Storage
- For data processing as well as control processing

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**Cache-Coherent 1-4 Cores**
- Linux with FPU/DSP
- Fast/Compact with FPU/DSP

**5-stage (1.1 GHz)**
- RV32/RV64
- A25MP AX25MP
- A25 AX25
- N25F D25F NX25F

**512-bit SIMD raises MobileNet by 30x**

**8-stage (1.2 GHz)**
- Superscalar
- N22 2-stage (700 MHz)
### Andes V5 Architecture for All Levels of Computing

#### AndeStar™ V5 CPUs
- **N/D-series**
  - N22 N(X)25 D25...
- **A-series**
  - A(X)25 A(X)27 A(X)45 Multicore...
- **Vector**
  - NX27V, NX45V...

#### Conventional Computing Architecture
- **Leading PPA Embedded Processor**
  - IoT, Sensing, Storage, Audio, GPS
- **High Performance and Power Efficient AP**
  - 5G, AI, Datacenter, Video Surveillance, Networking

#### Domain Specific Architecture (DSA)
- **Andes Custom Extension**
- Define custom instruction to handle time critical codes
- Better approach for accelerator/co-processor to do particular jobs
- Automation Tool for the generation of toolchain, ISS, partial RTL and verification

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RISC-V
Andes Custom Extension
RV32/64
Andes Technology

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High Performance and Power Efficient AP
Datacenter, Server, Deep Learning
Andes Processors to Fit Your AI

- Voice trigger
- Voice command
- Always-on
- Face trigger
- Object detection
- Intelligent HMI
- Barge-in
- Beamforming
- Speech to text
- Natural language
- Face unlock
- Bokeh
- Avatar
- SLAM
- Gesture recognition
- High resolution
- > 1 camera
- ADAS, HDR
- > 10 cameras
- > 30 MOPS
- >100 MOPS
- > 1 GOPS
- >1 TOPS
- >10 TOPS
- >100 TOPS

Smart Camera

Smart IoT Devices

Smart Home

Mobile
AR/VR
Surveillance

Automotive

Data Center

N-Series CPUs

D/A-Series CPUs

Vector CPUs

~30 MOPS
~100 MOPS
> 1 GOPS
>1 TOPS
>10 TOPS
>100 TOPS
RISC-V DSP Extension

- Andes contributed market-proven DSP (SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads

Real world speedup using P-Extension

- MP3 decode: 3.7x
- AMR voice codec: 5.2x
- ML-KWS (keyword spotting): 8.9x
- PNET (90% of Face Detection): 14x
- CIFAR10 (Image Classification): 16x

Increase power efficiency to your DSP applications
NX27V One Vector for All Implementations

- **Cloud Computing** – Datacenter, HPC, Server
  - *512b*

- **Edge Computing** – 5G, Vision Processing
  - *256b*

- **Endpoint Computing** – Natural Language Processing
  - *128b*

* Configurable compute data width (VLEN)
Andes Custom Extension

- ACE unlocks RISC-V’s Potential of DSA
  - Define ACE instruction to handle time critical codes
  - Another approach to co-processor or accelerators

- All-in-one COPILOT development environment
  - Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library
Taking RISC-V Cores to Next Level

- Andes is the worldwide leading supplier shipping the commercial RISC-V cores to market with

  - P-Extension: D25F, A(X)25(MP), A(X)27, A(X)45
  - V-Extension: NX27V, NX45V
  - Custom-Extension (w/ ACE* support): Entire 25, 27, 45 series

*: Andes Custom Extension
Bring Andes Strength to RISC-V Cores

**Performance & Extensibility**
- Leading PPA and code size
- Rich data processing in P, V, and ACE

**Configurability**
- Flexible configurations for rich features

**Maturity**
- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE
Aggressive in RISC-V Community

**Foundation Task Groups (partial list)**

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- Contributing hardware architecture extensions
  - Chair of the P-extension (Packed SIMD/DSP) Task Group
  - Co-chair of Fast Interrupts Task Group
  - Closely reviewing activities of other Task Groups
Andes Helps Strengthen RISC-V Ecosystem

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem
Andes Position in RISC-V

Complete product portfolio

Reliable RISC-V core IP vendor

Extreme low power consumption, high computing efficiency

World’s leading P-, V- and Custom-Ext. Capable RISC-V cores

Professional custom computing service
Two Ecosystems: Andes and Knect.me
Knect.me™ Ecosystem

- **Built up the community to help developing IoT products**
  - To knect solutions for silicon IP’s, SW stacks, tools, applications, systems and products
  - Including
    - SoC IP Platforms
    - Software Stack
    - Development Boards
    - Development Tools

- **Forms a IoT League**
  - To knect chip vendors, partners, application developers, system vendors
FreeStart Program

- **FreeStart Evaluation Program (FSEP)**
  - For all RISC-V enthusiasms and educator/researcher
  - Fixed-Configuration N22 RTL
  - Sign simple evaluation agreement directly on website

- **FreeStart Mass-production Program (FSMP)**
  - For industrial and academy mass production
  - Full-configuration N22 RTL
  - License fee: $0; only running royalty is required when mass production

- **Support Package (FSSP)**
  - For all
  - $20K for 1st year, including
    - 1 year e-service
    - FreeStart AE250 RTL
    - Corvette F1 FPGA board

For more info., please visit www.andestech.com
Event Promotion

RISC-V CON series
RISC-V Roadshow & Workshop Series
TSMC symposium & OIP series

RISC-V Summit in San Jose
2020: Diamond Sponsor
Concluding Remarks
Successfully rolled out new series of RISC-V cores (w/ leading P-, V- and Custom-Ext.), custom computing service and FreeStart program to extend more oppy.

Aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.

Becoming a technology contributor, market promoter, and sales leader in the RISC-V industry
Thank You

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