



Andes Technology Corp. Investor Conference Report

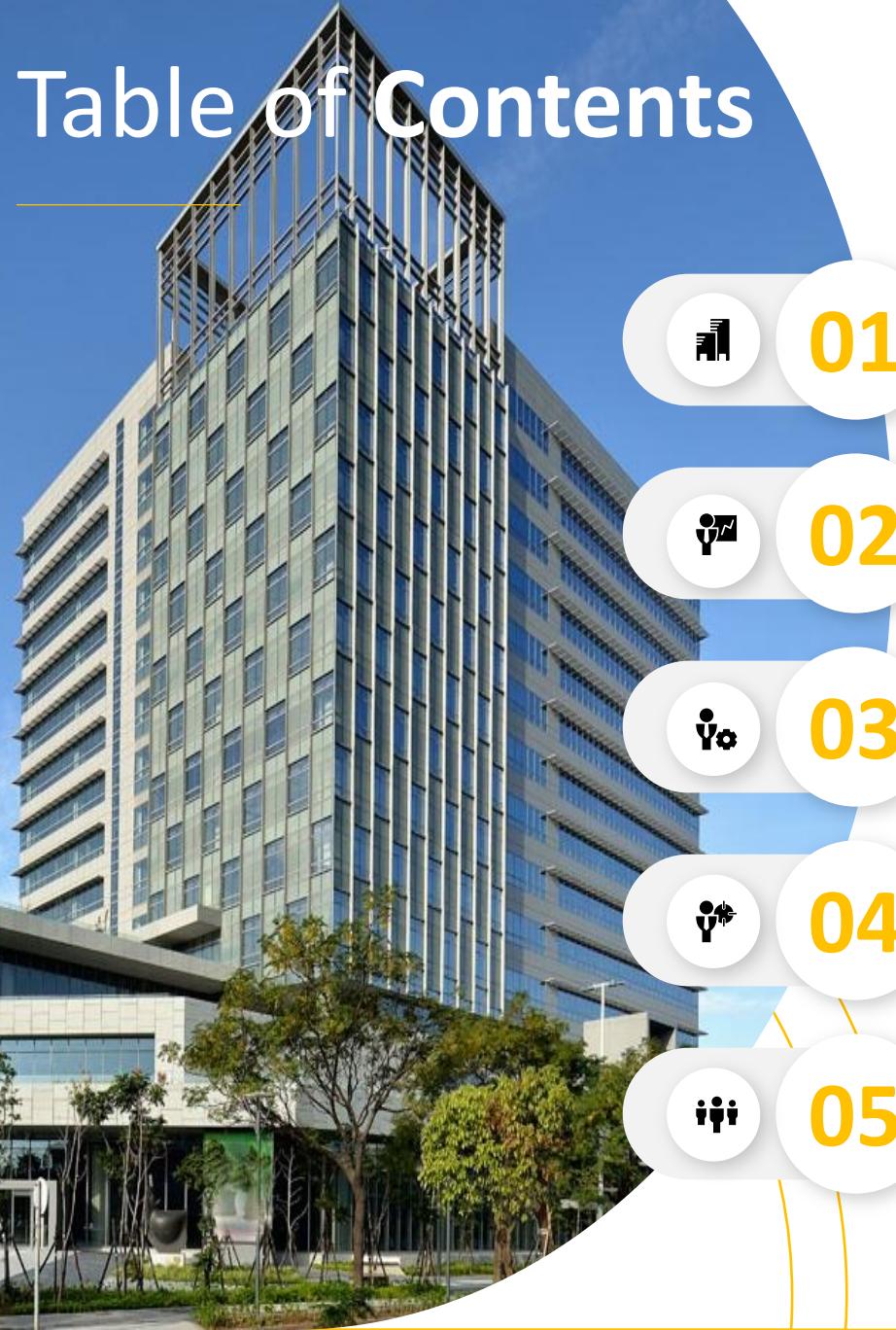
2020/11/09

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

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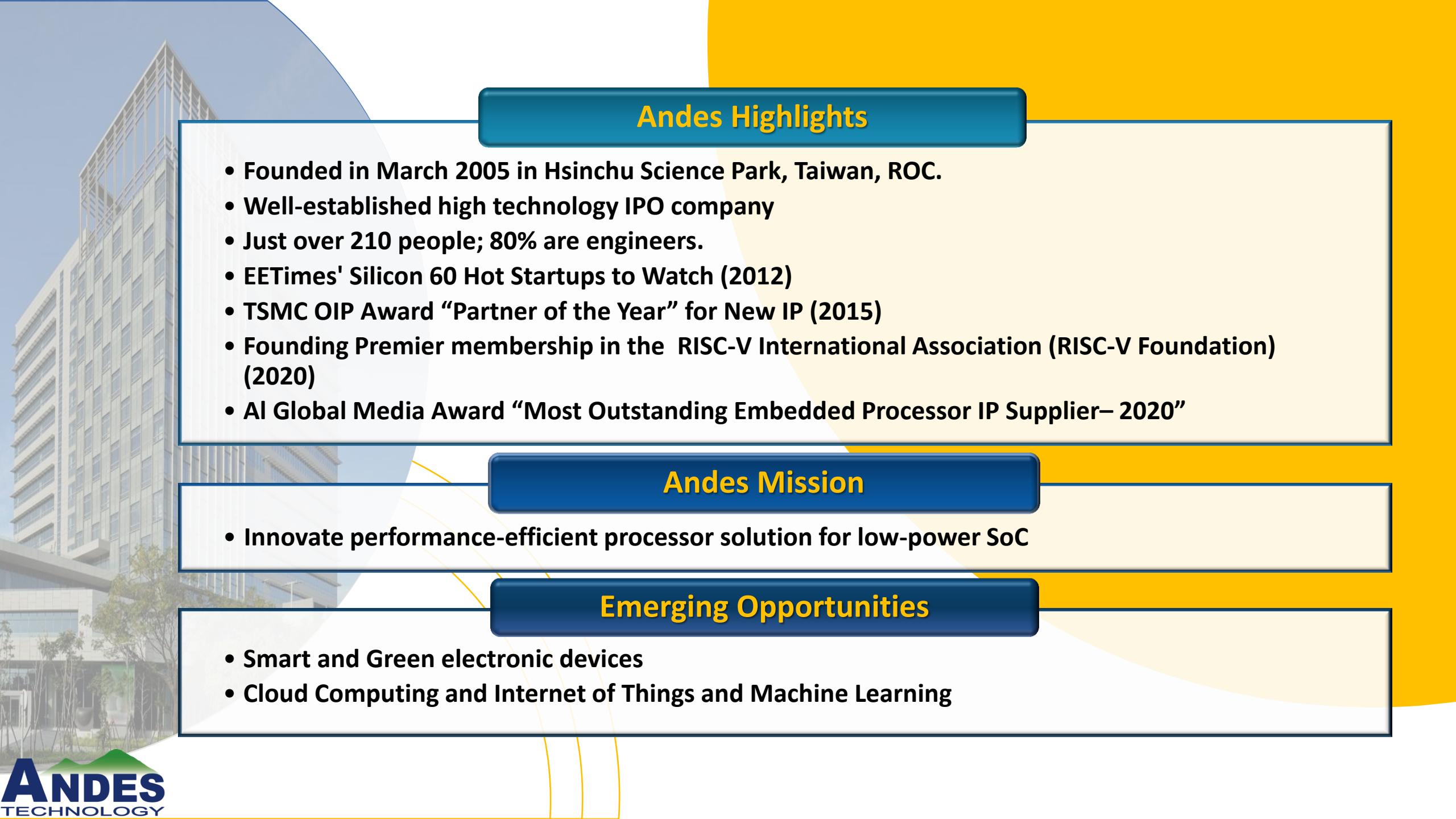
Concluding Remarks



Company Overview

<http://www.andestech.com>





Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Well-established high technology IPO company
- Just over 210 people; 80% are engineers.
- EETimes' Silicon 60 Hot Startups to Watch (2012)
- TSMC OIP Award "Partner of the Year" for New IP (2015)
- Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)
- AI Global Media Award "Most Outstanding Embedded Processor IP Supplier– 2020"

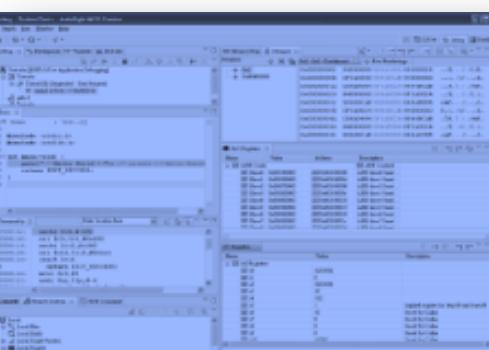
Andes Mission

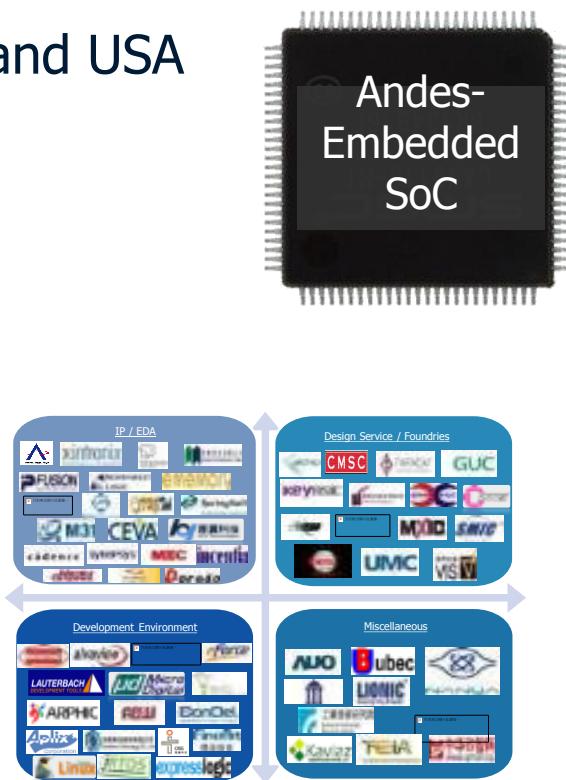
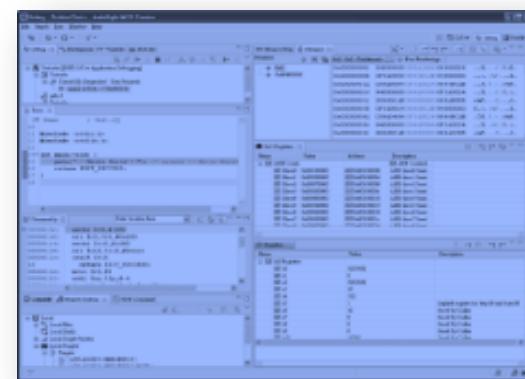
- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing and Internet of Things and Machine Learning

Business Status Overview

- ❖ **200+** commercial licensees
 - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA
 - **400+** license agreements signed
 - ❖ AndeSight™ IDE:
 - **19,000+** installations
 - ❖ Eco-system:
 - **160+** partners
 - ❖ ~**6B** Accumulative SoC Shipped



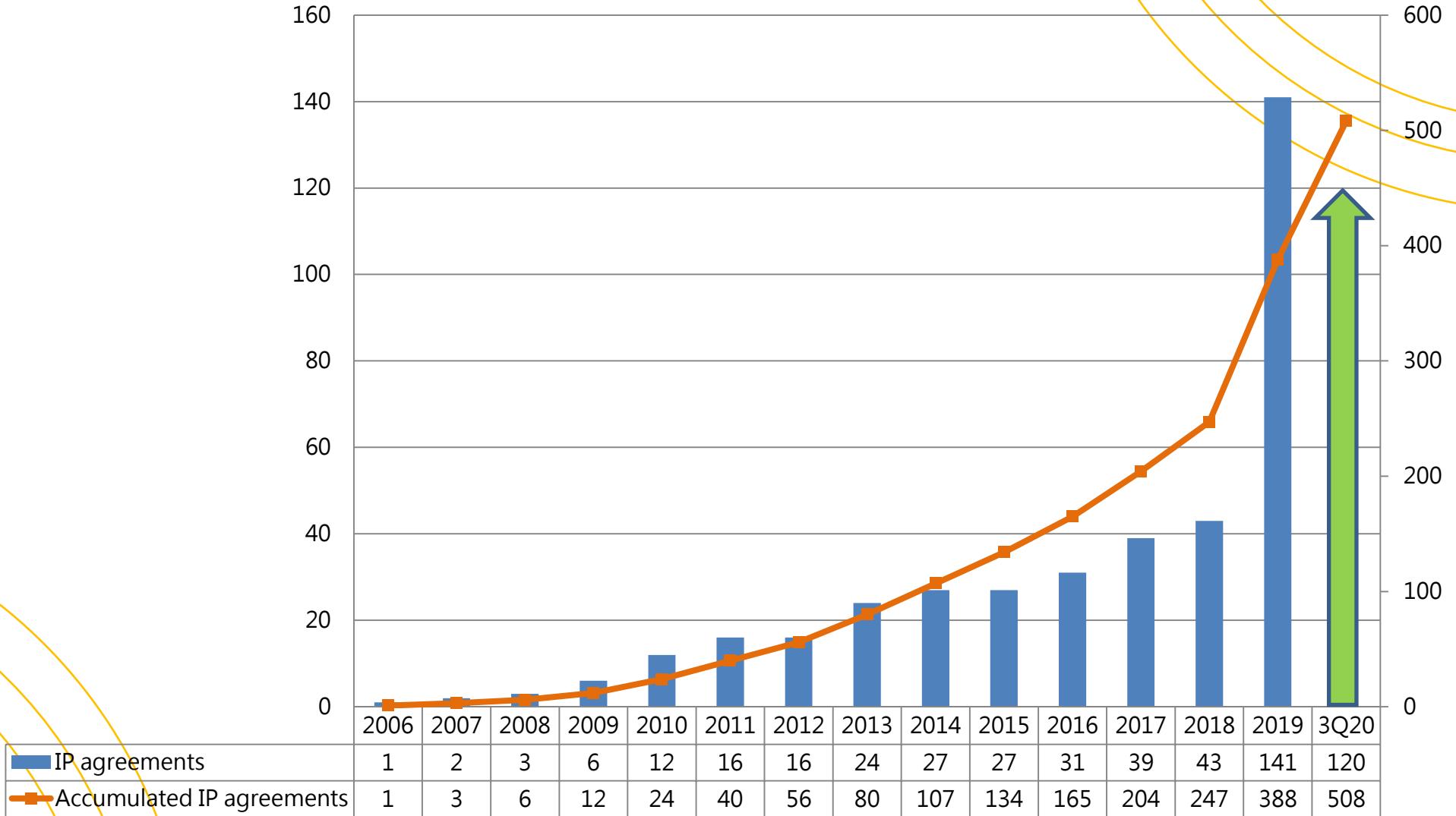


Operation Results

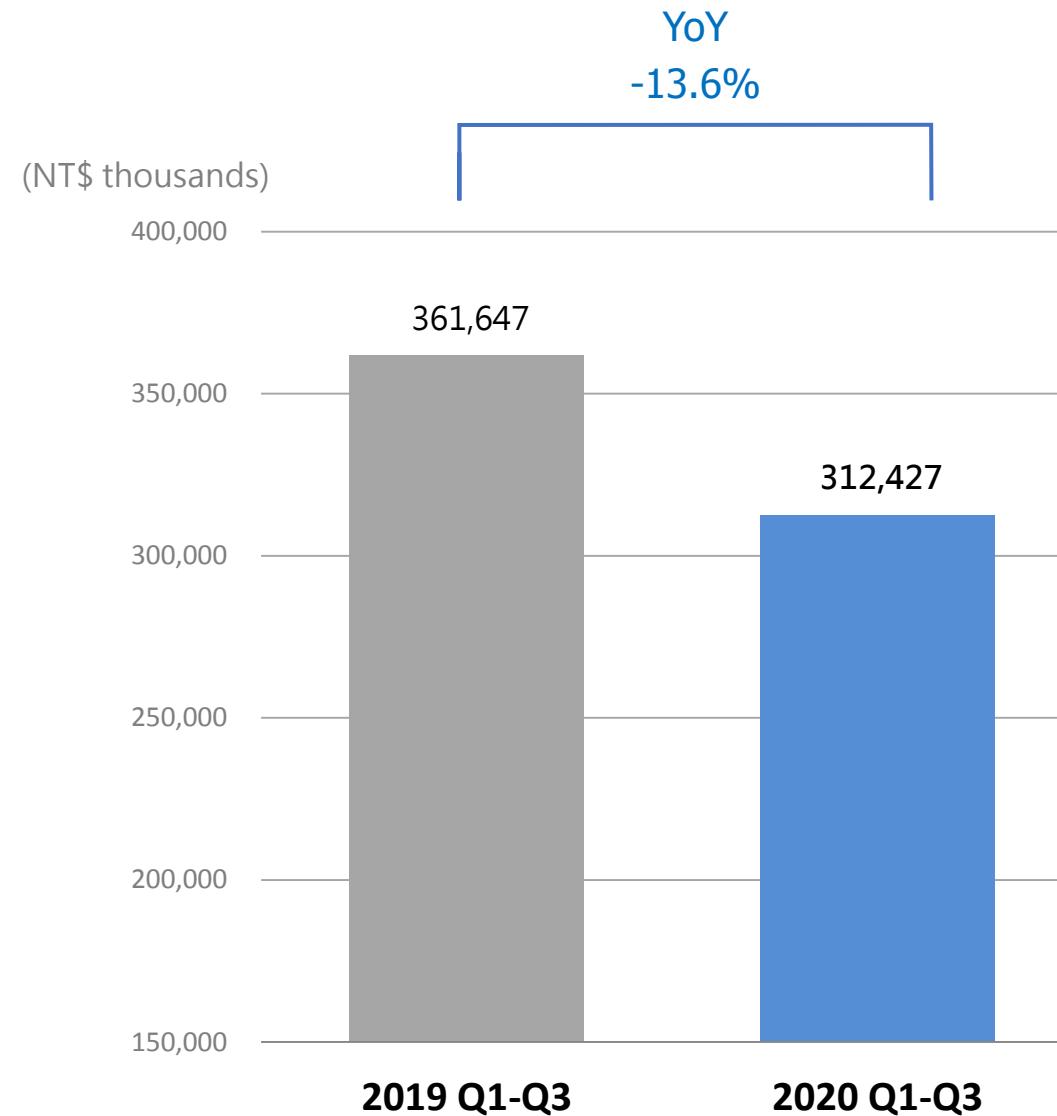
<http://www.andestech.com>



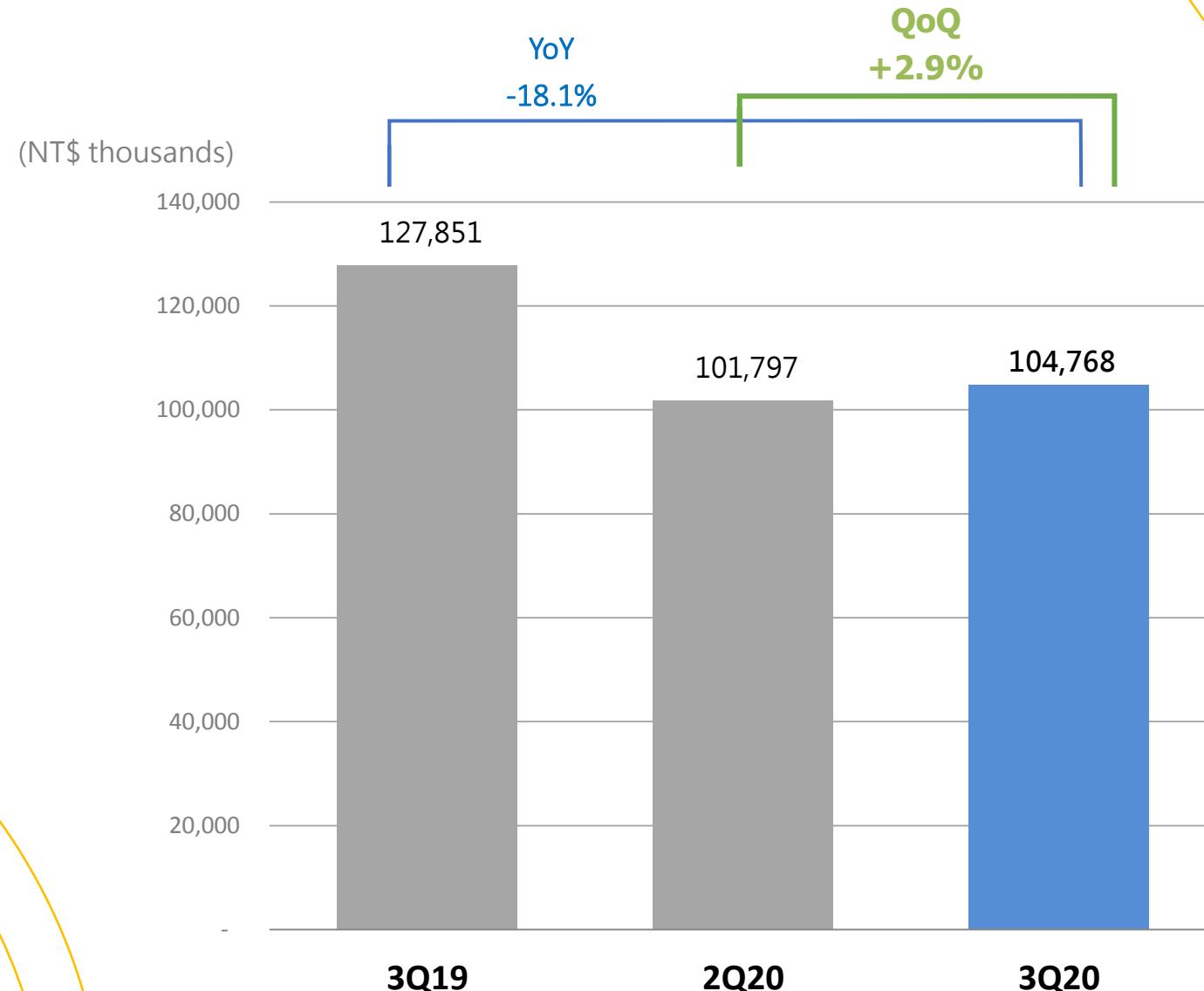
Agreement Growth Analysis



1Q-3Q20 Revenue Analysis



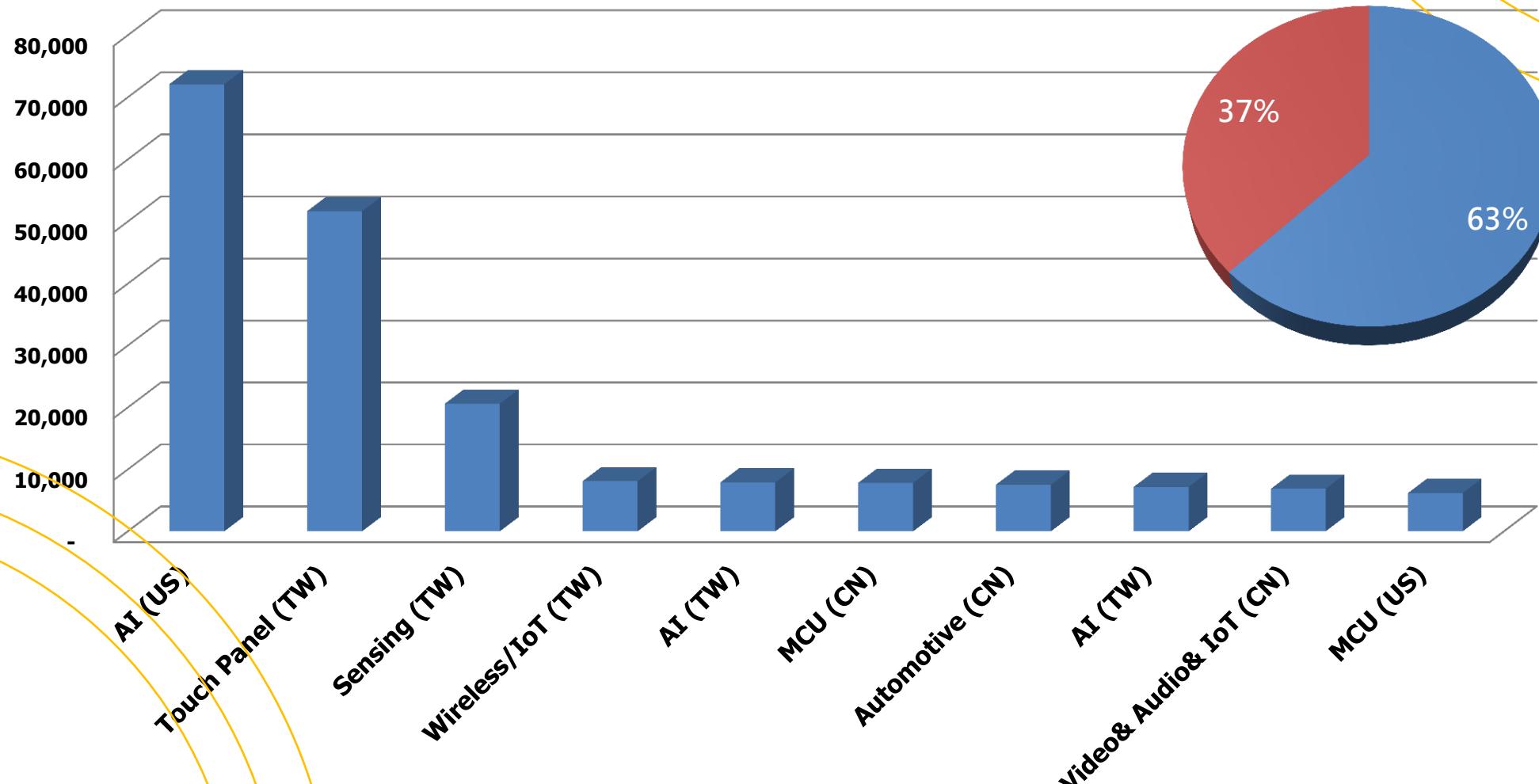
3Q20 Revenue Analysis



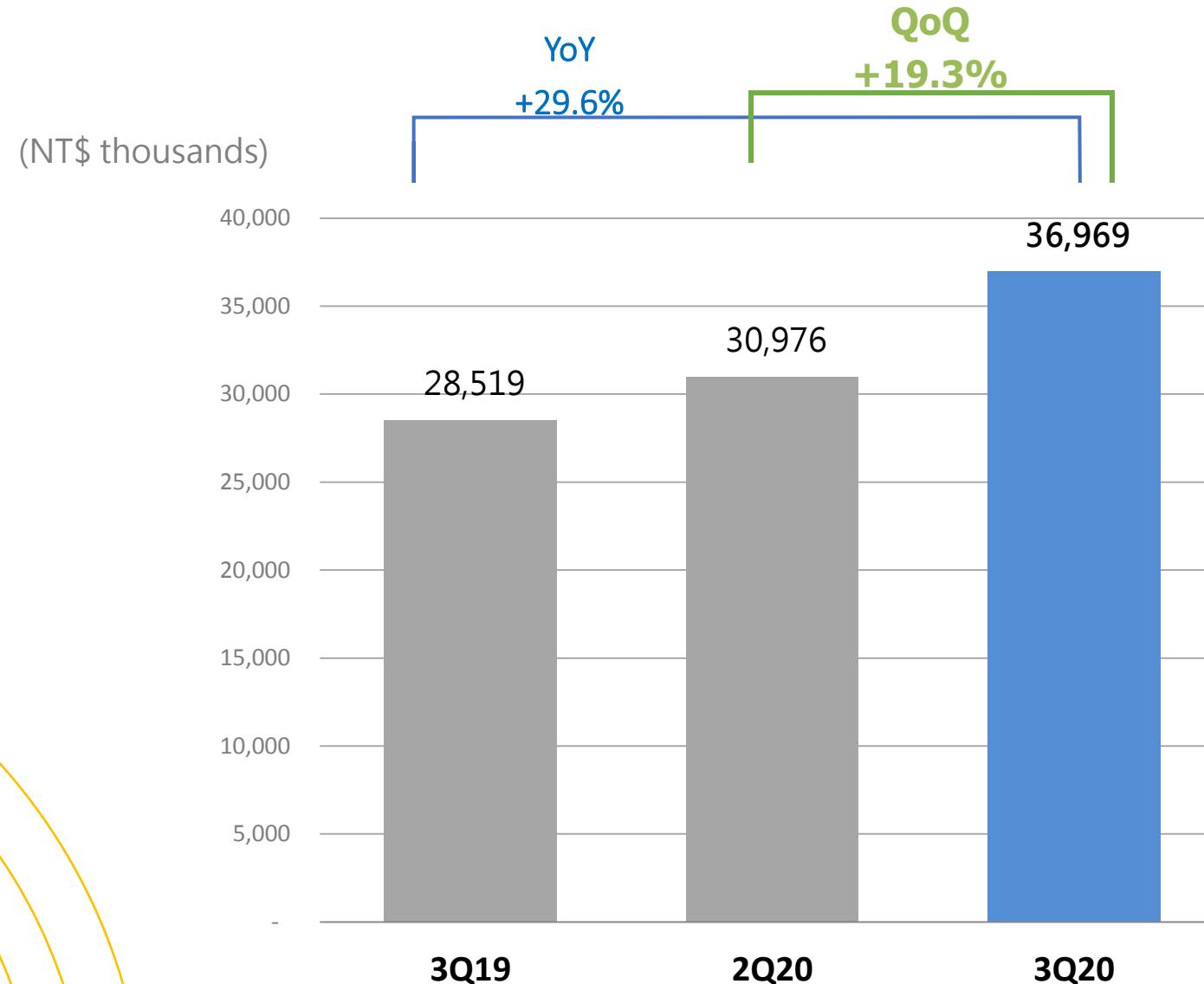
1Q-3Q20 Top 10 Customers Analysis by Revenue

(NT\$ thousands)

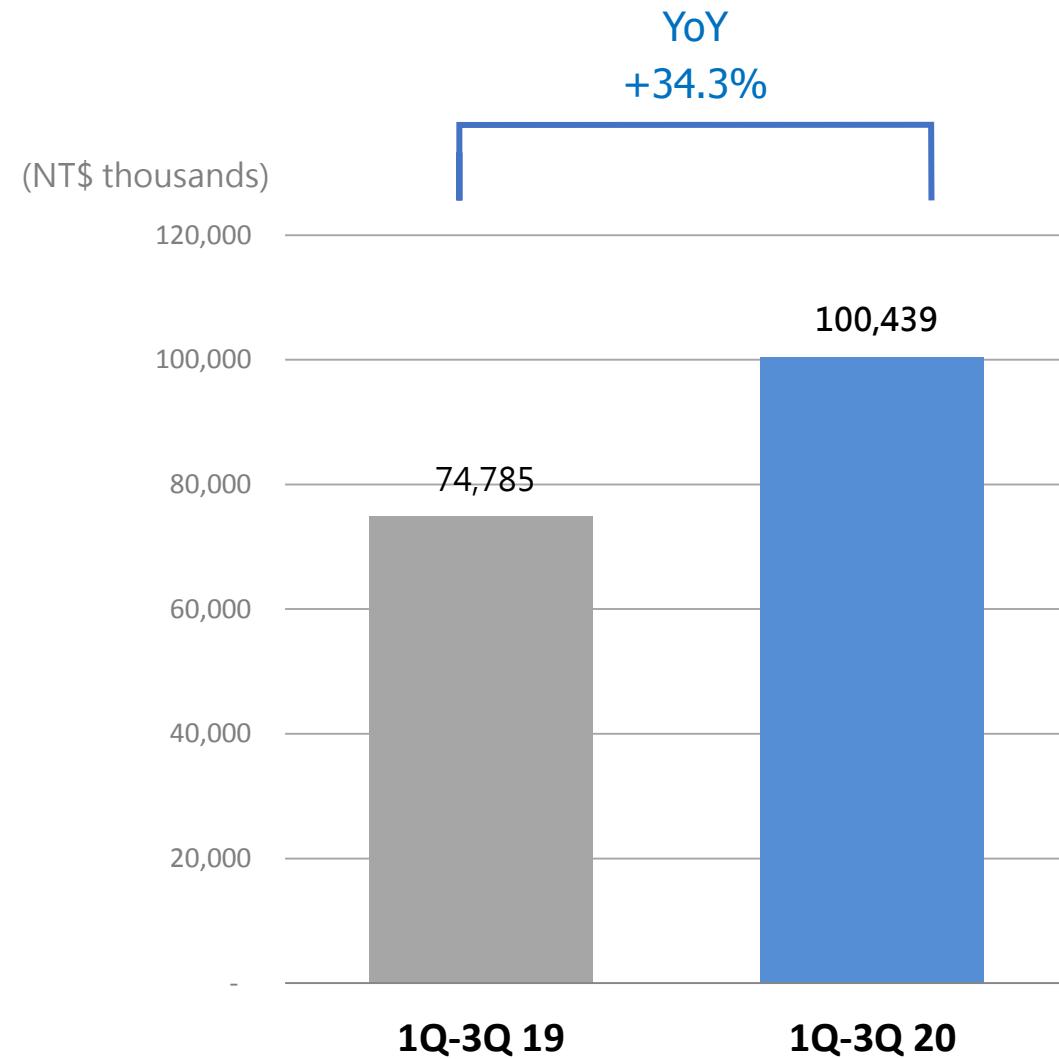
Top 10 Customer Contributed 63% Revenue



3Q20 Royalty Analysis

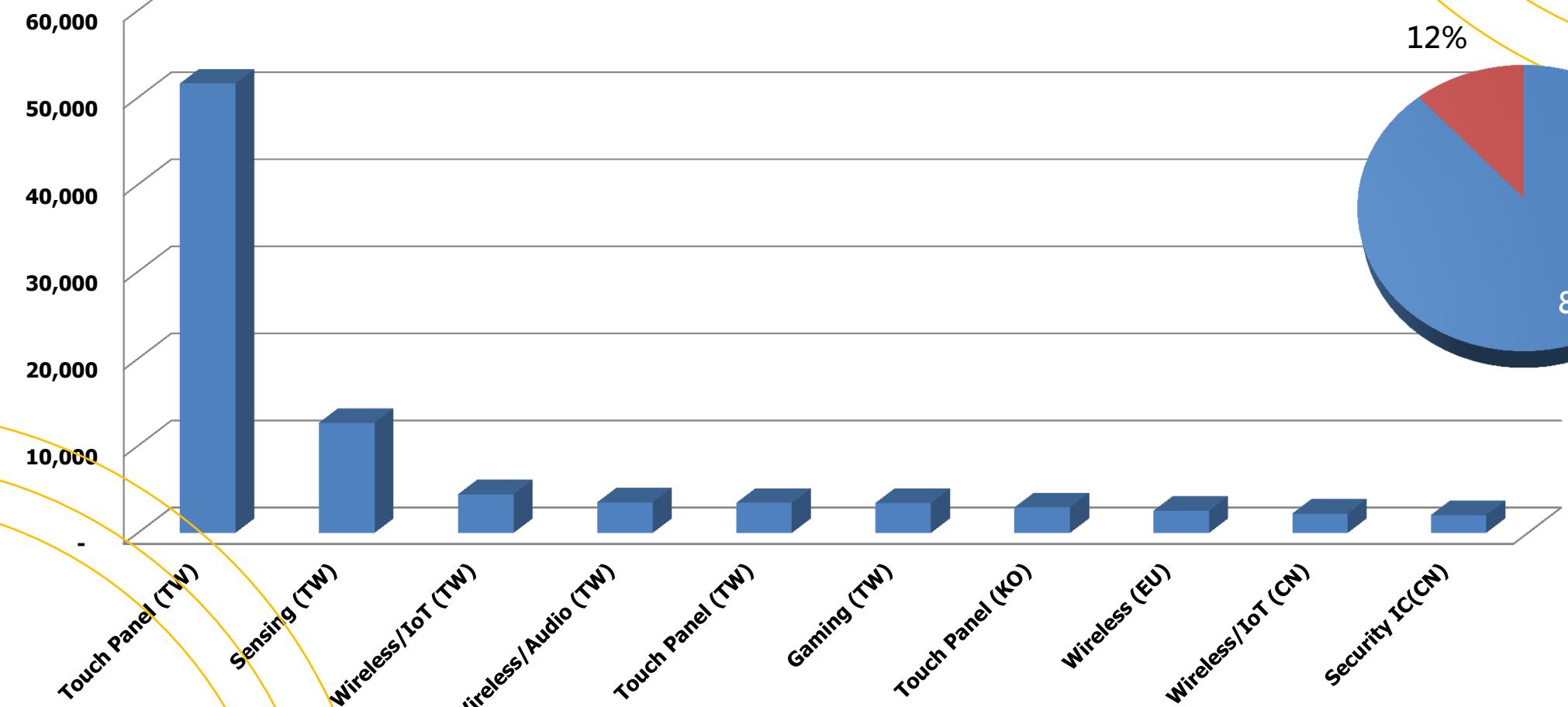


1Q-3Q20 Royalty Analysis



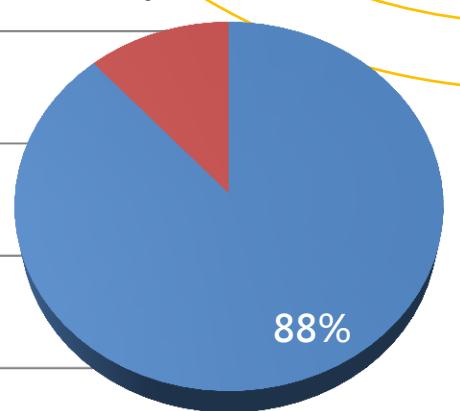
1Q-3Q20 Top Ten Royalty Contributors Analysis by Application

(NT\$ thousands)

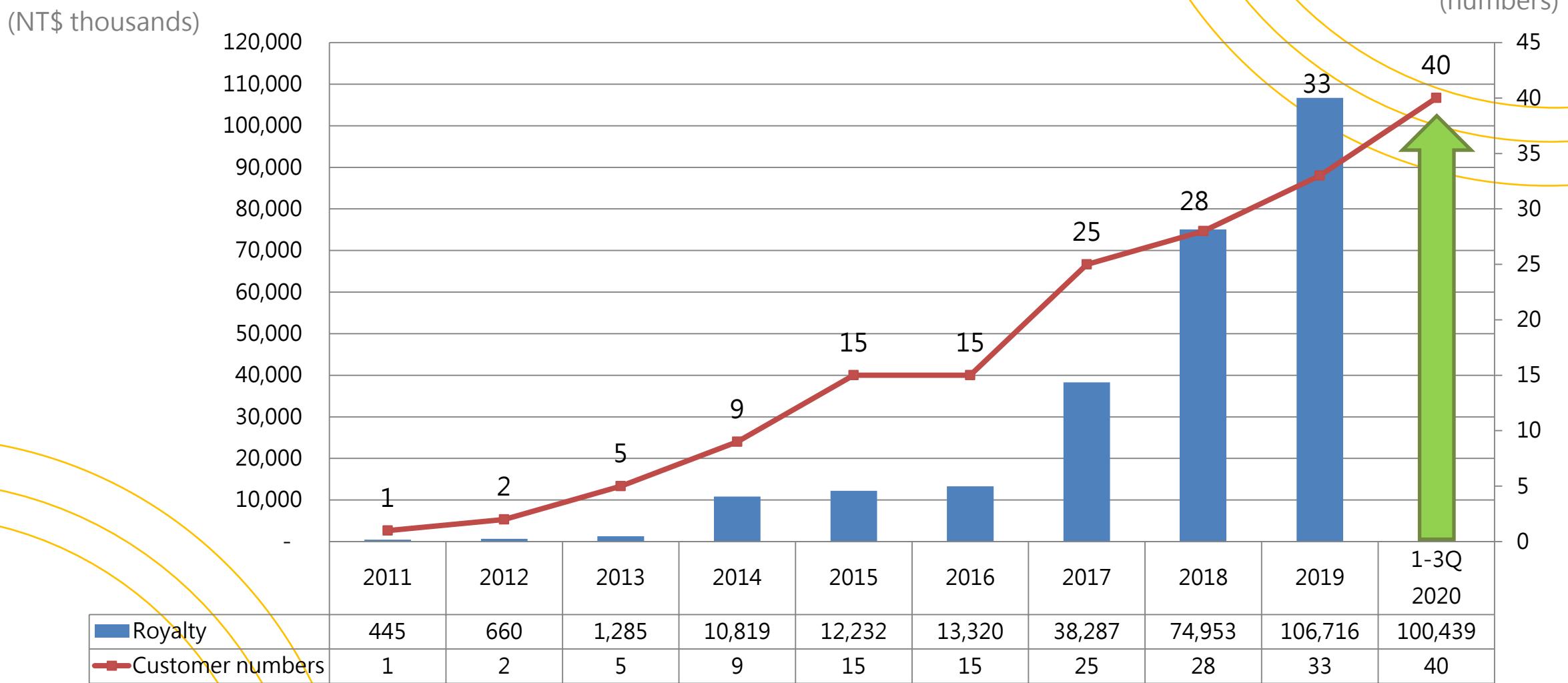


Top 10 Royalty Customers
Contributed 88% Royalty

12%

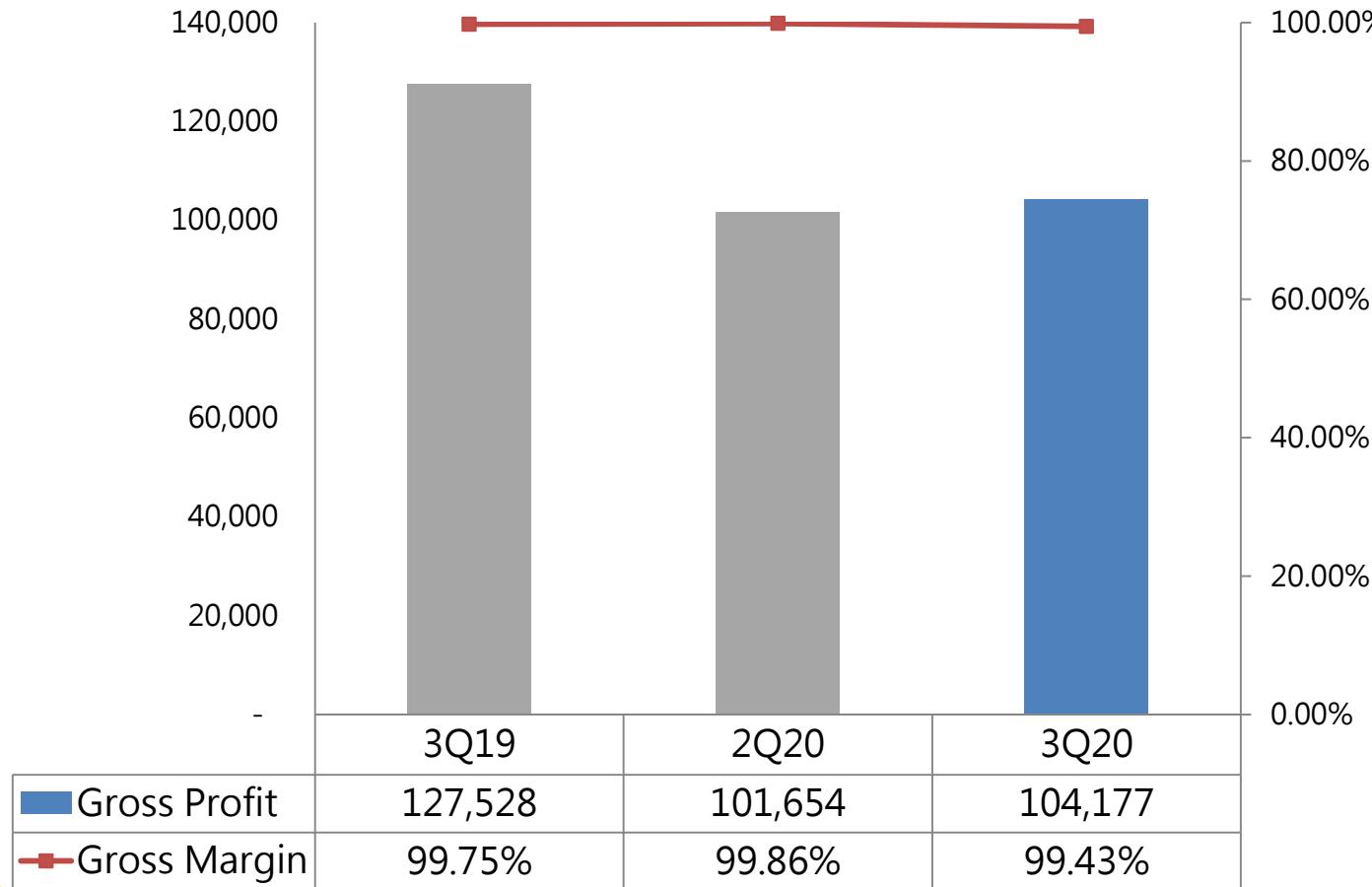


Royalty Analysis

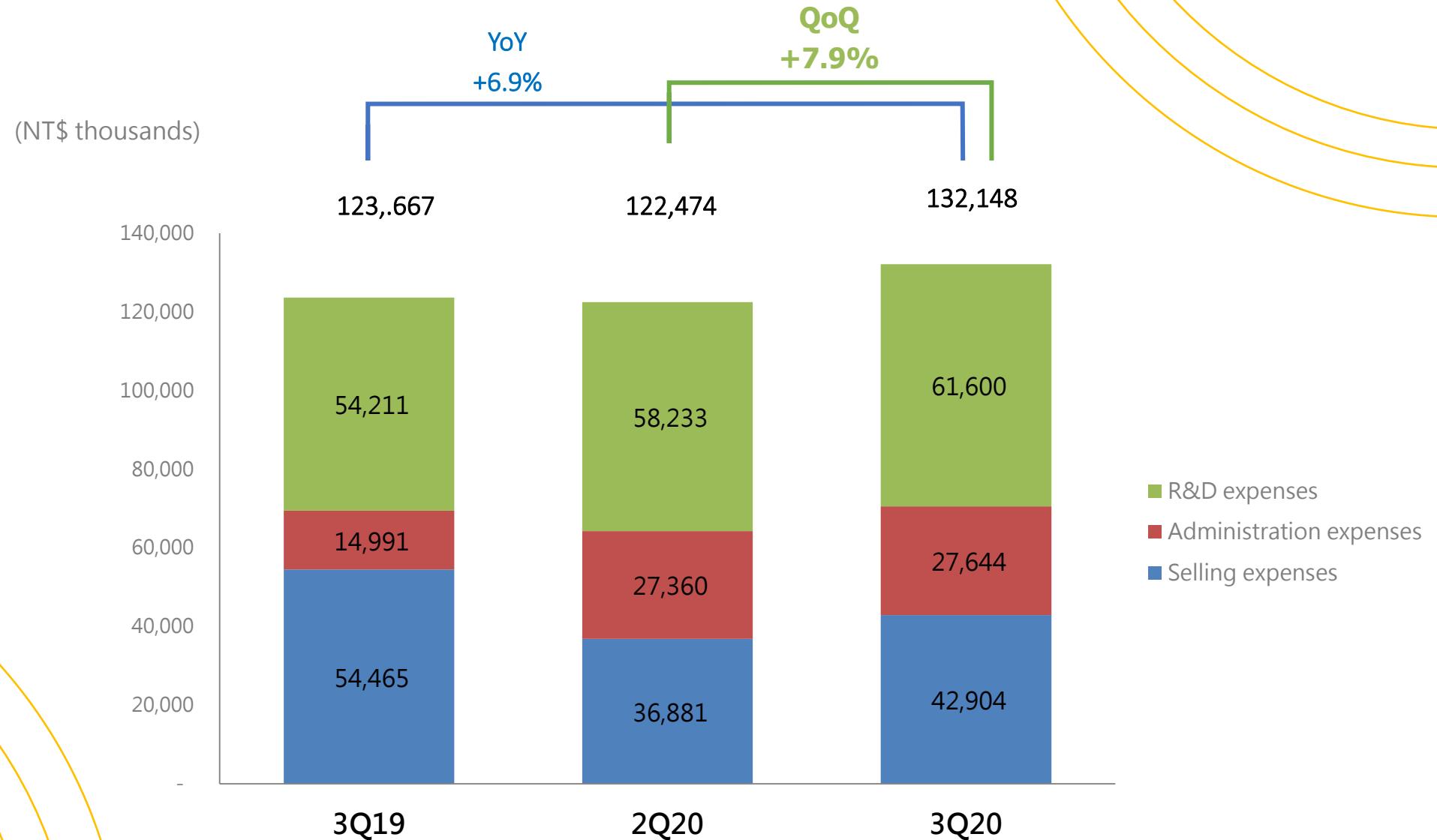


Consolidated Gross Margin

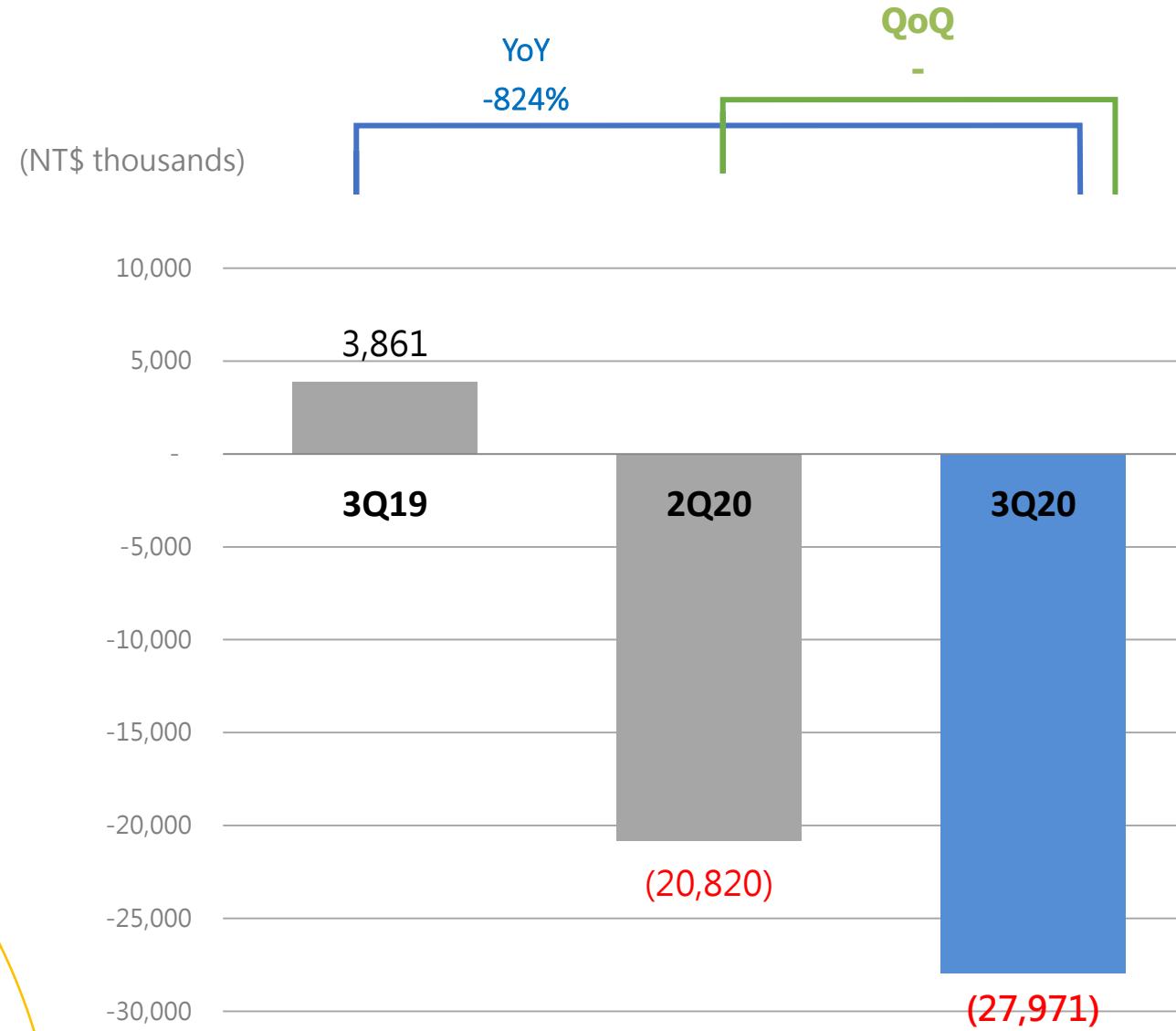
(NT\$ thousands)



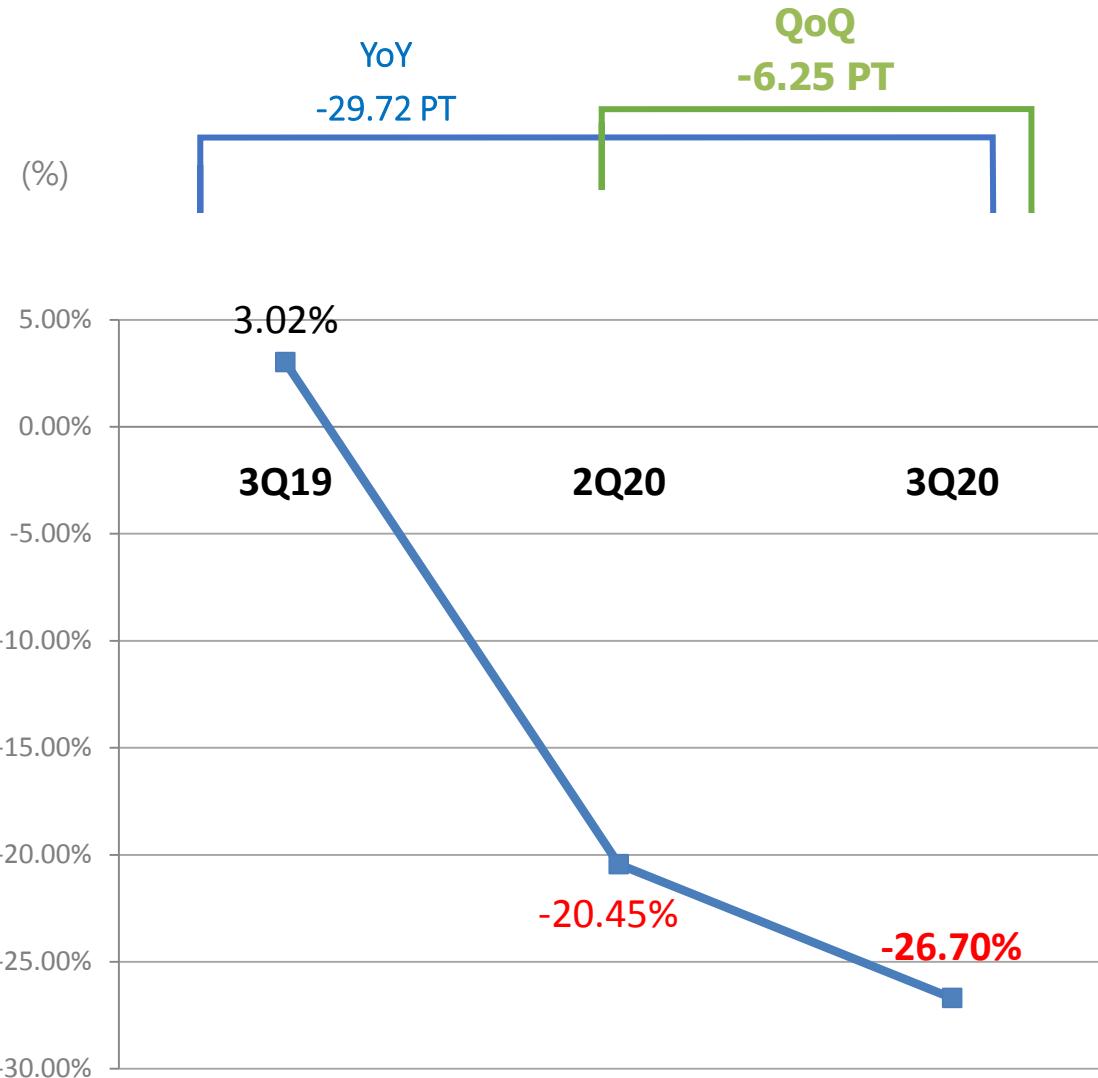
Consolidated Operating Expenses



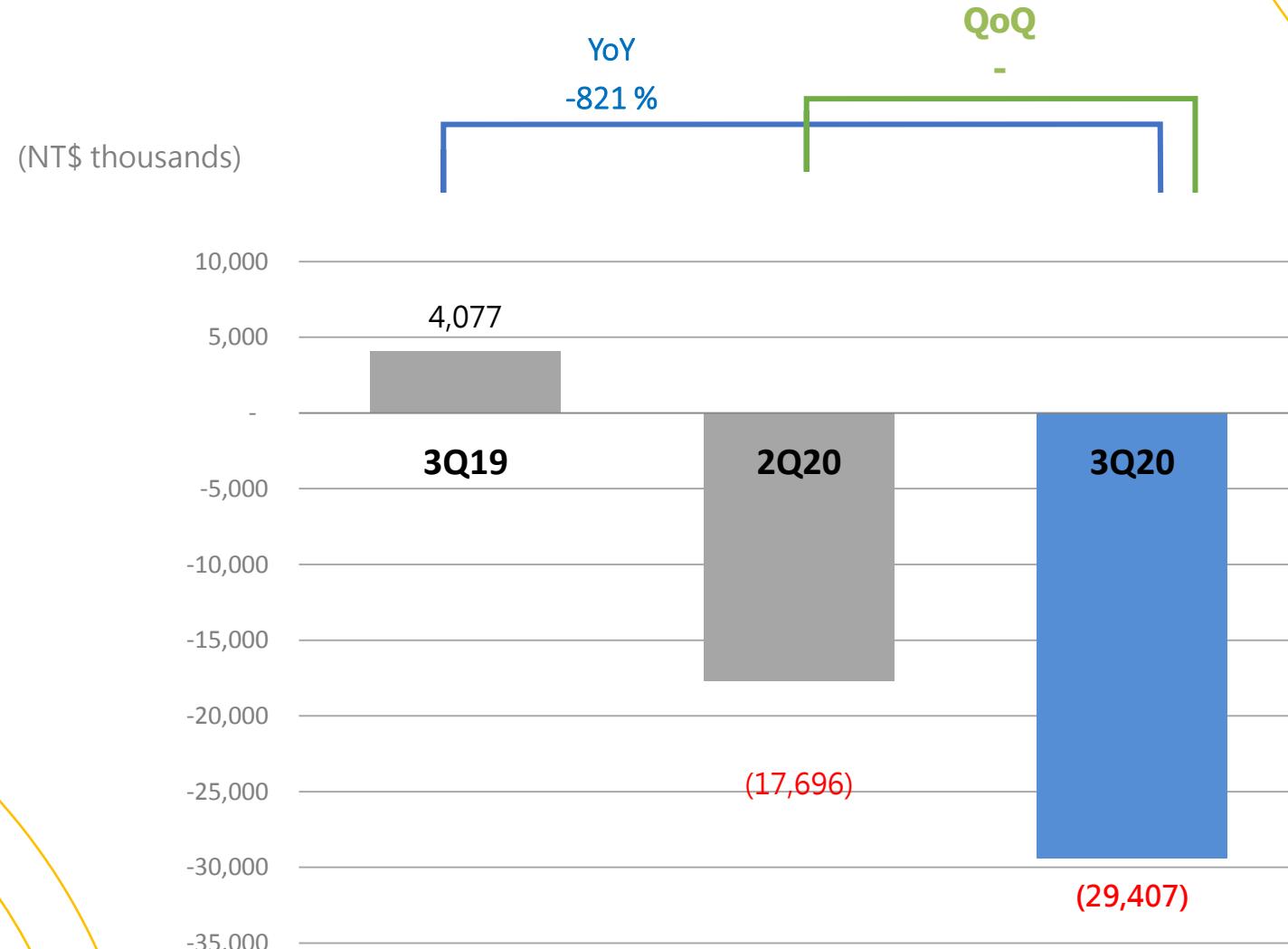
Consolidated Operating Income (Loss)



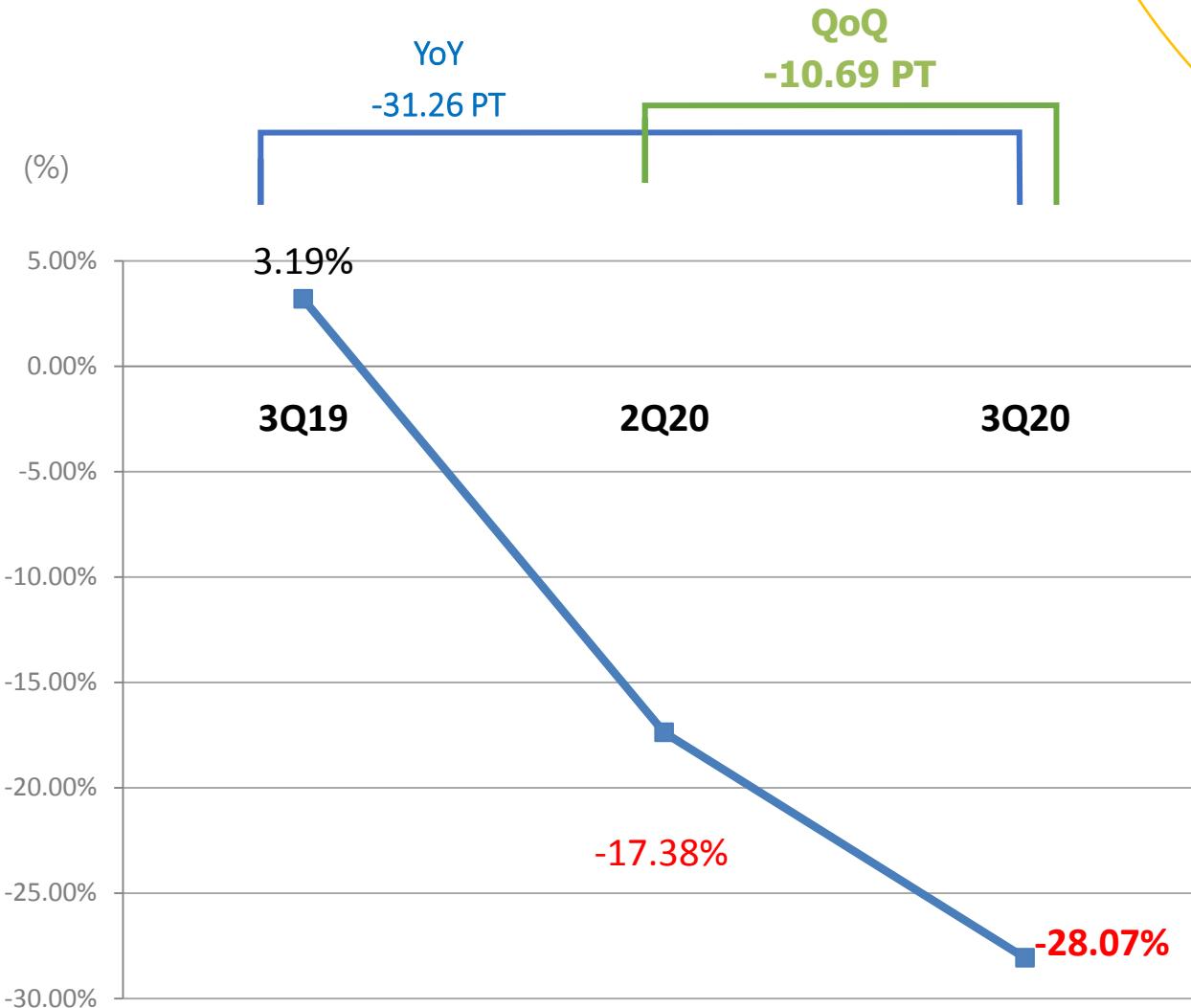
Consolidated Operating Margin



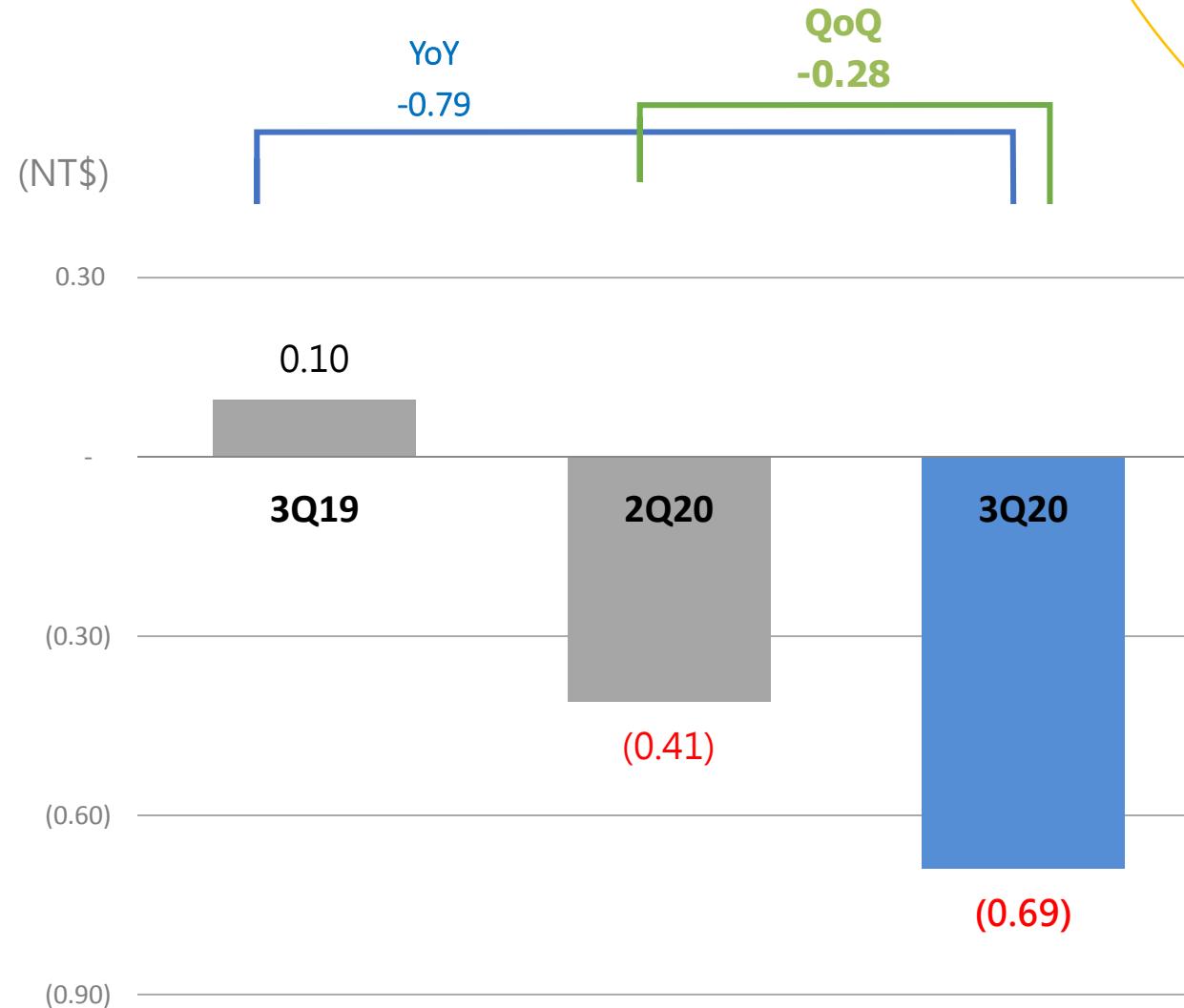
Consolidated Net Income (Loss)



Consolidated Net Profit Margin

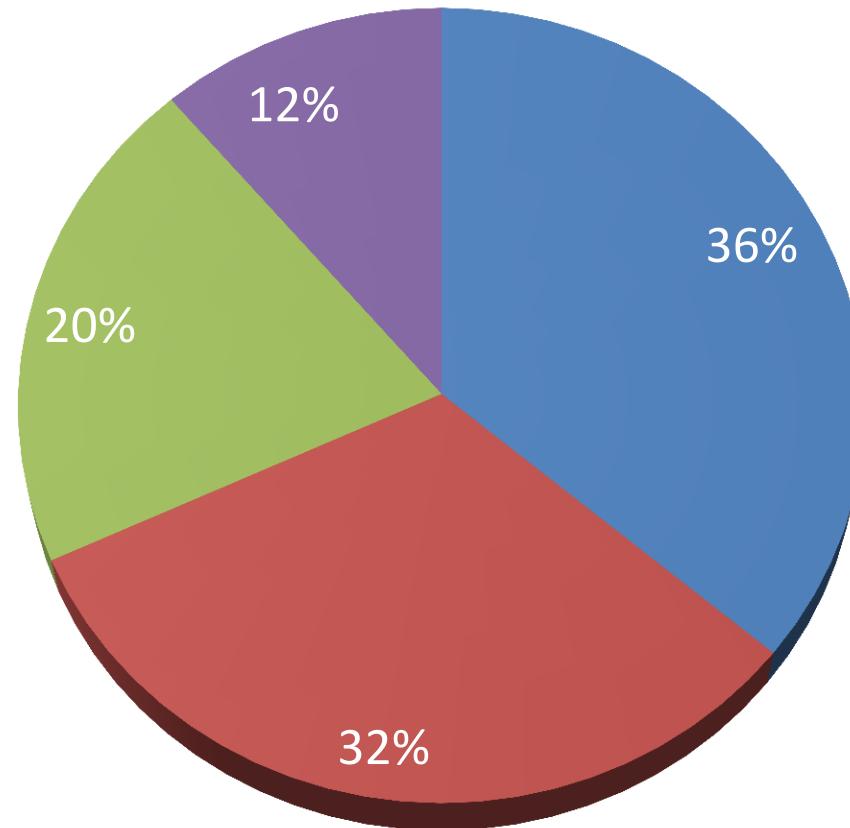


Consolidated Earnings Per Share



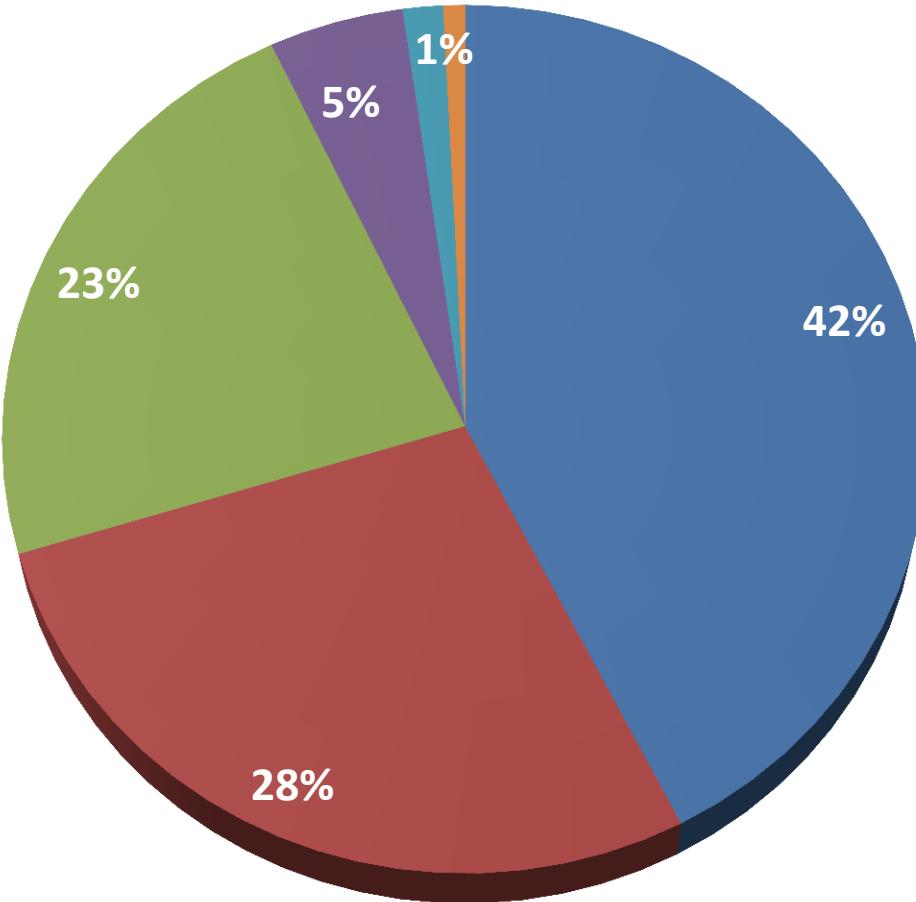
1Q-3Q20 Revenue Analysis by Payment Model

■ License Fee ■ Running Royalty ■ Custom Computing Service ■ Maintenance & Others

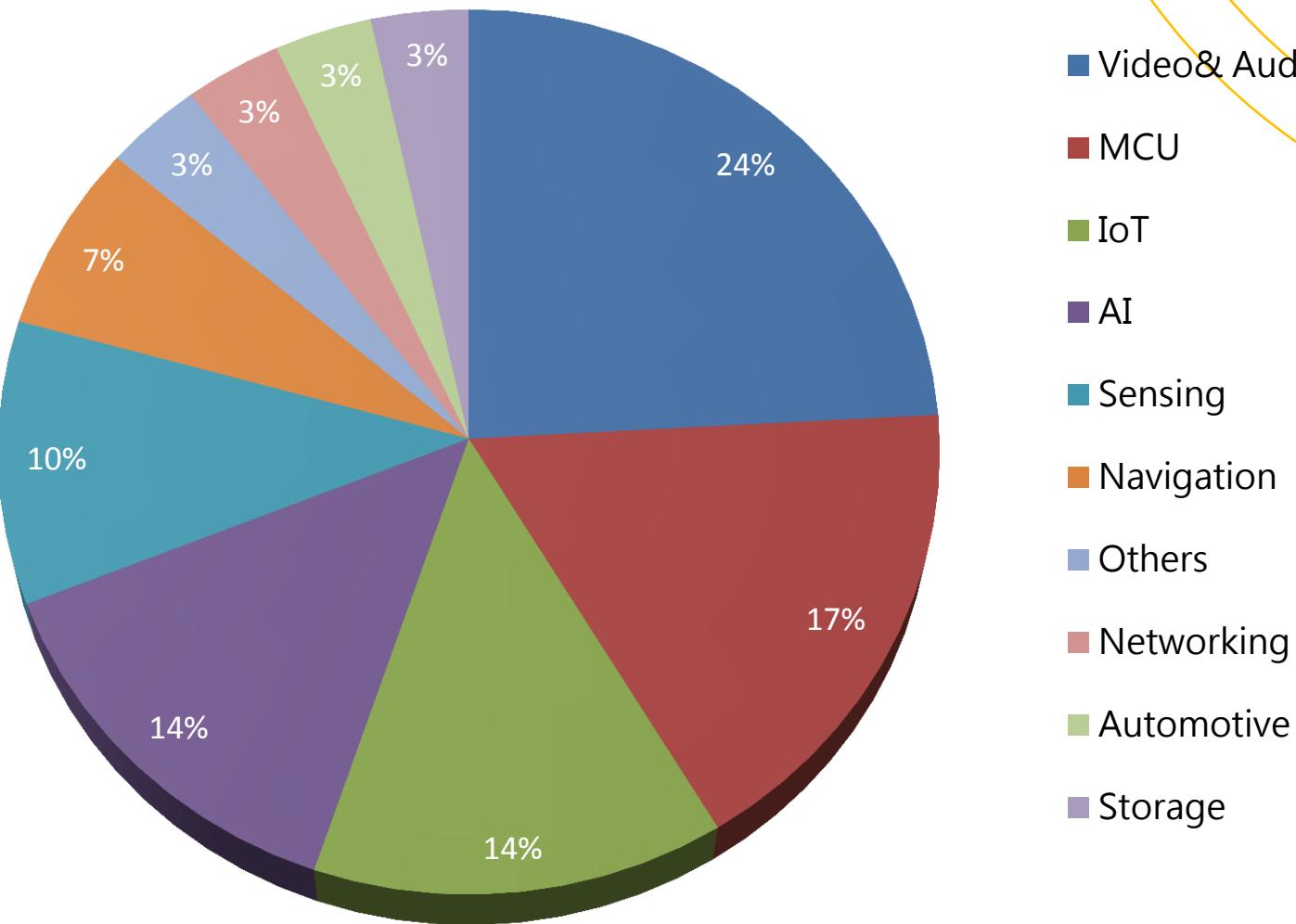


1Q-3Q20 Revenue Analysis by Region

Taiwan USA China Korea Europe Japan

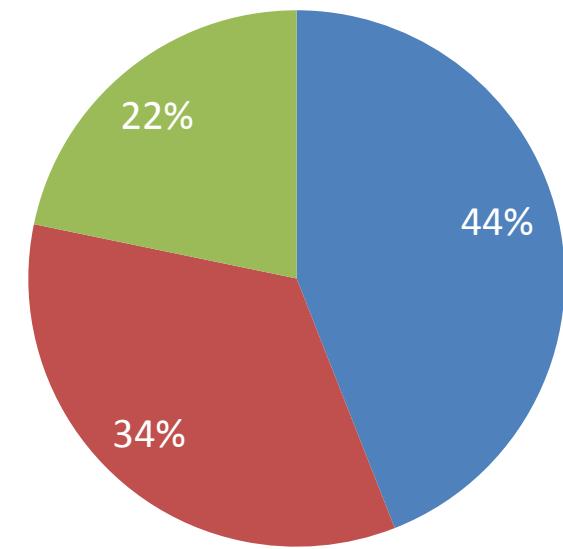


1Q-3Q20 Customer Application Analysis

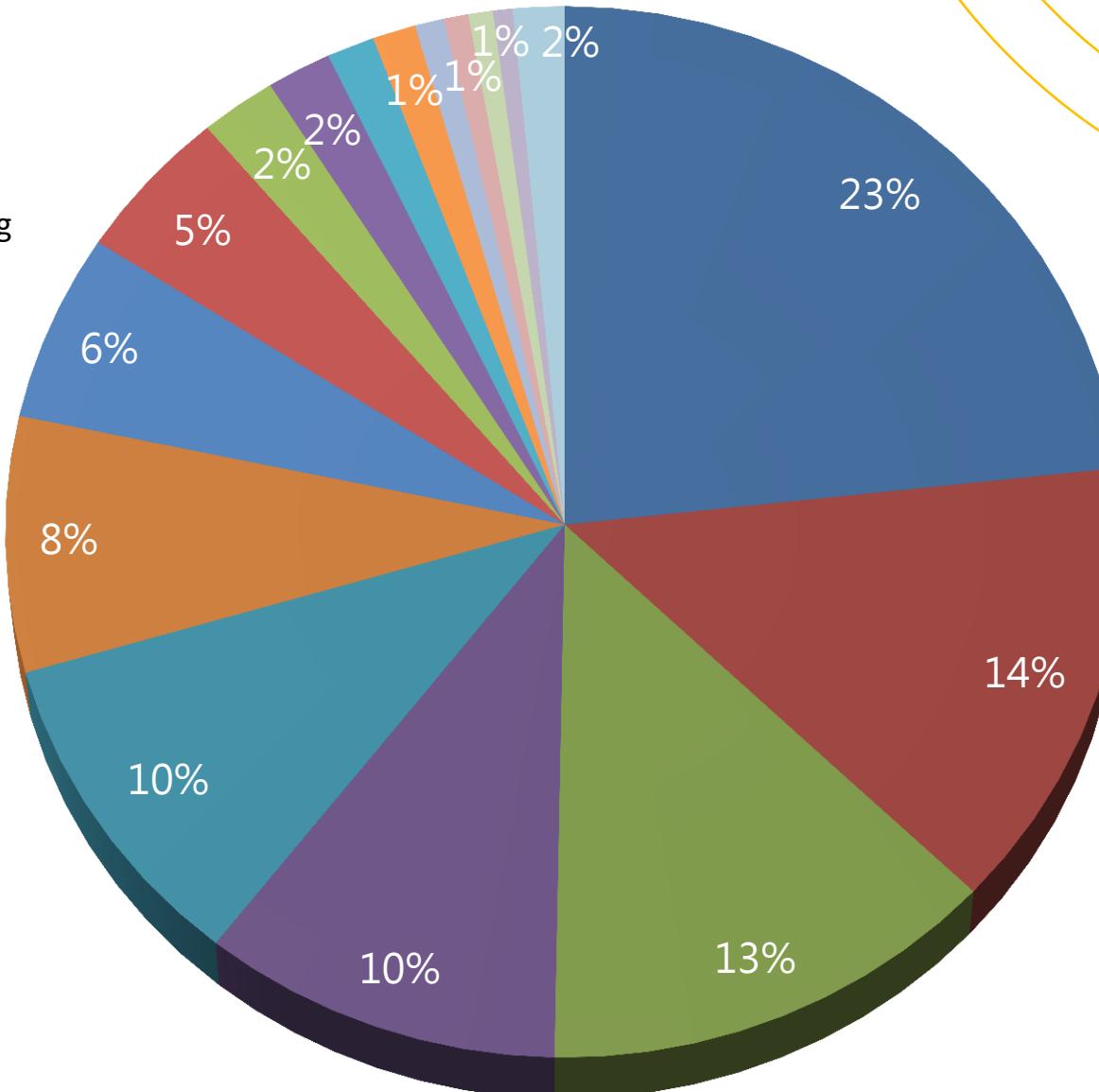


*Based on agreement number

1Q-3Q20 Revenue Analysis by Product

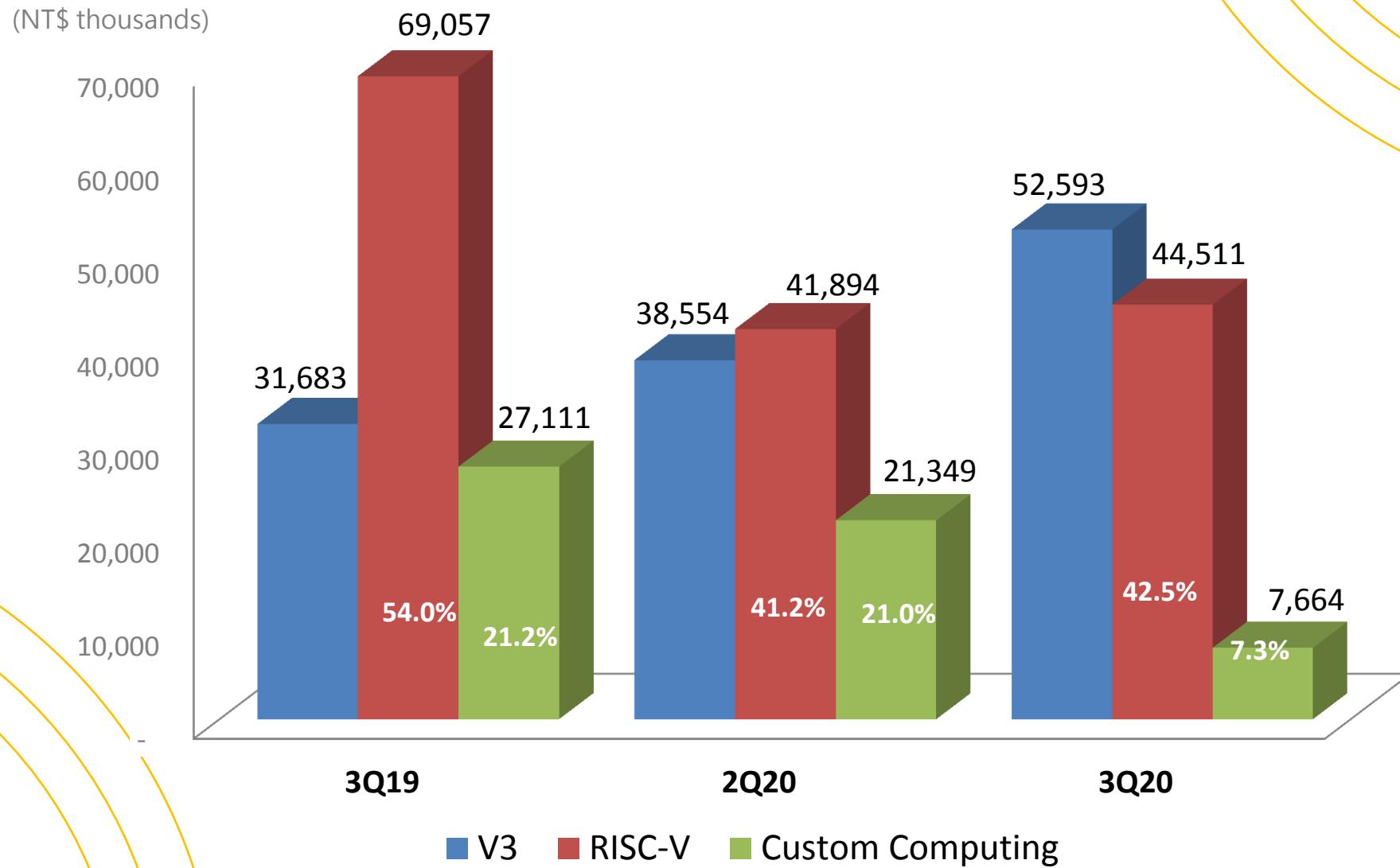


■ V3
■ RISC-V
■ Custom Computing



■ N8
■ Customized IP
■ D25
■ N9
■ N25
■ Service
■ D10
■ AX25
■ N10
■ N22
■ NX25
■ N13
■ N7
■ ACE
■ AndeSight
■ EVB
■ OTHERS

3Q20 Revenue Analysis - RISC-V





Product Applications

<http://www.andestech.com>



Andes Updates

- ❖ A 15-year-old public CPU IP company
- ❖ 1.5B+ Andes-Embedded SoC annually in 2019



- ❖ A **founding premier** member of the RISC-V International
- ❖ An active role in RISC-V International & its extension task groups
 - RISC-V Board Director
 - Vice Chair of Technical Steering Committee
 - RISC-V Ambassador
 - Chair of P-extension (Packed DSP/SIMD) Task Group
 - Co-chair of Fast Interrupt Task Group
- ❖ A major open source maintainer/contributor

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only supports rv64i-based ISAs
- newlib: August, 2017
- "Probably not a compiler bug"

GNU Toolchains

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM/SM
 - Talk yesterday afternoon
 - Poster on Tuesday night
- RV32IM(A)FI support upstream
 - Missing hard-float calling convention
 - Missing 64-bit support
 - Missing compressed support
- Clang, Go, and OpenJDK have run code
 - Build port in progress
 - Poster on Tuesday

LLVM

RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64i-based systems
 - Drivers are trickling in now

Berkeley

SiFive

ANDES TECHNOLOGY

Linux

Andes Embedded in Various Applications



Smart Speakers:
WiFi IoT



Bike Sharing:
GPS Ctrl



X-Trail:
ADAS Ctrl



Switch:
Game Flash Ctrl

- ❖ In leading **machine learning computers** for datacenter
- ❖ In tier-one **switch routers** for datacenter
- ❖ Recent applications: **5G networking, 802.11ax, AI processors** (using Andes Custom Extension, ACE)

V5 Adoptions: From MCU to Datacenters

❖ Edge to Cloud

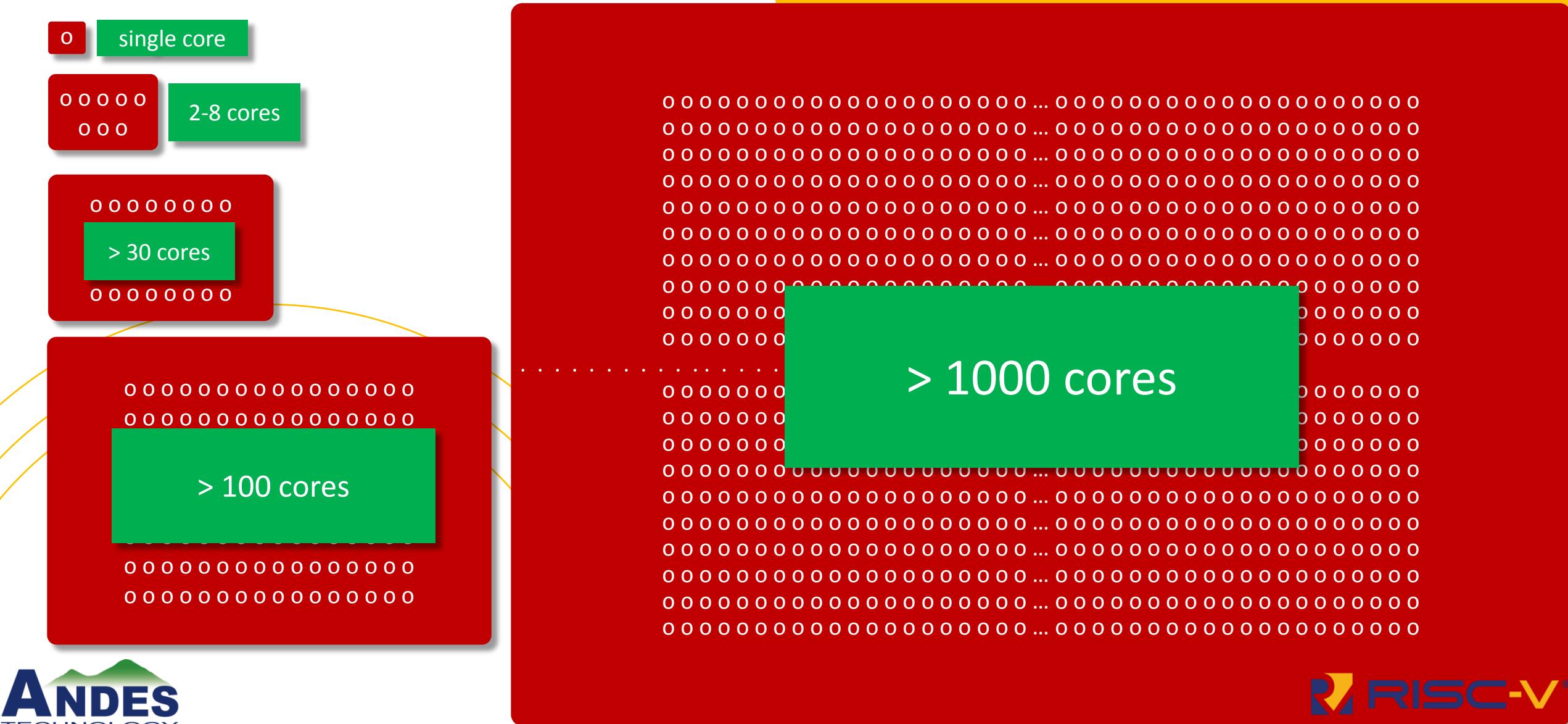
- ADAS
- AIoT
- Blockchain
- FPGA
- MCU
- Multimedia
- Security
- Wireless (BT/WiFi)
- Datacenter AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

❖ 40nm to 7nm

❖ Many in AI



Andes RISC-V Cores Adopted in SoC



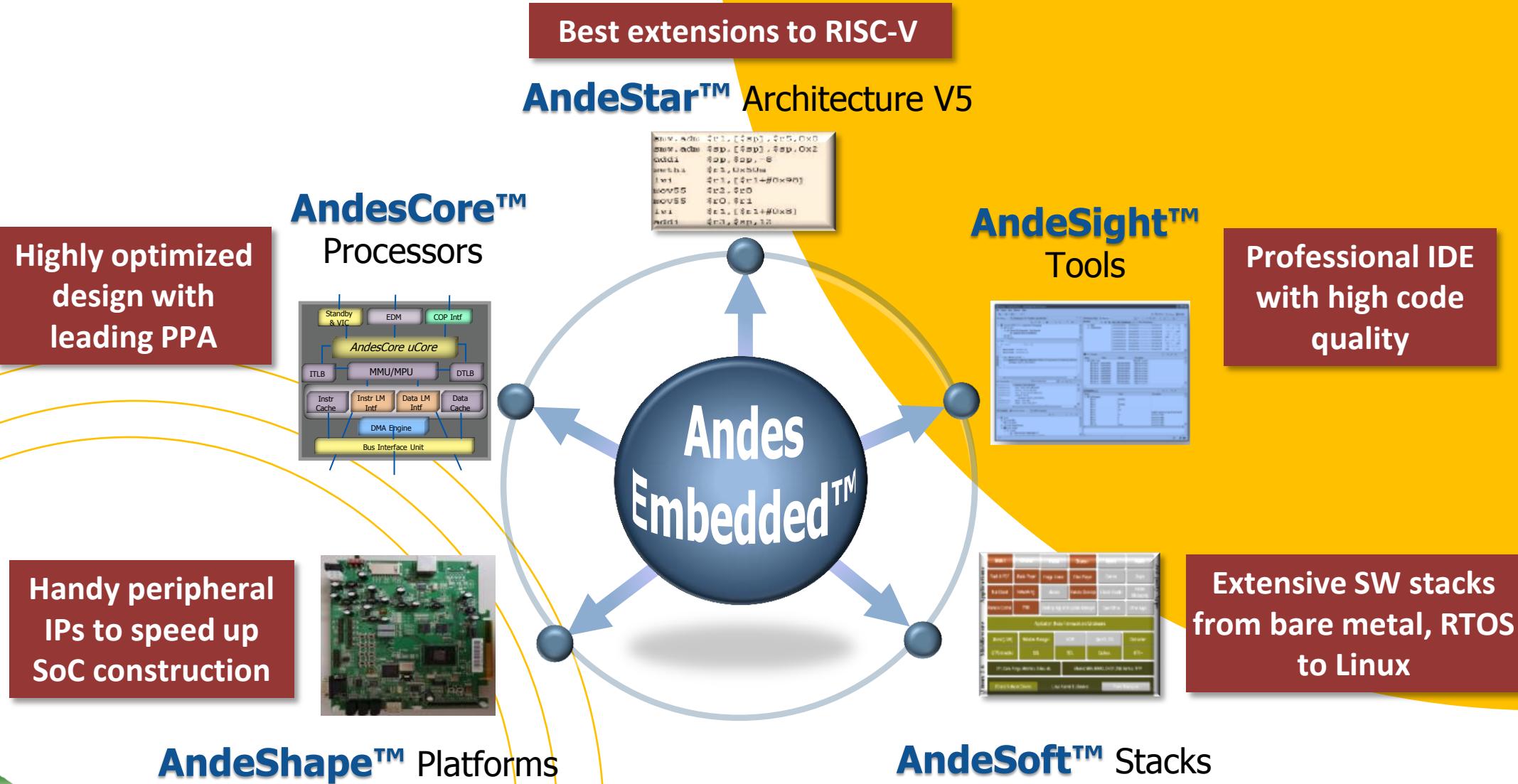


New Products and Ecosystems

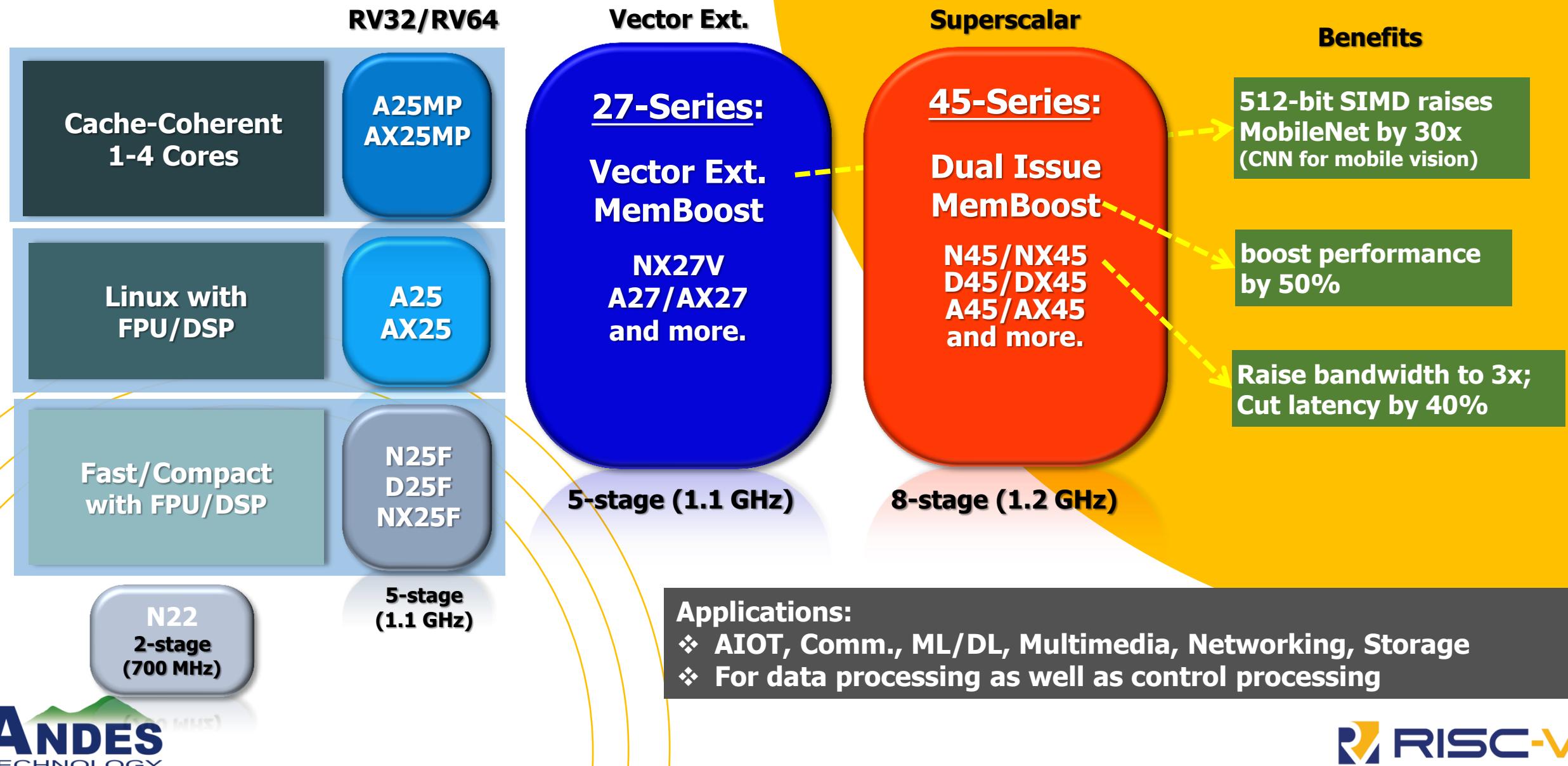
<http://www.andestech.com>



Andes RISC-V Product Overview



Andes RISC-V Product Roadmap



Andes V5 Architecture for All Levels of Computing

AndeStar™ V5 CPUs



RV32/64



Andes Extension

N/D-series

N22 N(X)25 D25...

A-series

A(X)25 A(X)27 A(X)45
Multicore...

Vector

NX27V, NX45V...

Conventional Computing Architecture

Leading PPA Embedded Processor

IoT, Sensing, Storage, Audio, GPS

High Performance and Power Efficient AP

5G, AI, Datacenter, Video Surveillance, Networking

Cray Style, Scalable Vector Processor

Datacenter, Server, Deep Learning

Domain Specific Architecture (DSA)



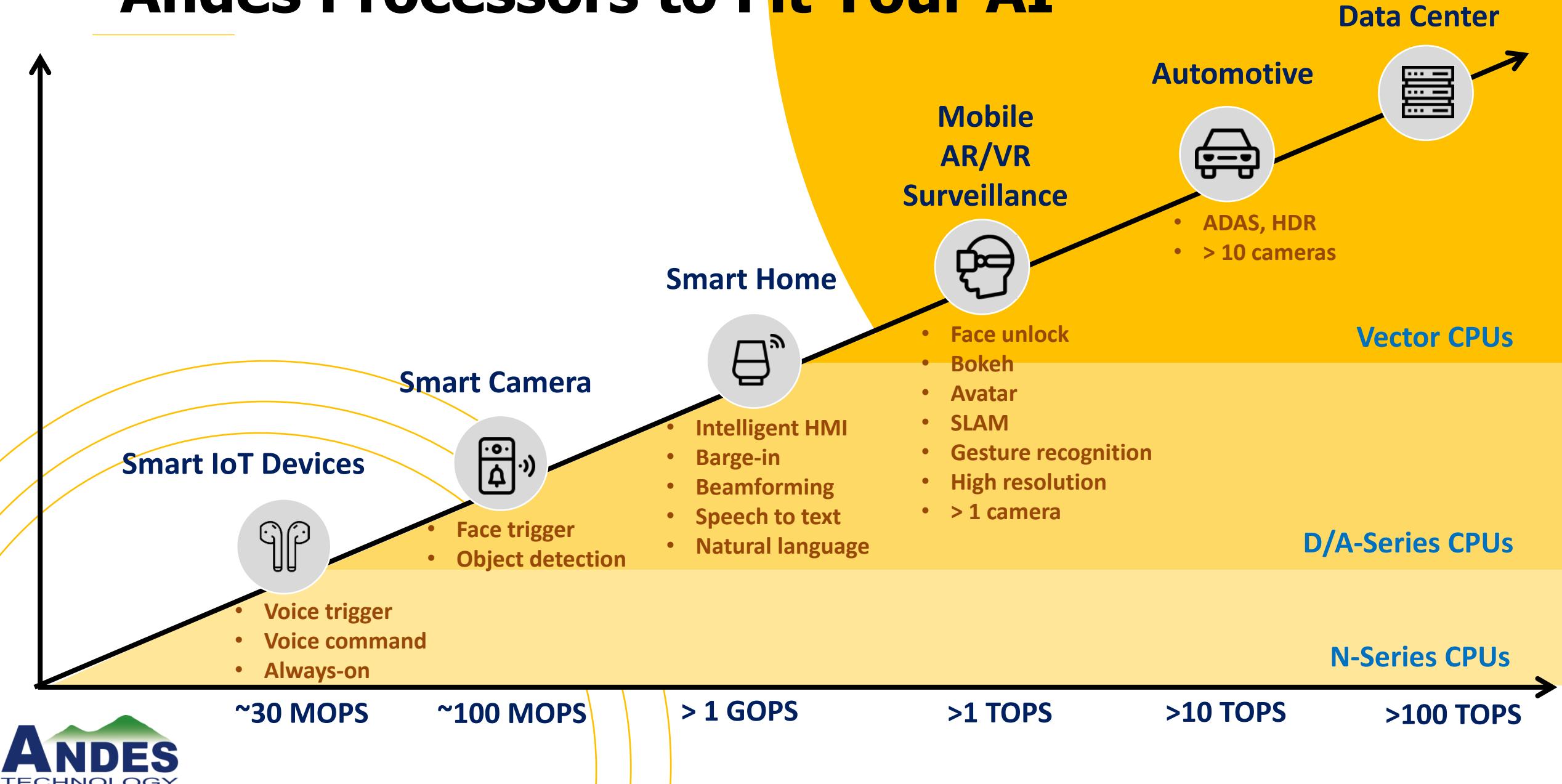
Define custom instruction to handle time critical codes

Andes Custom Extension

Better approach for accelerator /co-processor to do particular jobs

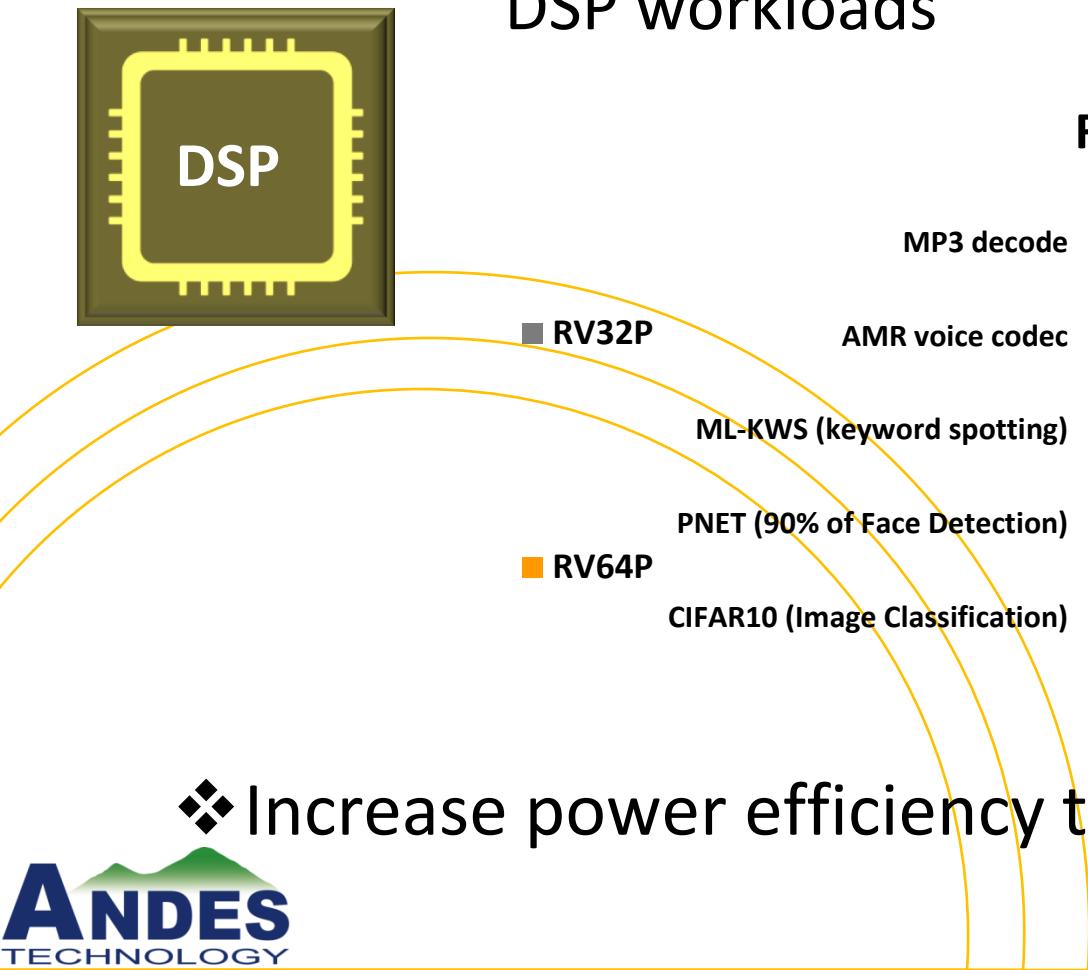
Automation Tool for the generation of toolchain, ISS, partial RTL and verification

Andes Processors to Fit Your AI

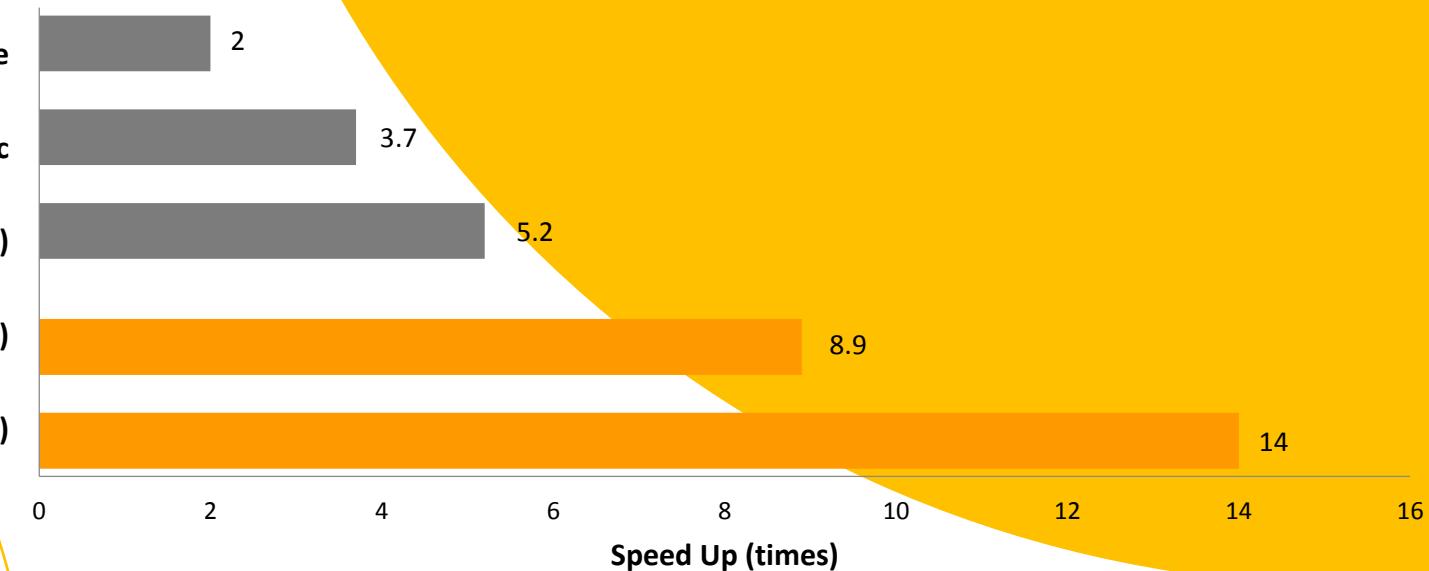


RISC-V DSP Extension

- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads

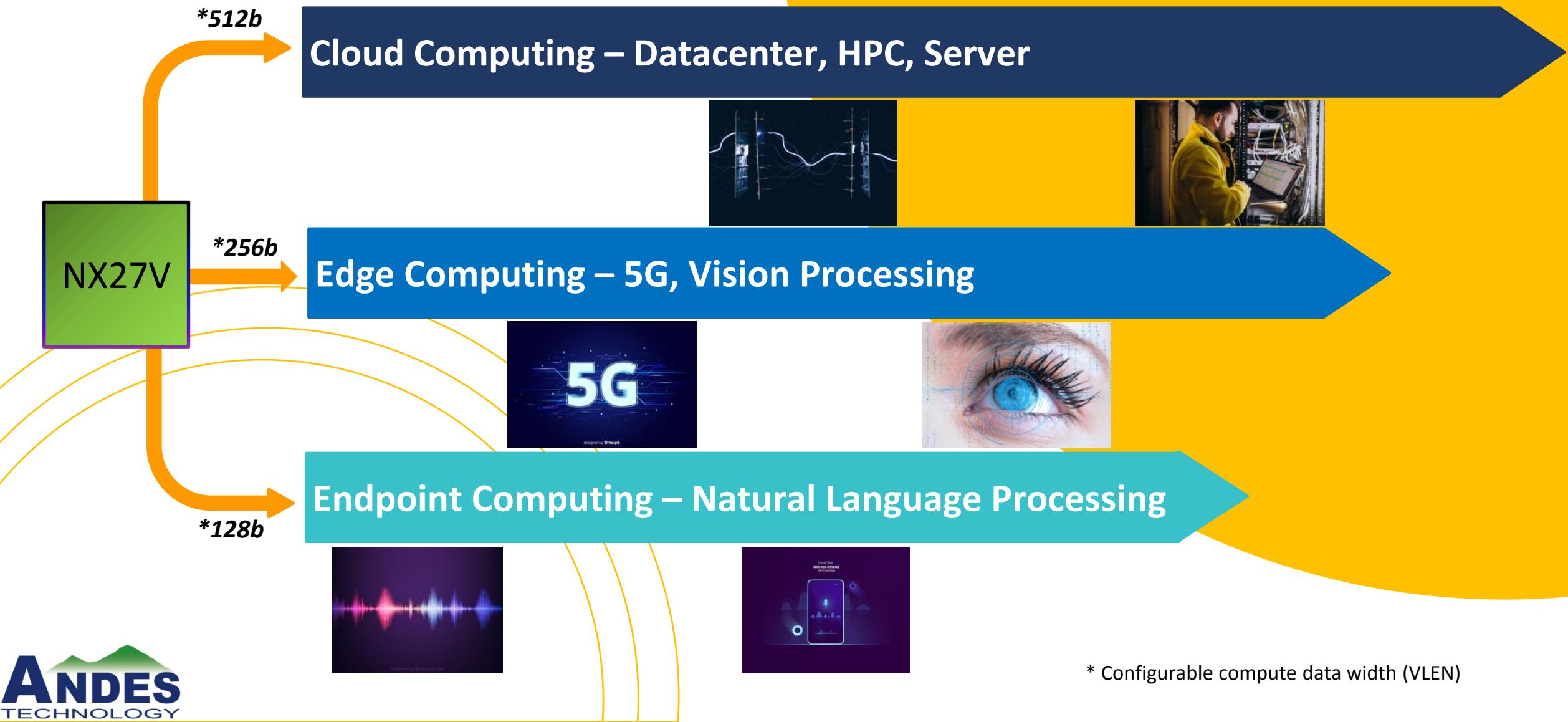


Real world speedup using P-Extension



❖ Increase power efficiency to your DSP applications

NX27V One Vector for All Implementations

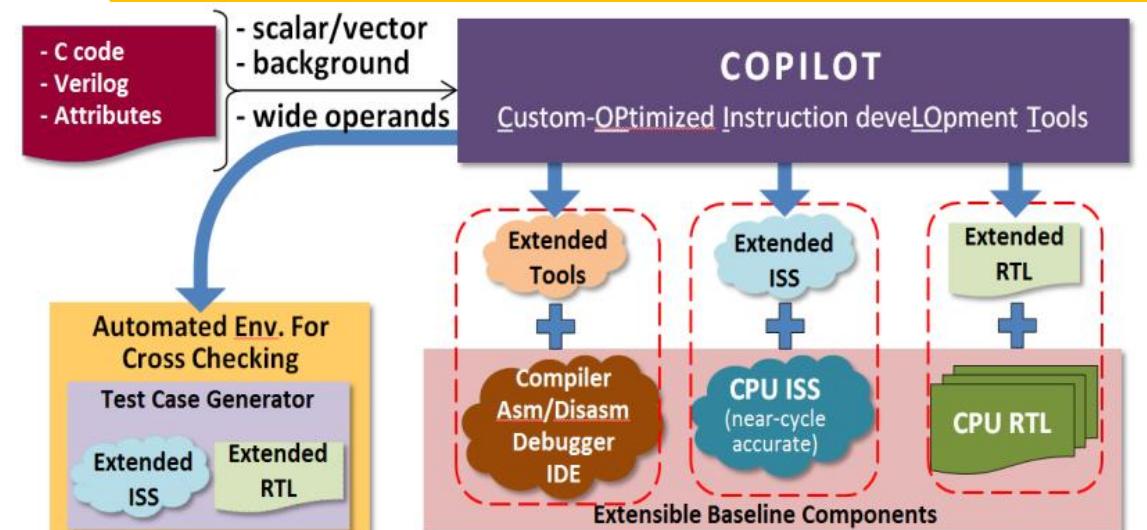


Andes Custom Extension



- ❖ ACE unlocks RISC-V's Potential of DSA
 - Define ACE instruction to handle time critical codes
 - Another approach to co-processor or accelerators

- ❖ All-in-one **COPilot** development environment
 - Automation tool and ease of use
 - Extensions are easy to re-use, can be used as a library



Taking RISC-V Cores to Next Level

❖ Andes is the world-leading supplier shipping the commercial RISC-V cores to market with the support of

P-Extension

- D25F, A(X)25(MP), A(X)27, A(X)45

V-Extension

- NX27V, NX45V

Custom-Extension

(w/ ACE* support)

- Entire 25, 27, 45 series

*: Andes Custom Extension

Bring Andes Strength to RISC-V Cores

Performance & Extensibility

- Leading PPA and code size
- Rich data processing in P, V, and ACE

Configurability

- Flexible configurations for rich features

Maturity

- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE

Aggressive in RISC-V Community

Foundation Task Groups (partial list)



- ❖ Contributing hardware architecture extensions
 - Chair of the P-extension (Packed SIMD/DSP) Task Group
 - Co-chair of Fast Interrupts Task Group
- ❖ Closely reviewing activities of other Task Groups

Andes Helps Strengthen RISC-V Ecosystem

- ❖ More choices for customers are good
- ❖ Andes works closely with partners to grow RISC-V ecosystem



Andes Position in RISC-V



Complete product portfolio

Reliable RISC-V core IP vendor

Extreme low power consumption, high computing efficiency

World's leading P-, V- and Custom-Ext. Capable RISC-V cores

Professional custom computing service

Two Ecosystems: Andes and Knect.me



knectme™



Knect.me™ Ecosystem

❖ Built up the community to help developing IoT products

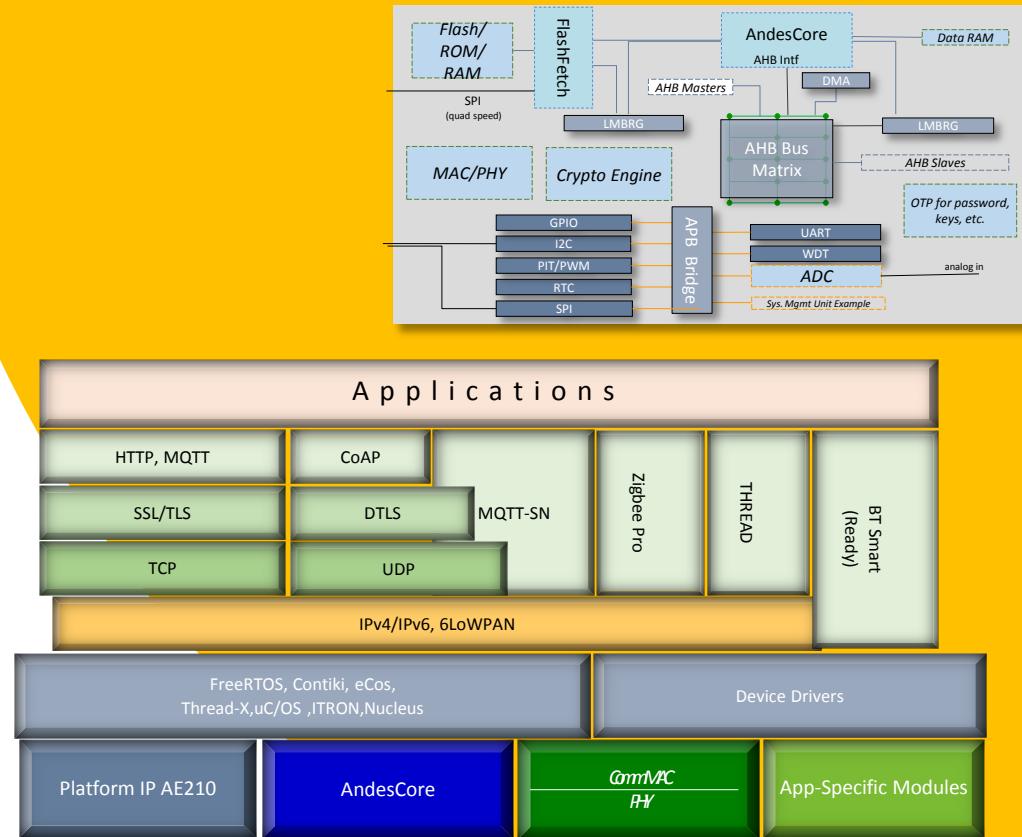
- To knect solutions for silicon IP's, SW stacks, tools, applications, systems and products

■ Including

- SoC IP Platforms
- Software Stack
- Development Boards
- Development Tools

❖ Forms a IoT League

- To knect chip vendors, partners, application developers, system vendors



FreeStart Program

❖ FreeStart Evaluation Program (FSEP)

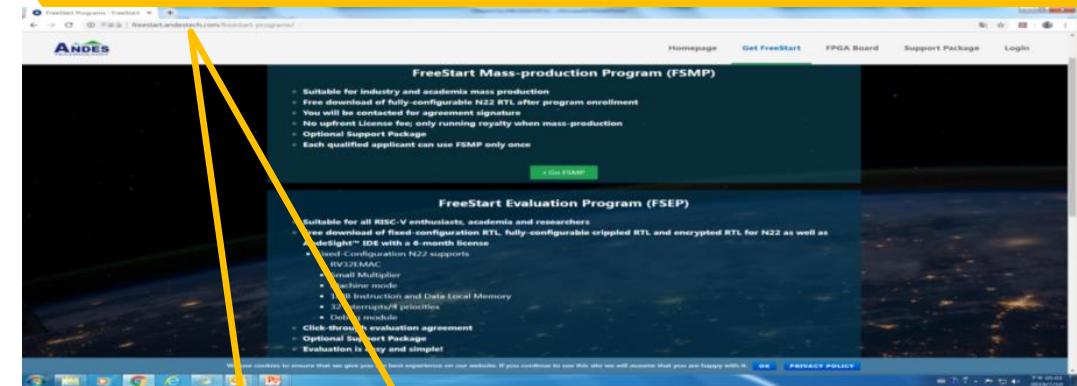
- For all RISC-V enthusiasms and educator/researcher
- Fixed-Configuration N22 RTL
- Sign simple evaluation agreement directly on website

❖ FreeStart Mass-production Program (FSMP)

- For industrial and academy mass production
- Full-configuration N22 RTL
- License fee: \$0; only running royalty is required when mass production

❖ Support Package (FSSP)

- For all
- \$20K for 1st year, including
 - 1 year e-service
 - FreeStart AE250 RTL
 - Corvette F1 FPGA board



For more info., please visit
www.andestech.com

Event Promotion



RISC-V Summit in San Jose
2020: Diamond Sponsor



Concluding Remarks

<http://www.andestech.com>



A Trusted Computing Expert



Thank You

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