

Andes Technology Corporation 2018 Investor Conference Report

Driving Innovations™



Stock #: 6533
2019/03/22

Safe Harbor Notice



Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

Agenda

- **Overview of Andes Technology Corporation**
- **Operating Results**
- **Product Applications**
- **New Products and Ecosystems**
- **Andes Awarded**
- **Concluding Remarks**

Overview of Andes Technology Corporation



Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Core RD team from **AMD, DEC, Intel, MIPS, nVidia**, and **Sun** veterans.
- Over 160 people now; 80% are engineers.
- EETimes' Silicon 60 **Hot Startups to Watch** (2012)
- **TSMC OIP Award** "Partner of the Year" for New IP (2015)
- A founding member of **RISC-V Foundation** (2016)
- **IPO in Taiwan Stock Exchange** (March 2017)

Andes Mission

- Innovate **performance-efficient** processor solution for **low-power** SoC

Emerging Opportunities

- **Smart** and **Green** electronic devices
- **Cloud Computing, Artificial Intelligence** and **Internet of Things**

Operating Results

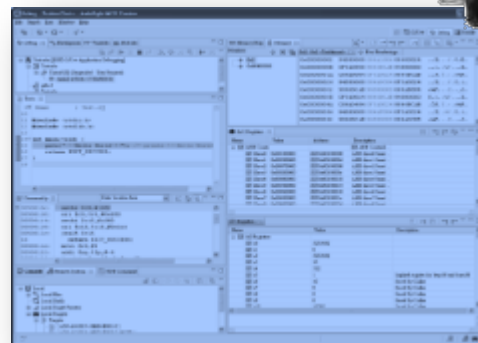


Business Status Overview

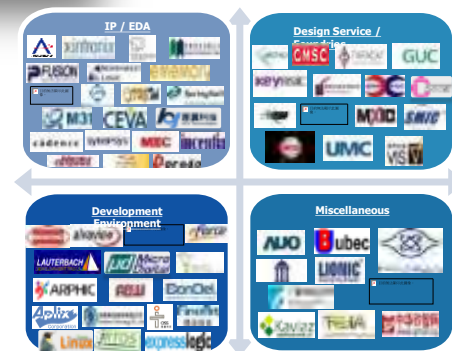
- **>160** commercial licensees
 - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
 - **>246** license agreements signed



- AndeSight™ IDE:
 - **>14,000** installations

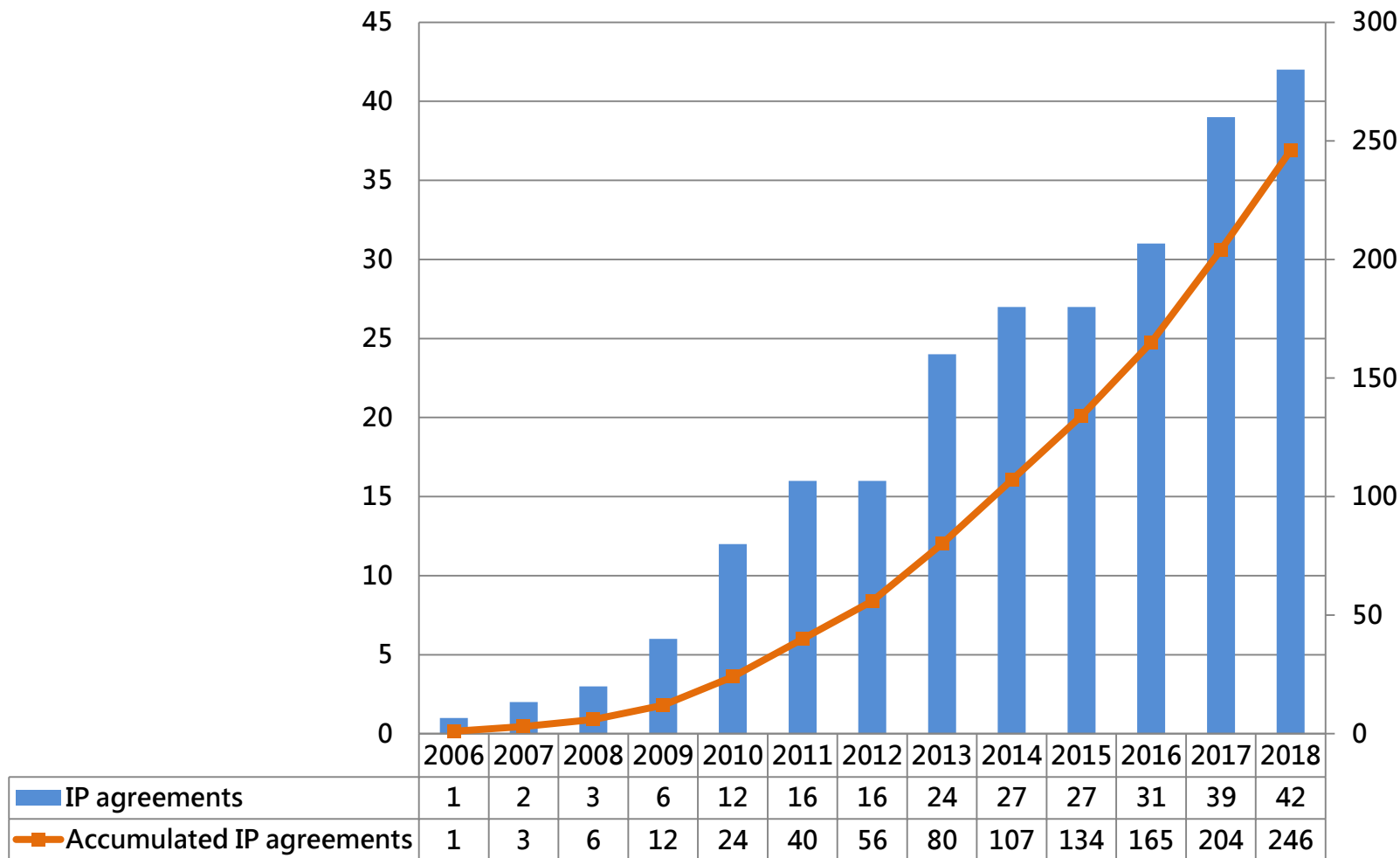


- Eco-system:
 - **>130** partners

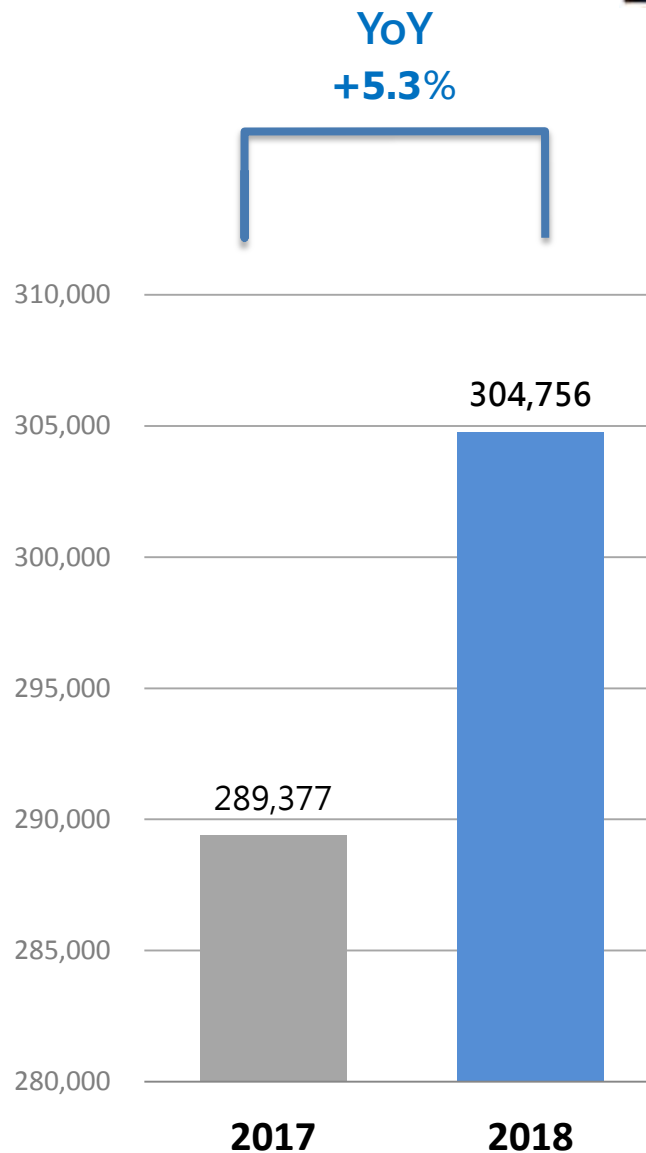
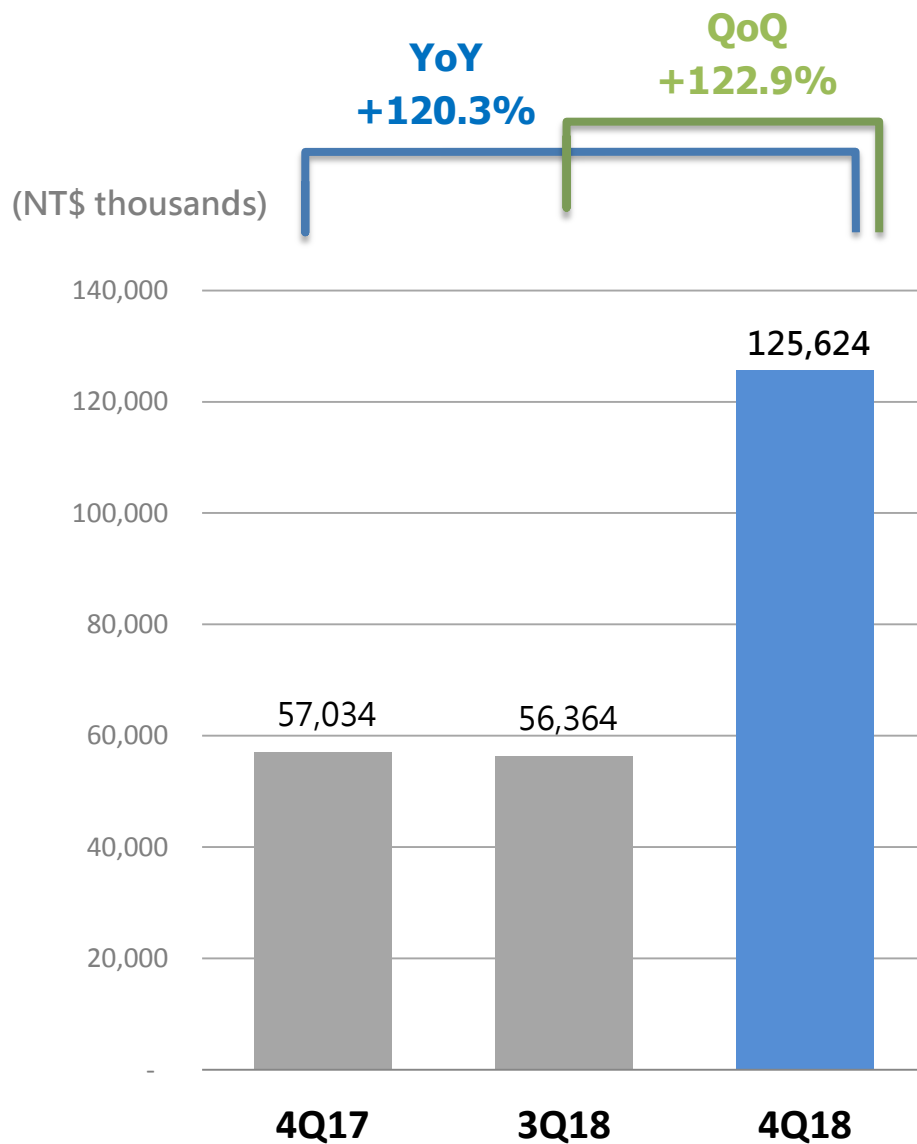


- **>3.6B** Accumulative SoC Shipped by the end of 2018

Agreement Growth Analysis



2018 Revenue Analysis

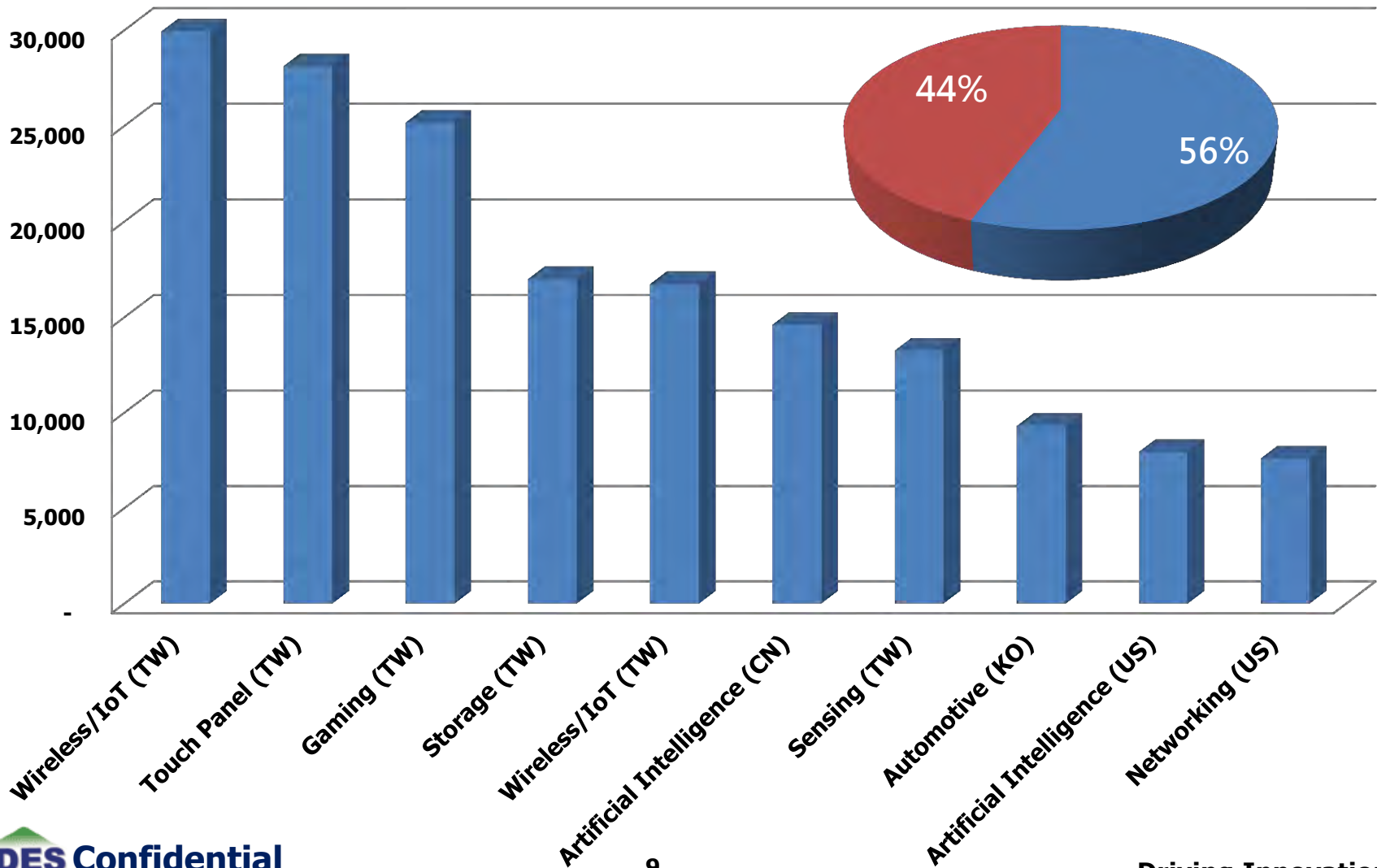


2018 Top 10 Customers Analysis by Revenue



(NT\$ thousands)

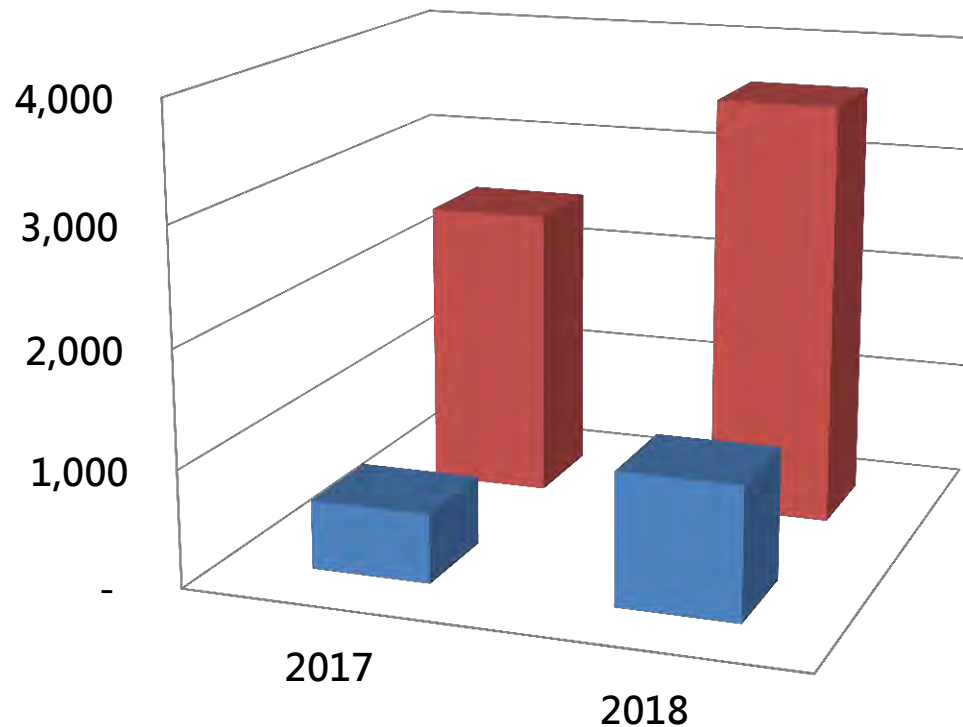
Top 10 Customer Contributed 56% Revenue



Total Customers Annual and Accumulated Shipment

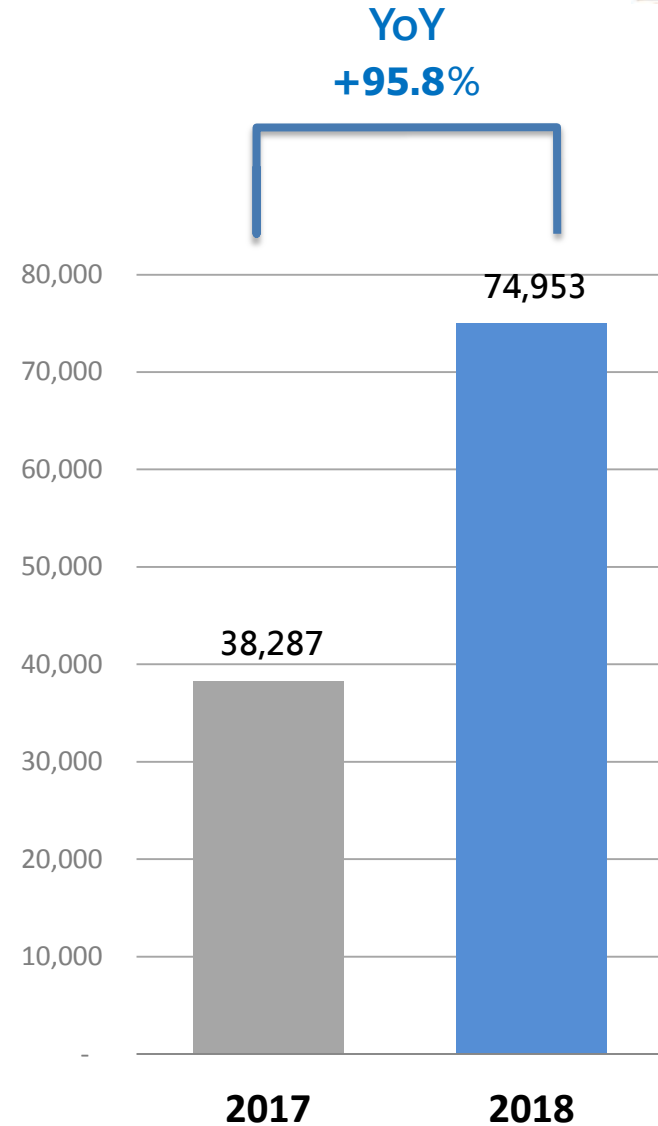
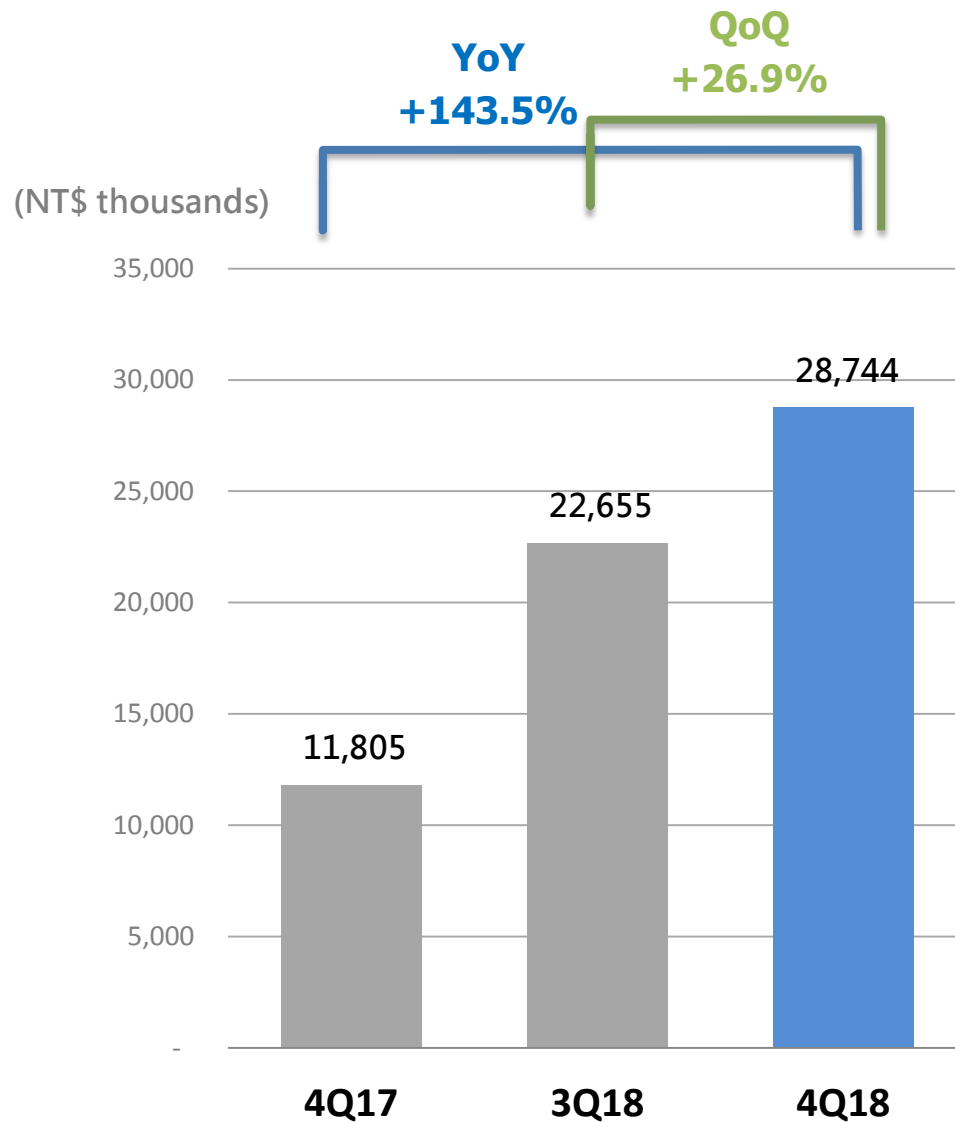


(Unit: M ps)



	2017	2018
■ Annual Shipment	590	1,132
■ Accumulated Shipment	2,500	3,632

2018 Royalty Analysis

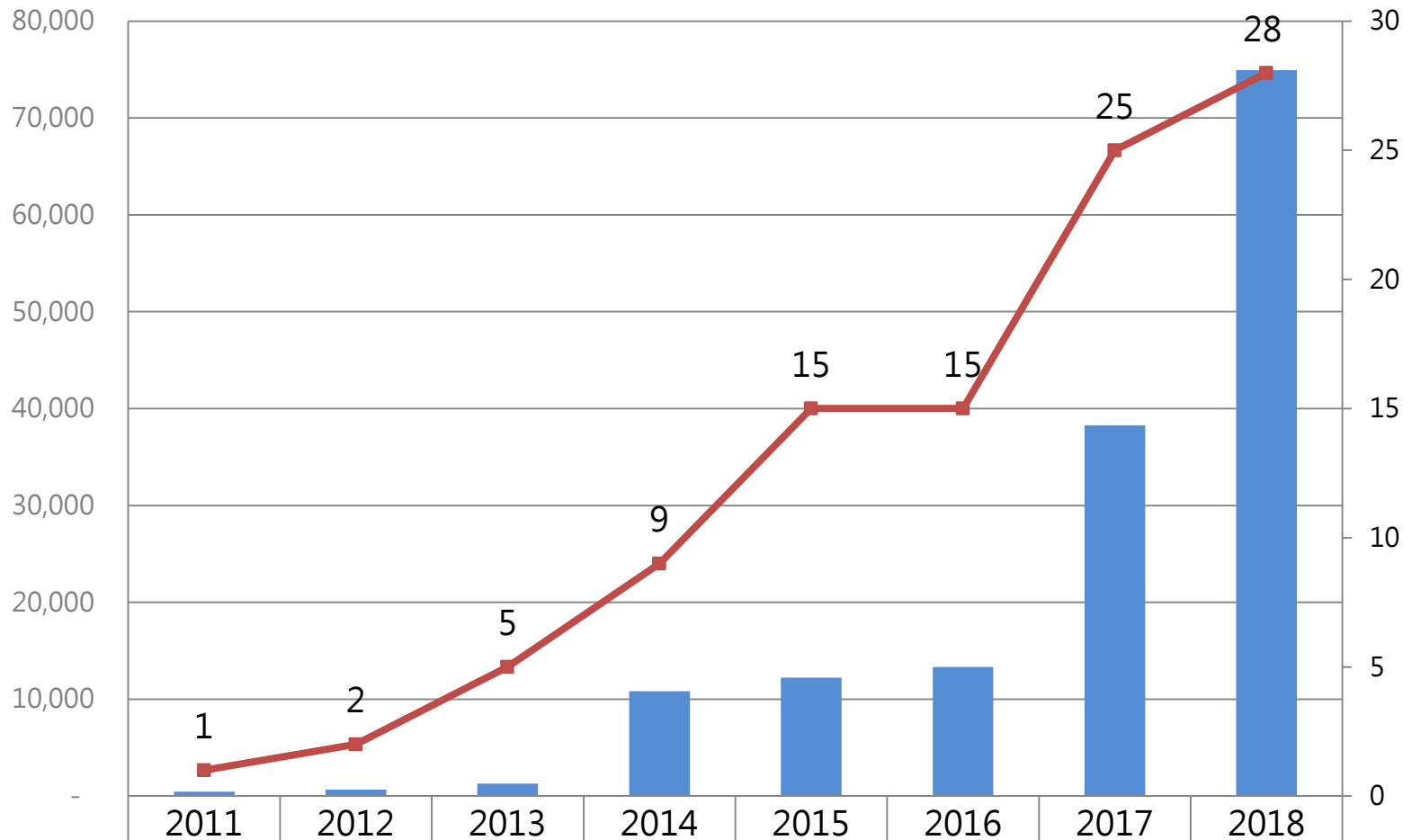


Royalty & Contributors Analysis



(NT\$ thousands)

(Customer numbers)



Royalty	445	660	1,285	10,819	12,232	13,320	38,287	74,953
Customer numbers	1	2	5	9	15	15	25	28

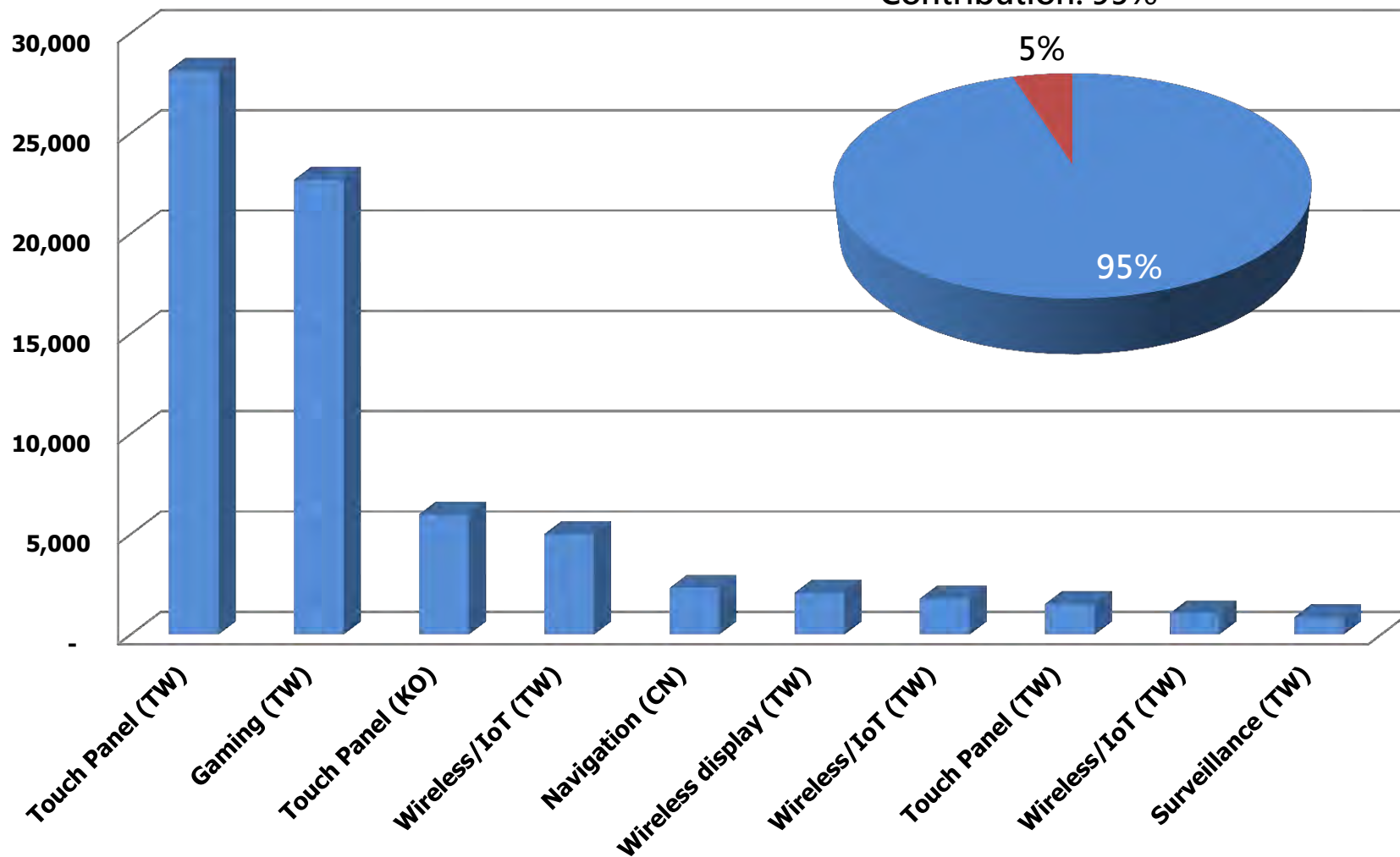
2018 Top Ten Royalty Contributors Analysis by Application



(NT\$ thousands)

Top 10 Royalty Customers

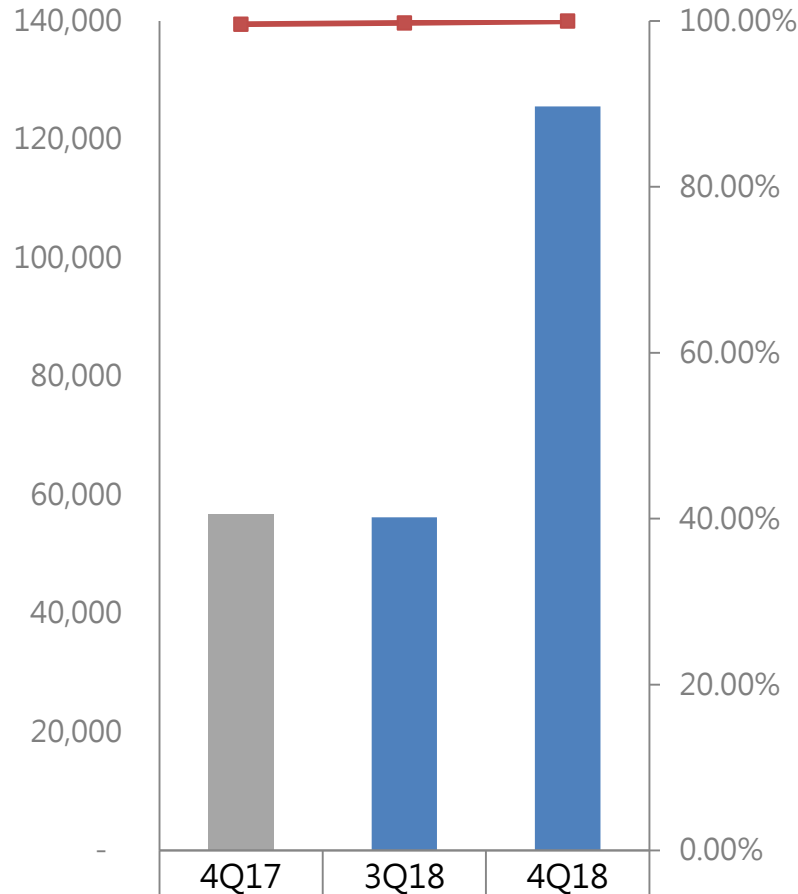
Contribution: 95%



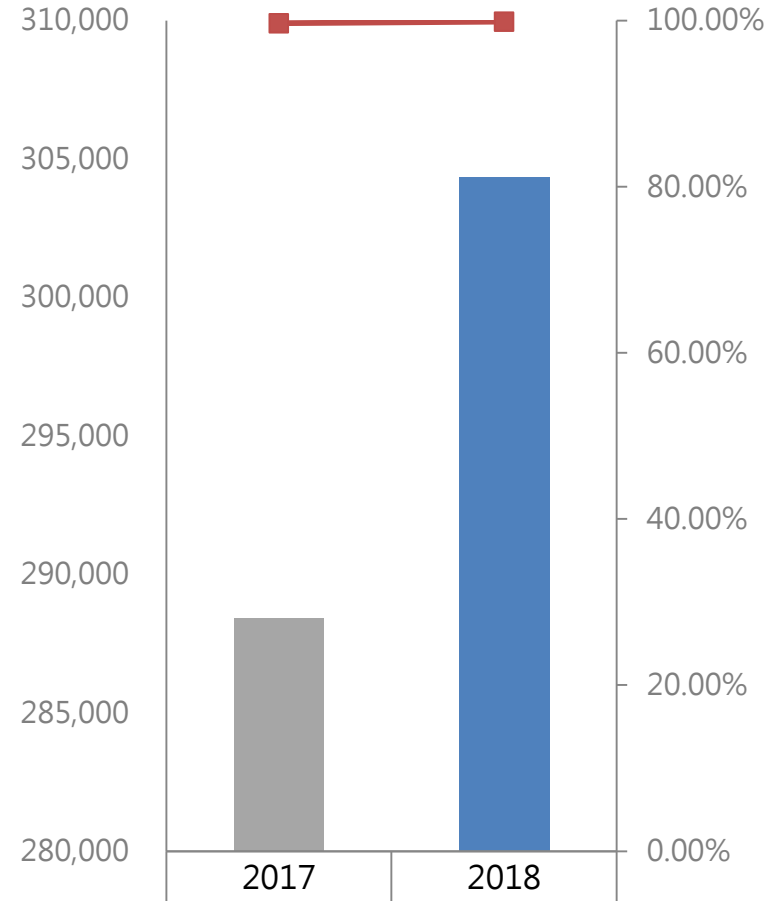
Consolidated Gross Margin



(NT\$ thousands)

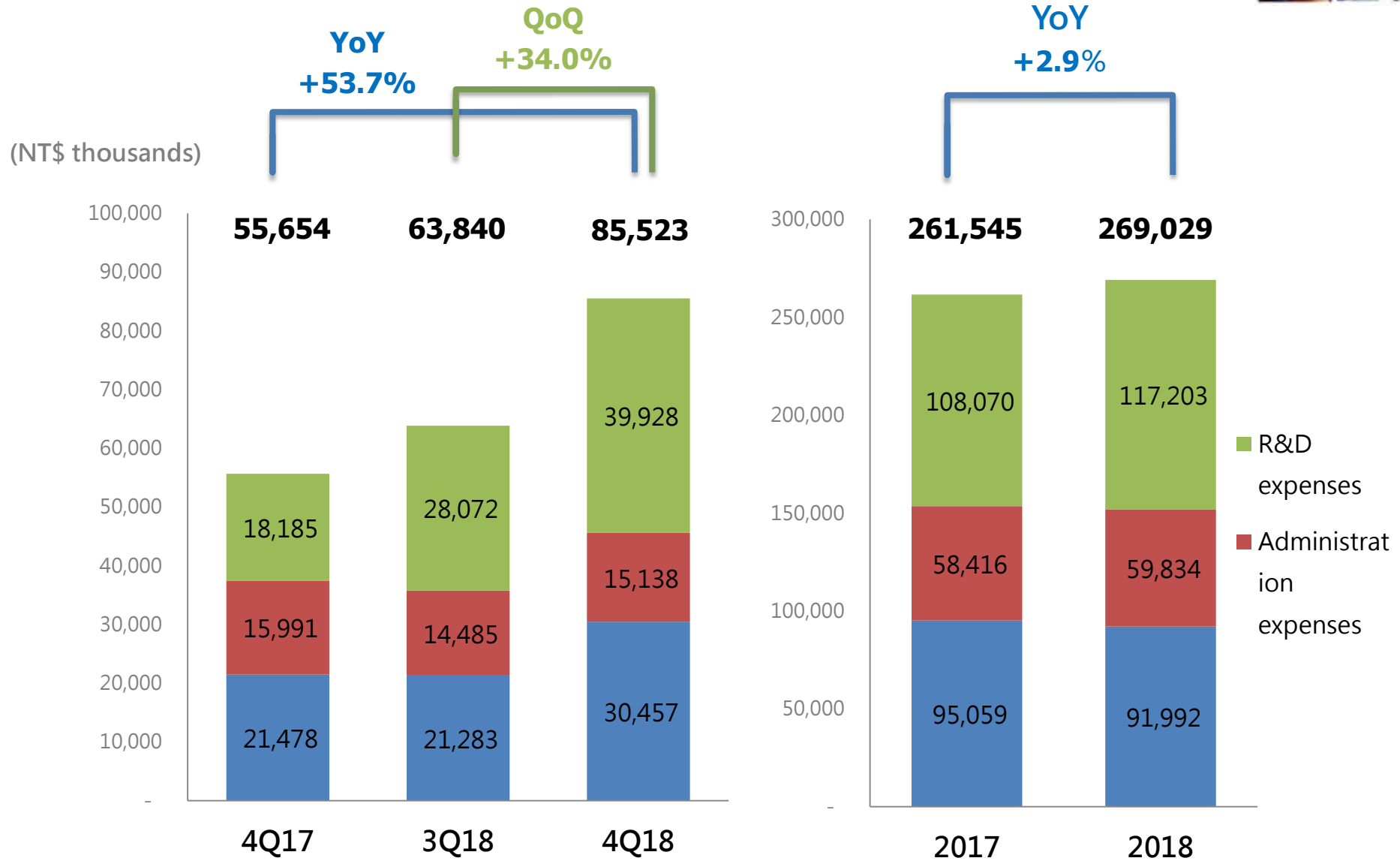


Gross Profit	56,798	56,217	125,574
Gross Margin	99.59%	99.74%	99.96%

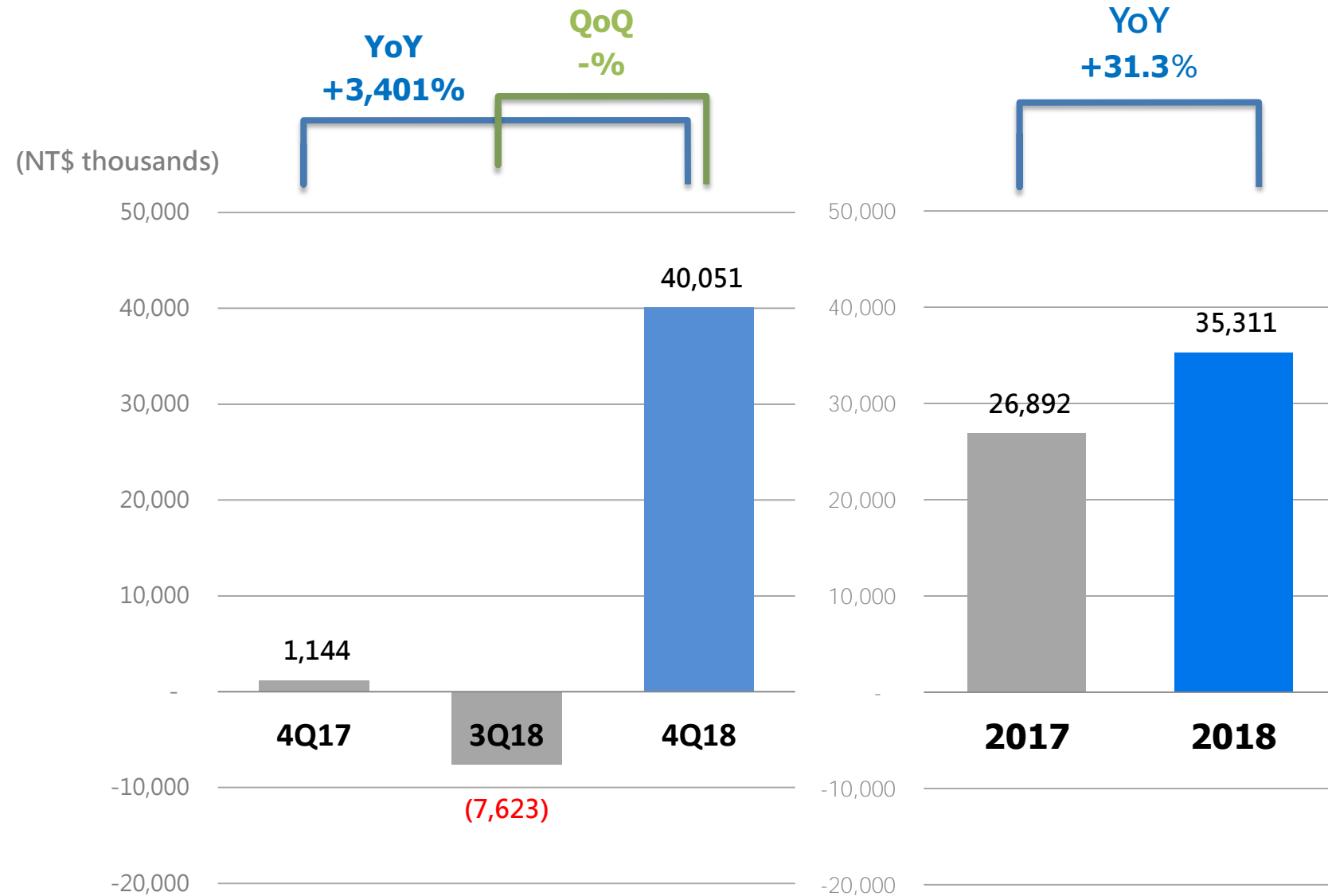


Gross Profit	288,437	304,340
Gross Margin	99.68%	99.86%

Consolidated Operating Expenses



Consolidated Operating Income



Consolidated Operating Margin

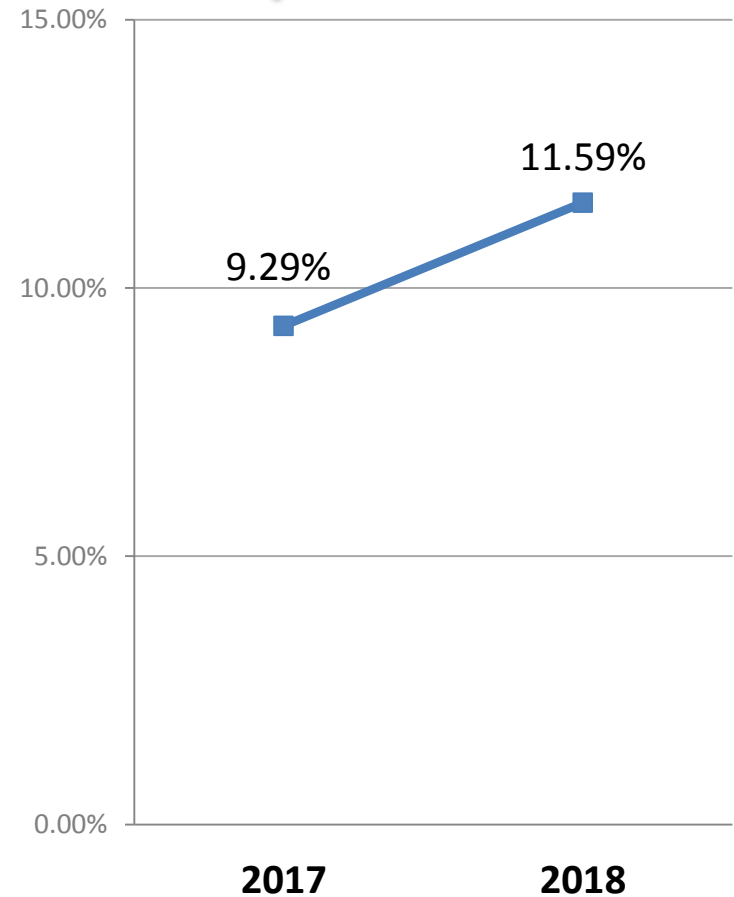
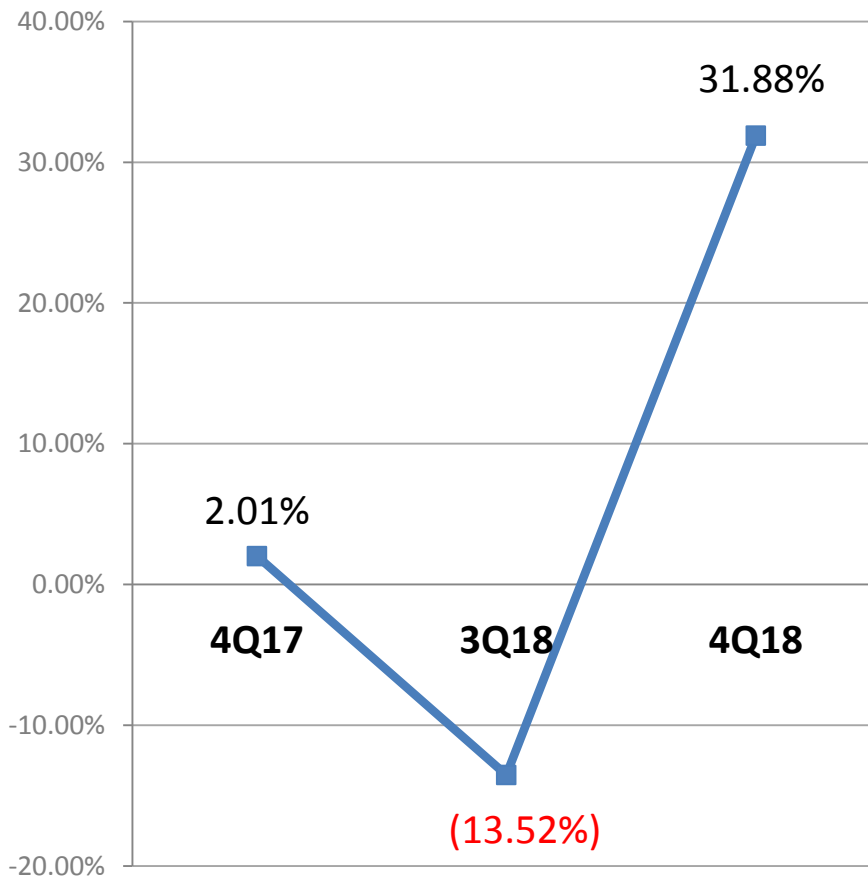


YoY
+29.87 pt

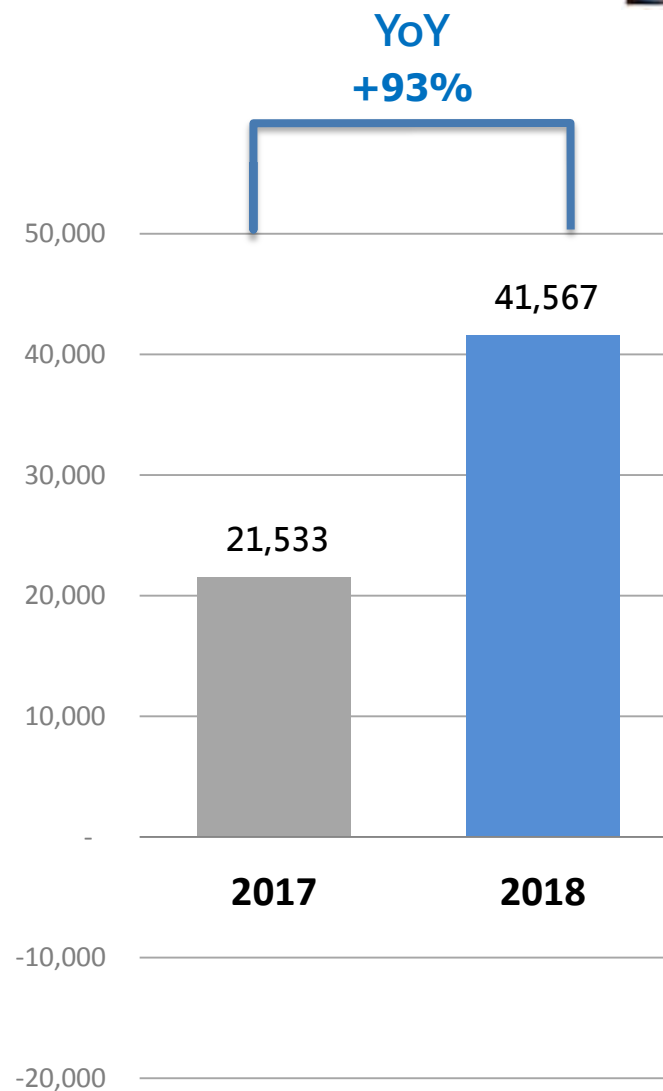
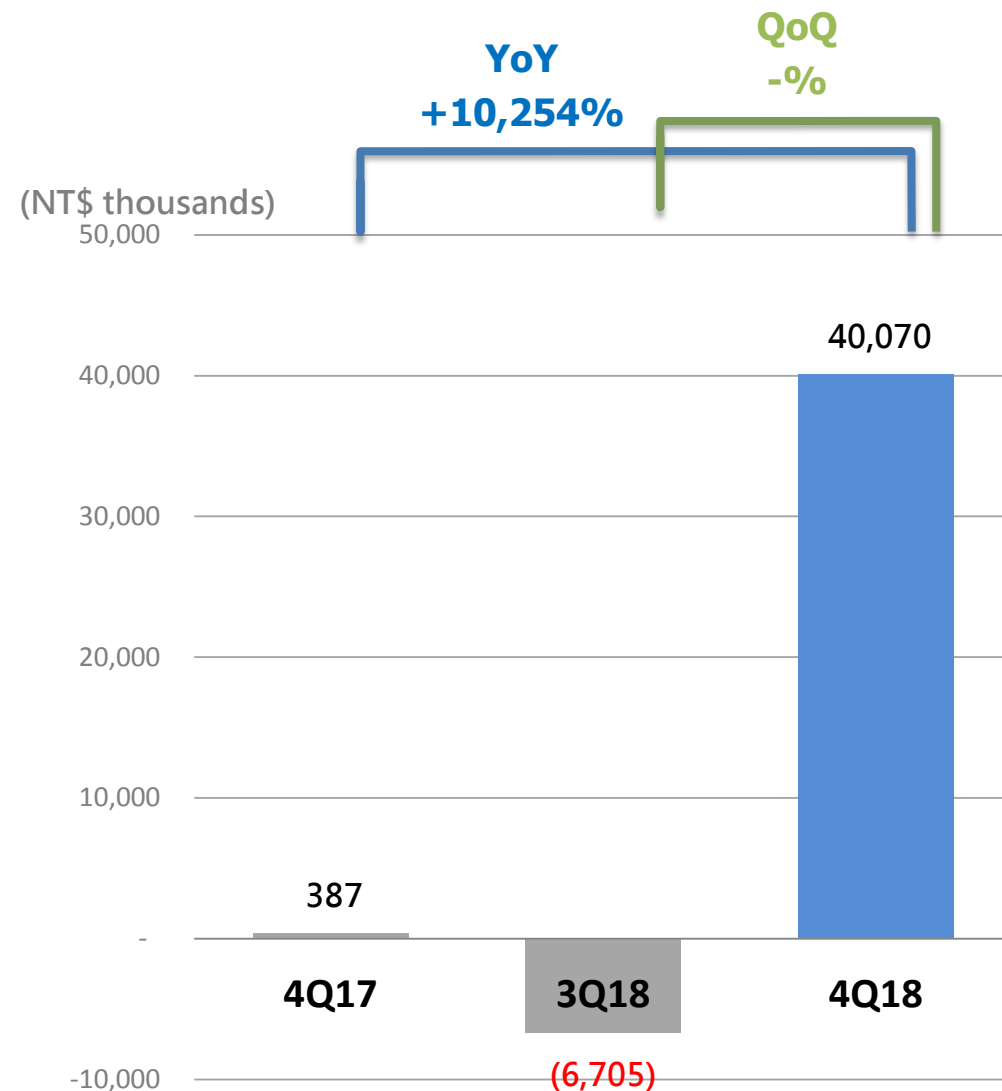
QoQ
+45.40 pt

YoY
+2.30 pt

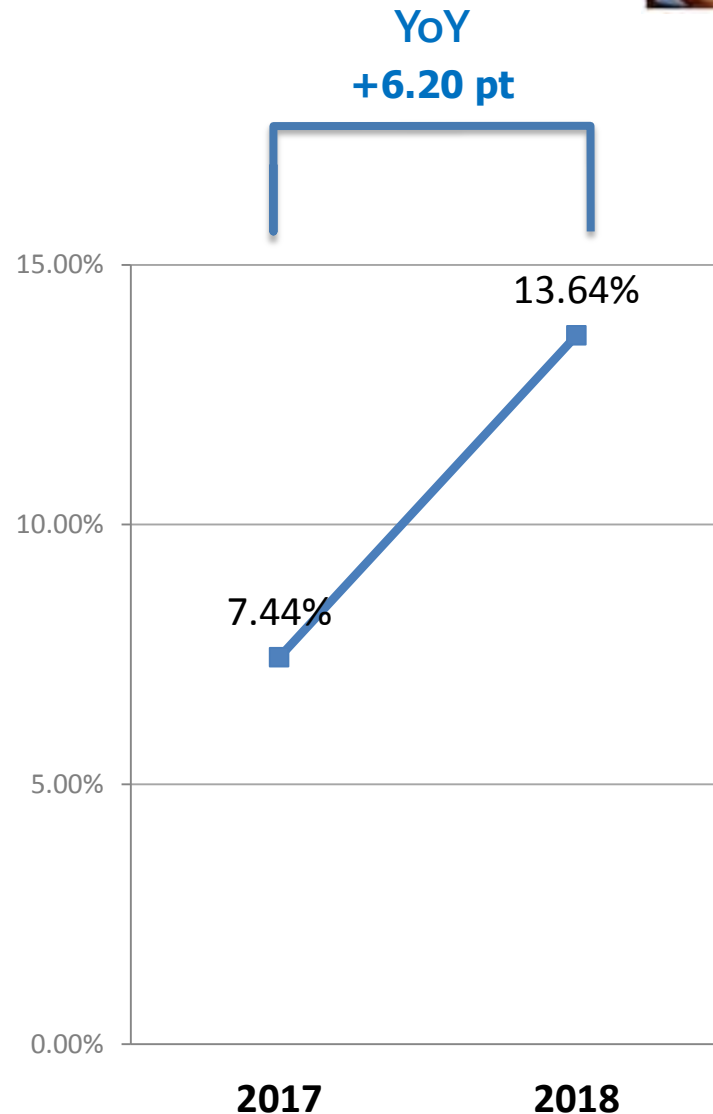
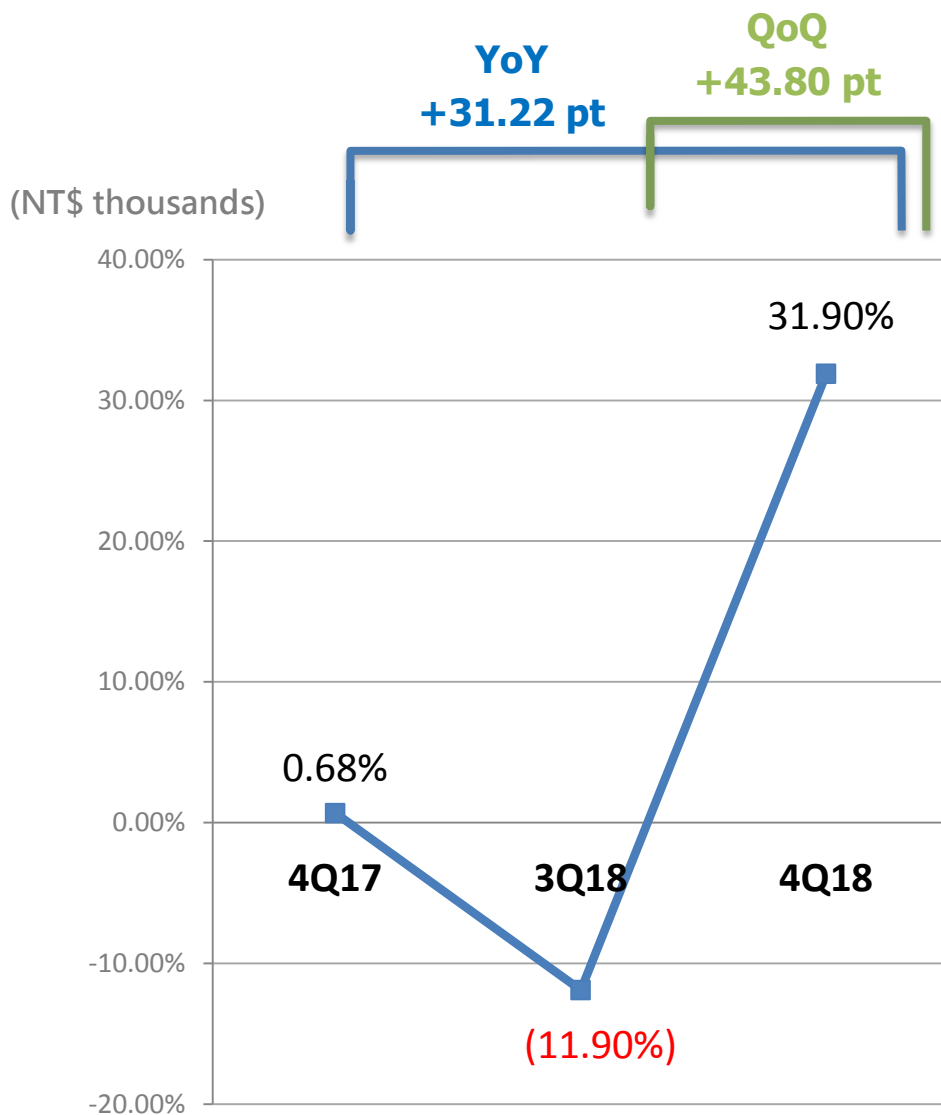
(NT\$ thousands)



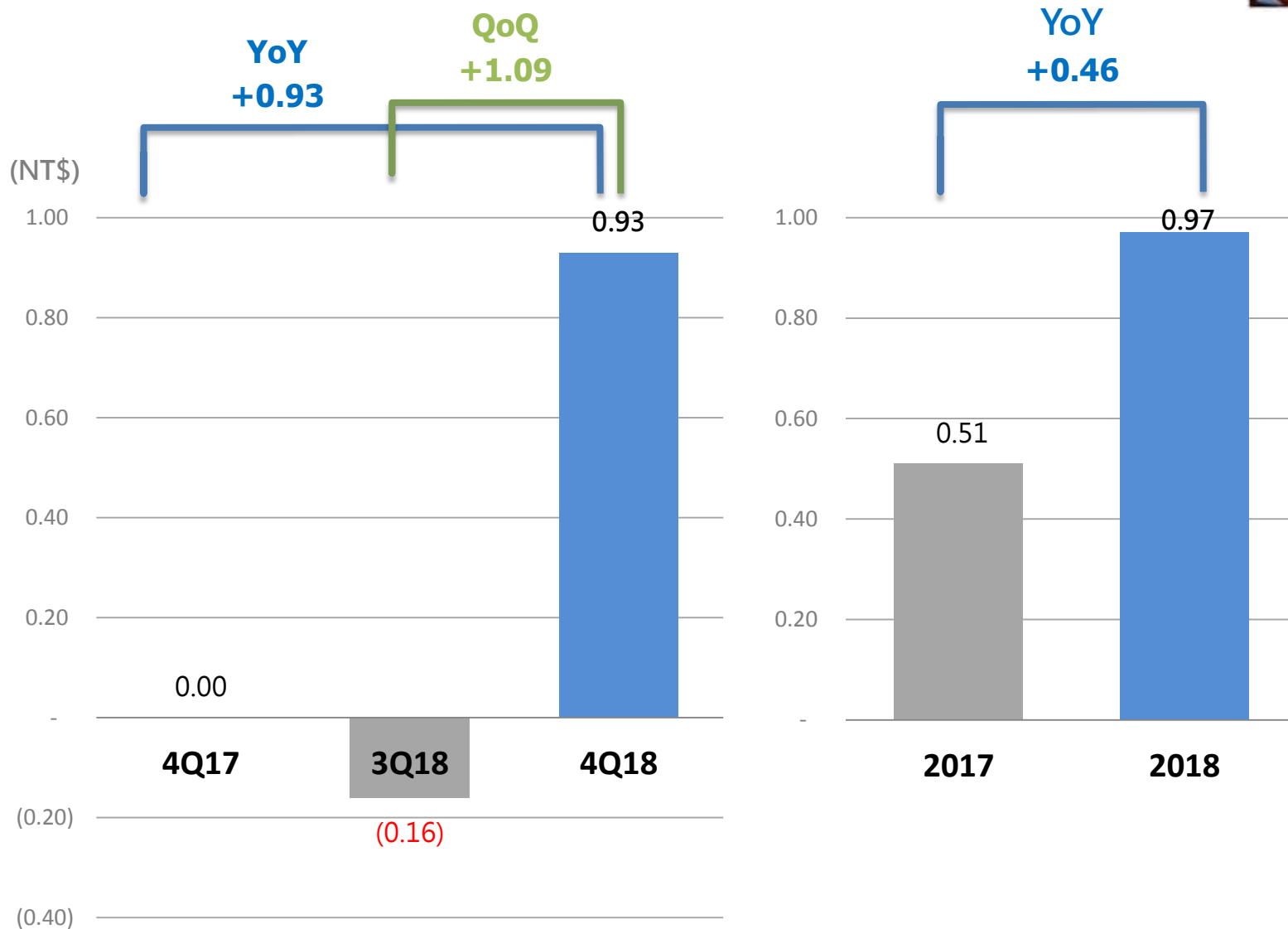
Consolidated Net Income



Consolidated Net Profit Margin



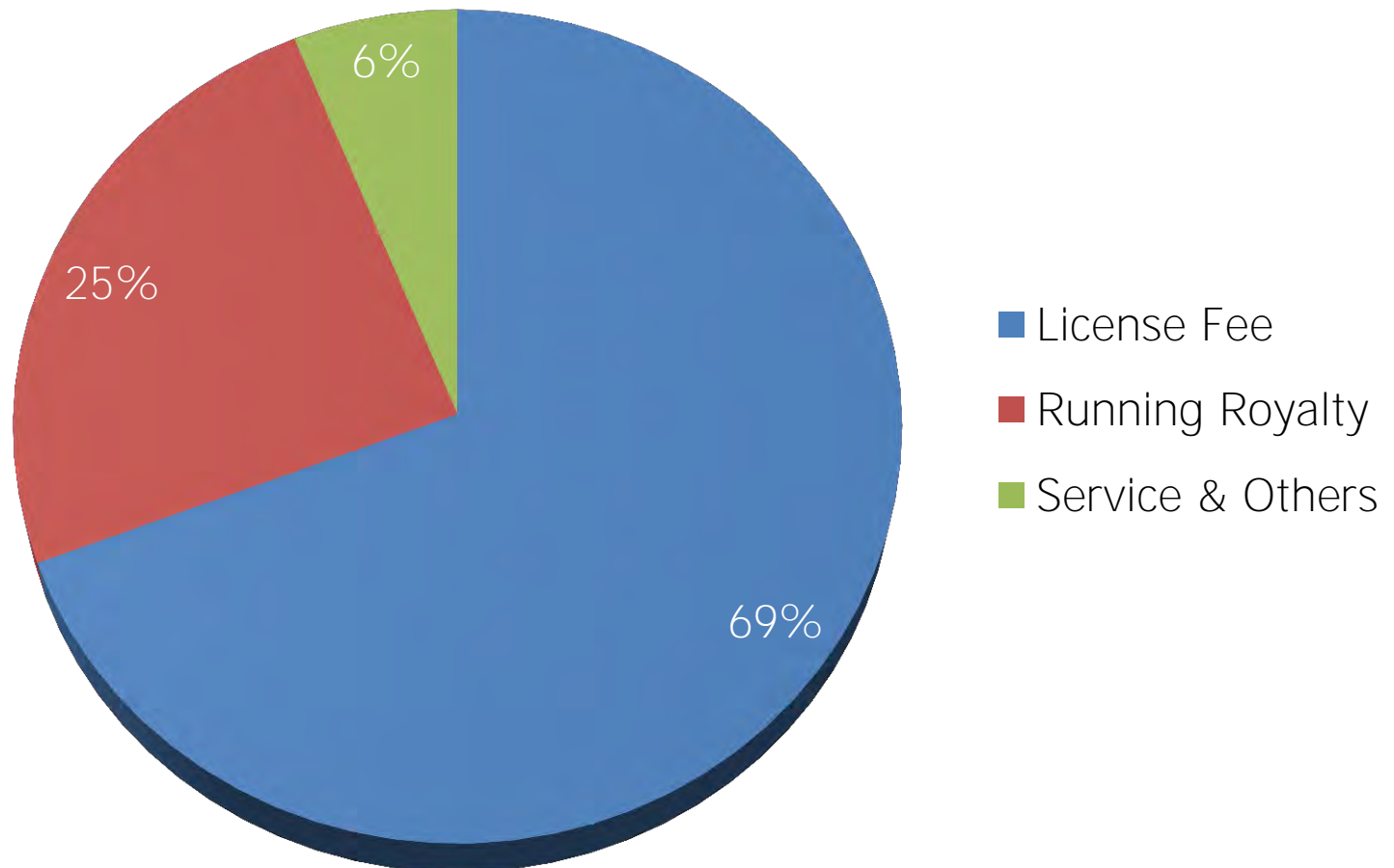
Consolidated Earnings Per Share



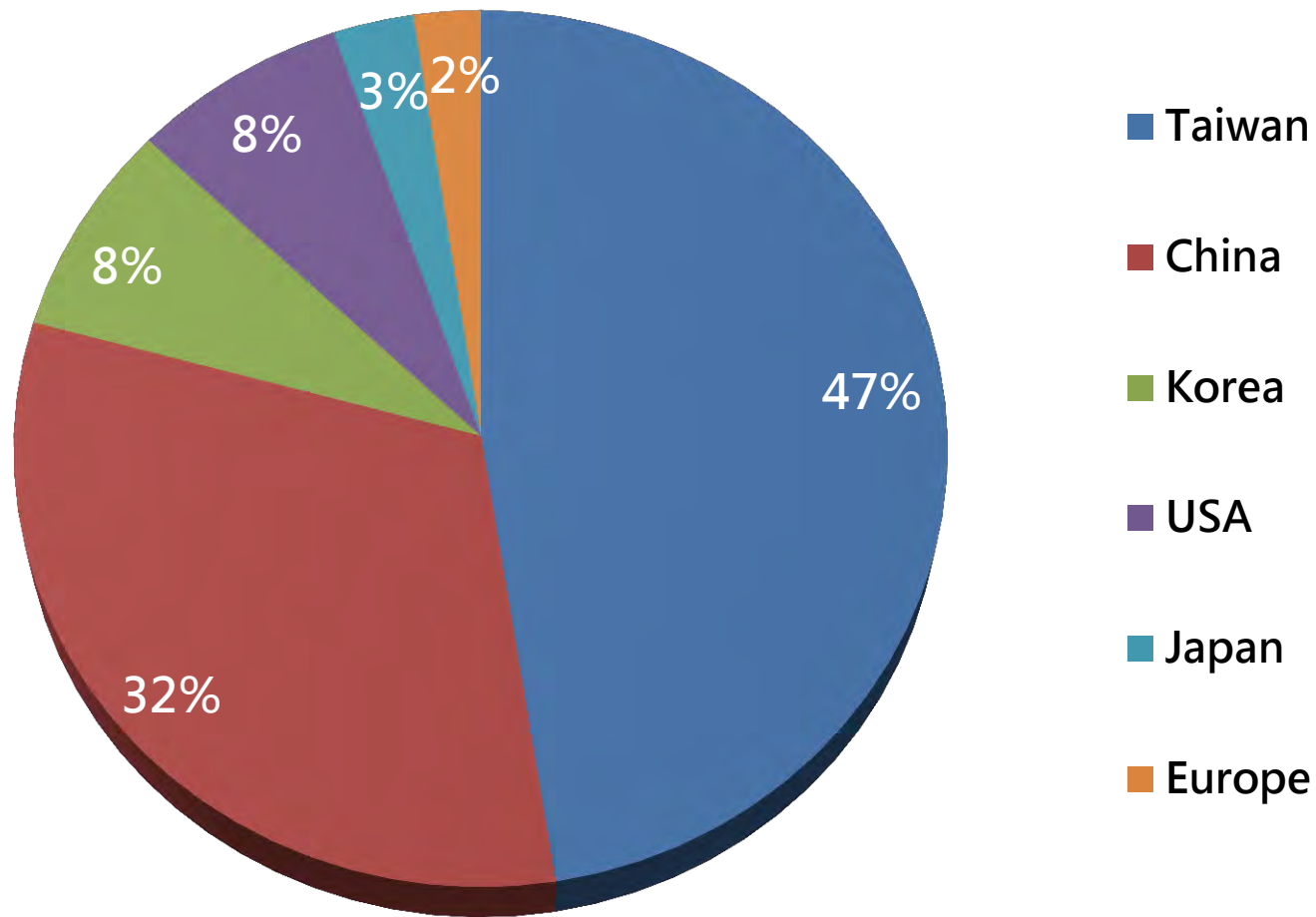
Revenue Analysis by Payment Model



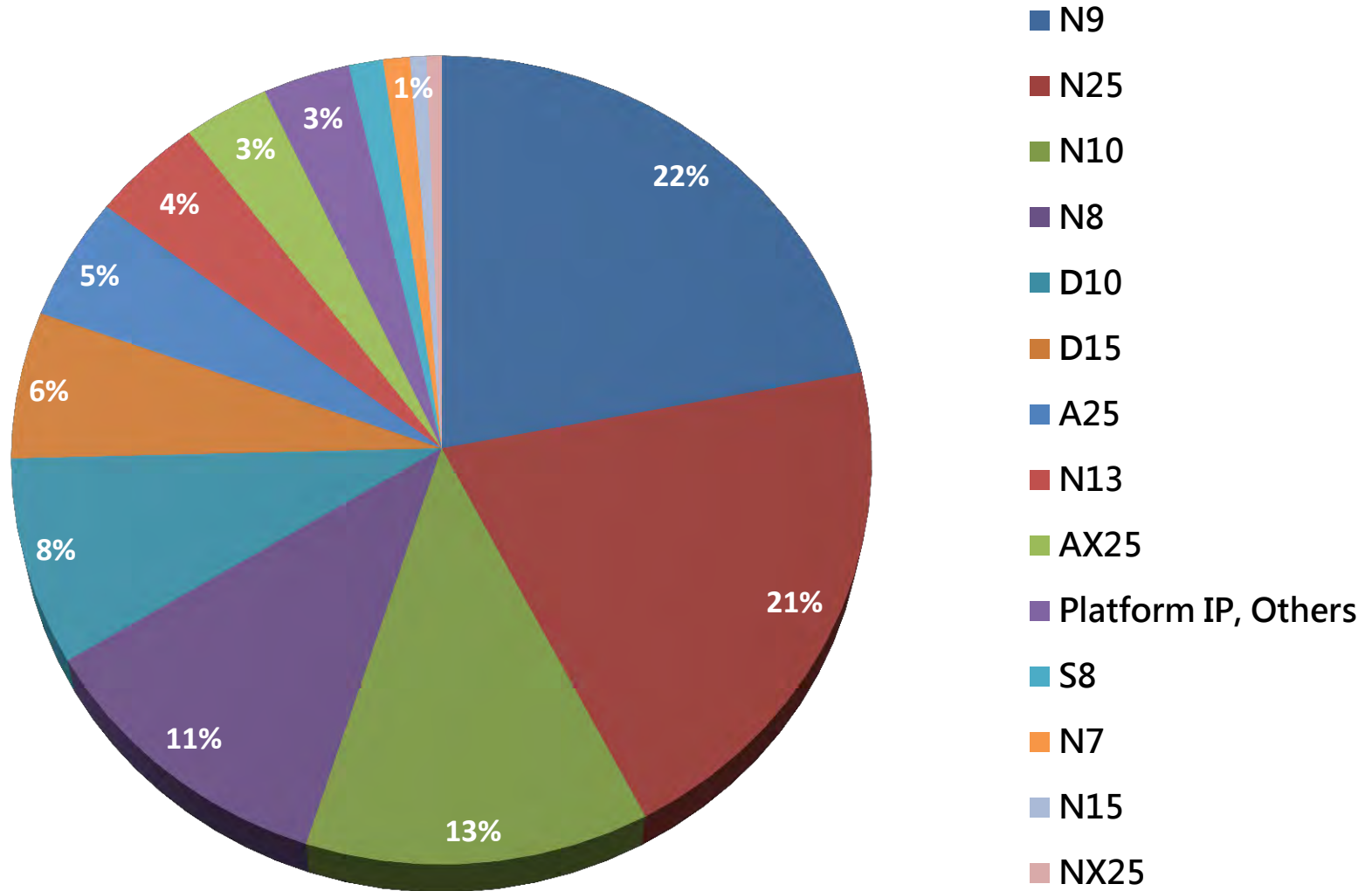
(2018/01-12 New Agreements: 42)



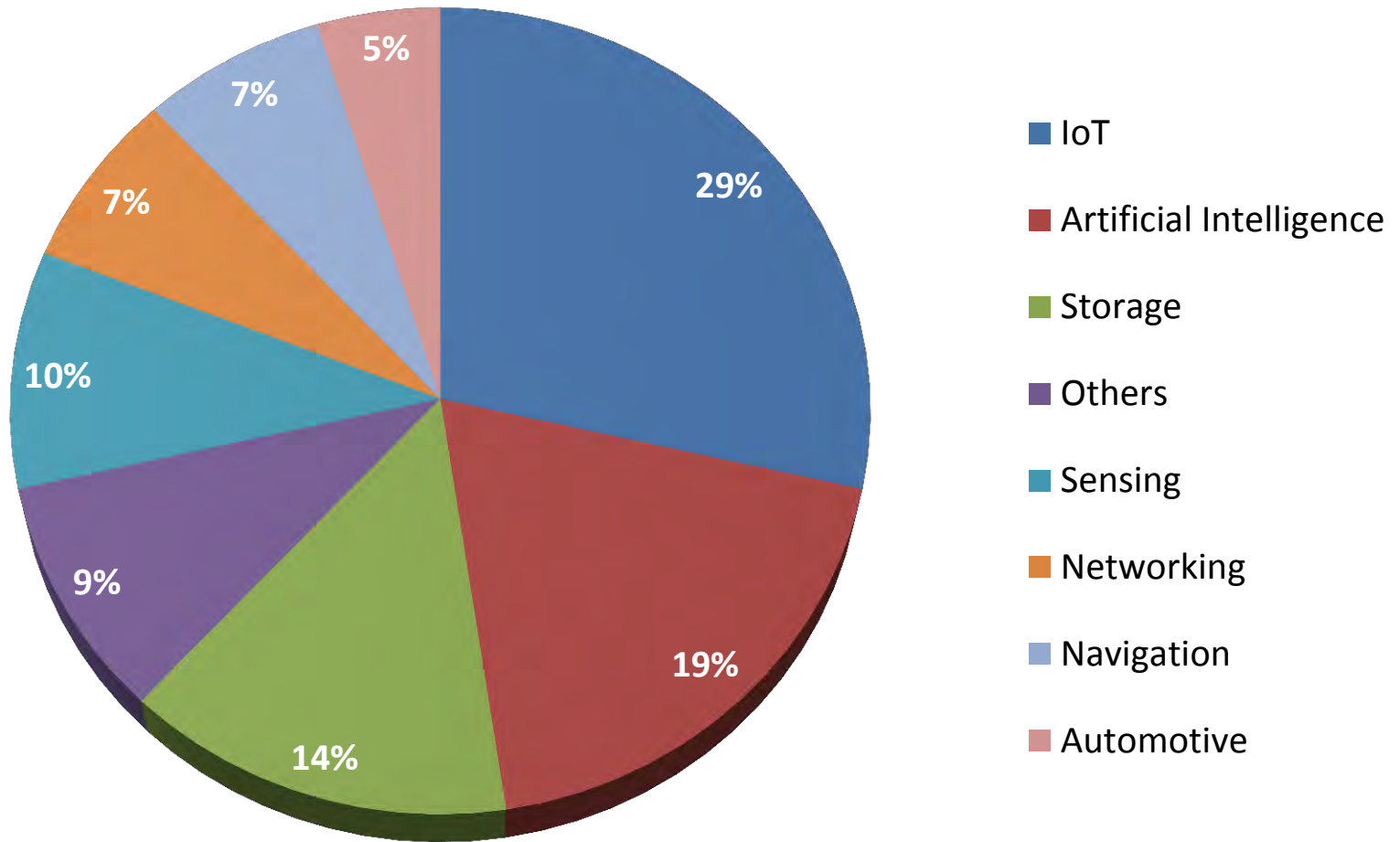
Revenue Analysis by Region



Revenue Analysis by Product



Customer Application Analysis

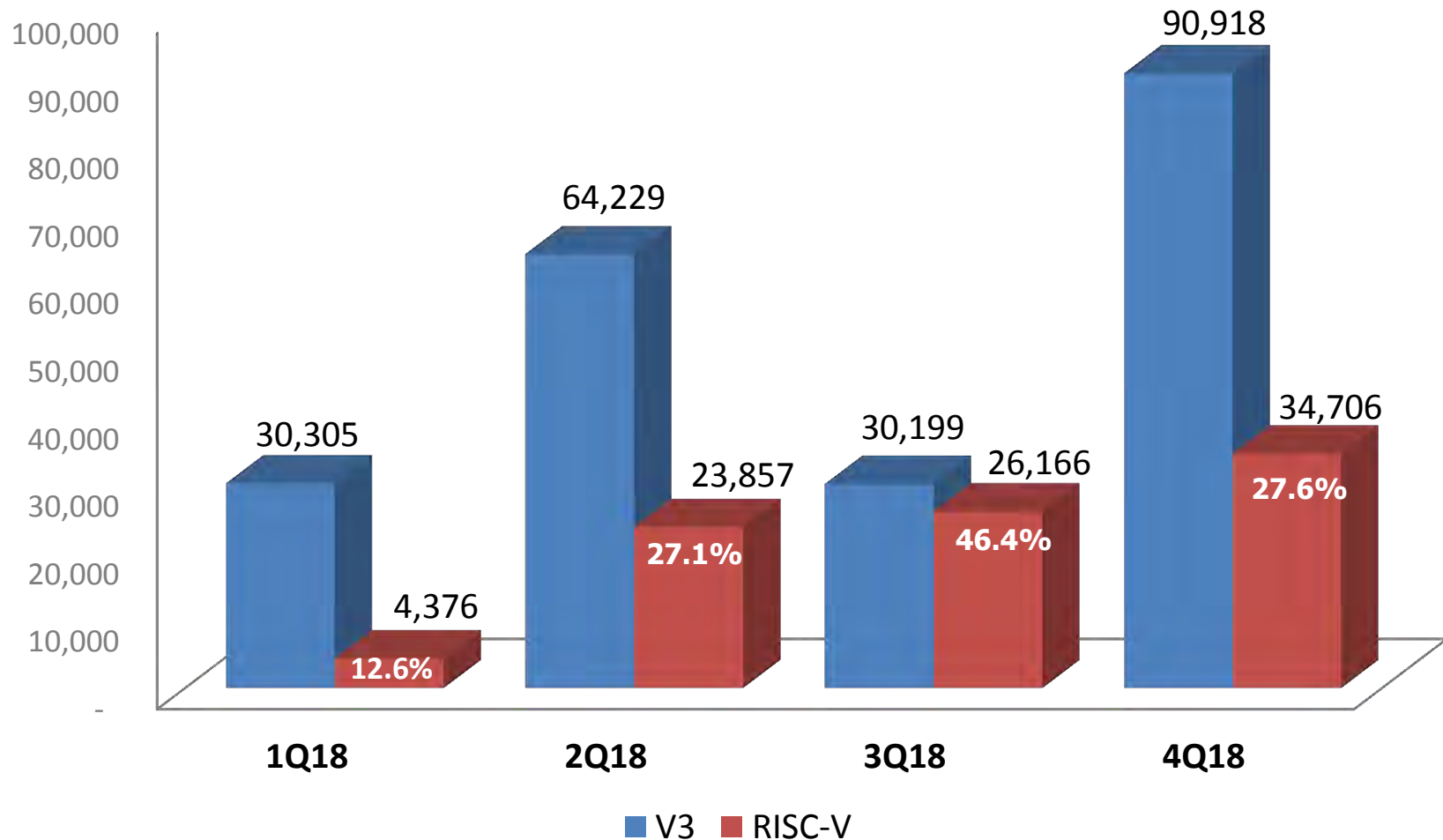


*Based on agreement number

2018 Revenue Analysis - RISC-V



(NT\$ thousands)



Product Application

Andes Update



- ❖ A 14-year-old public CPU IP company
- ❖ >1B Andes-Embedded SoC shipped in 2018. >3.6B cumulatively.



- ❖ A founding member of the RISC-V Foundation
- ❖ A major open source maintainer/contributor
- ❖ Active involvement in standard extensions
 - Chair of P-extension (Packed DSP/SIMD) Task Group
 - Co-chair of Fast Interrupt Task Group

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 - only support RV64-based CPU
- newlib: August, 2017
- "Probably not a compiler bug"

GNU Toolchains

Alex Bradbury is in charge of RISC-V LLVM

- Toolchain (left)
- RV32IM(A)FD support upstream
 - Adding hard float calling convention
 - Adding hard float support
 - Adding compressed support
- Clang, Gcc, and OpenDK have run code
 - Real port is ongoing
 - Impending

LLVM

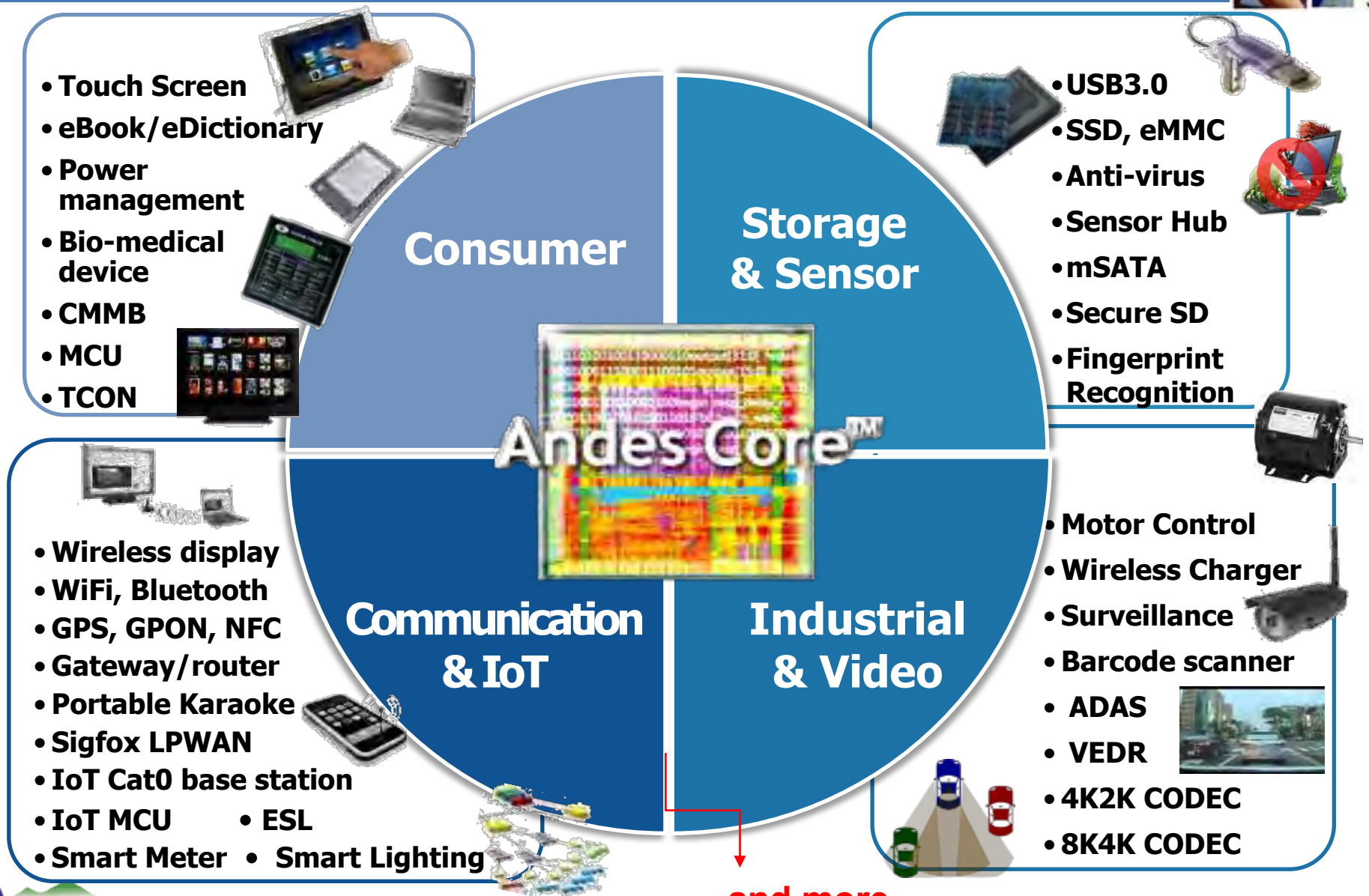
RISC-V Linux Kernel Port

- Linux: January, 2018
 - Only RV64-based systems
 - Drivers are trickling in now

Linux

Logos: SiFive, bluespec, redhat, ANDES TECHNOLOGY, lowRISC, Berkeley

Example Applications of Andes-Embedded™ SoC



and more.....

IoT Application -1



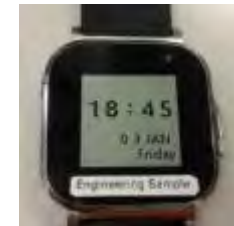
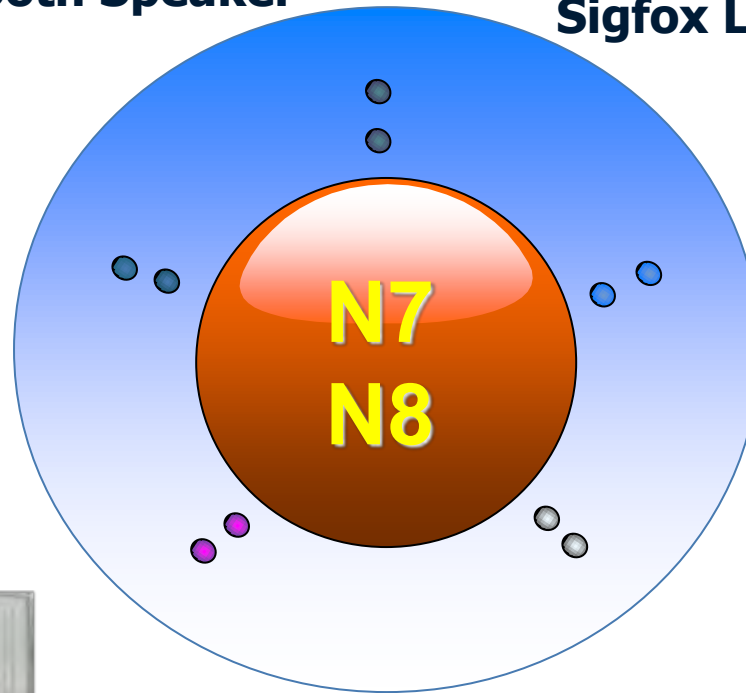
Bluetooth Speaker



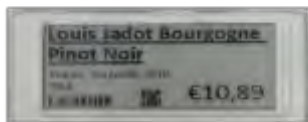
Sigfox LPWAN



Healthcare device



Wearable device



Electronic price tags



Sensor Hub

IoT Application -2



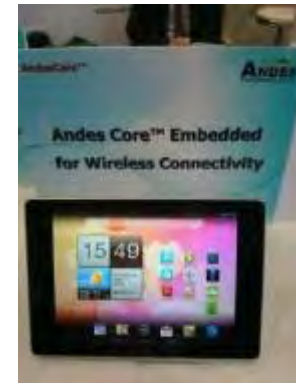
Wearable devices



Drone



Portable Karaoke



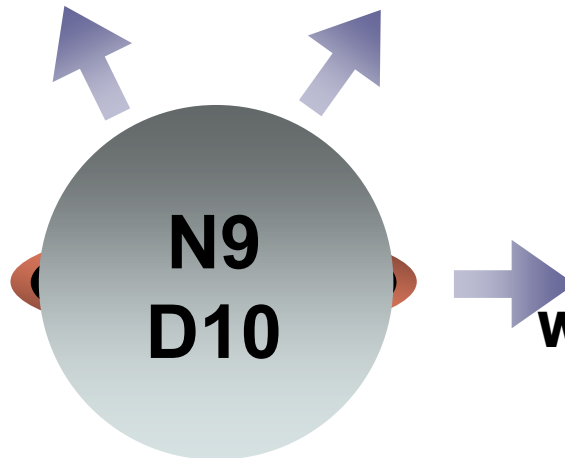
**WiFi/GPS/FM/Bluetooth
combo**



GPS/Beido in shared bikes



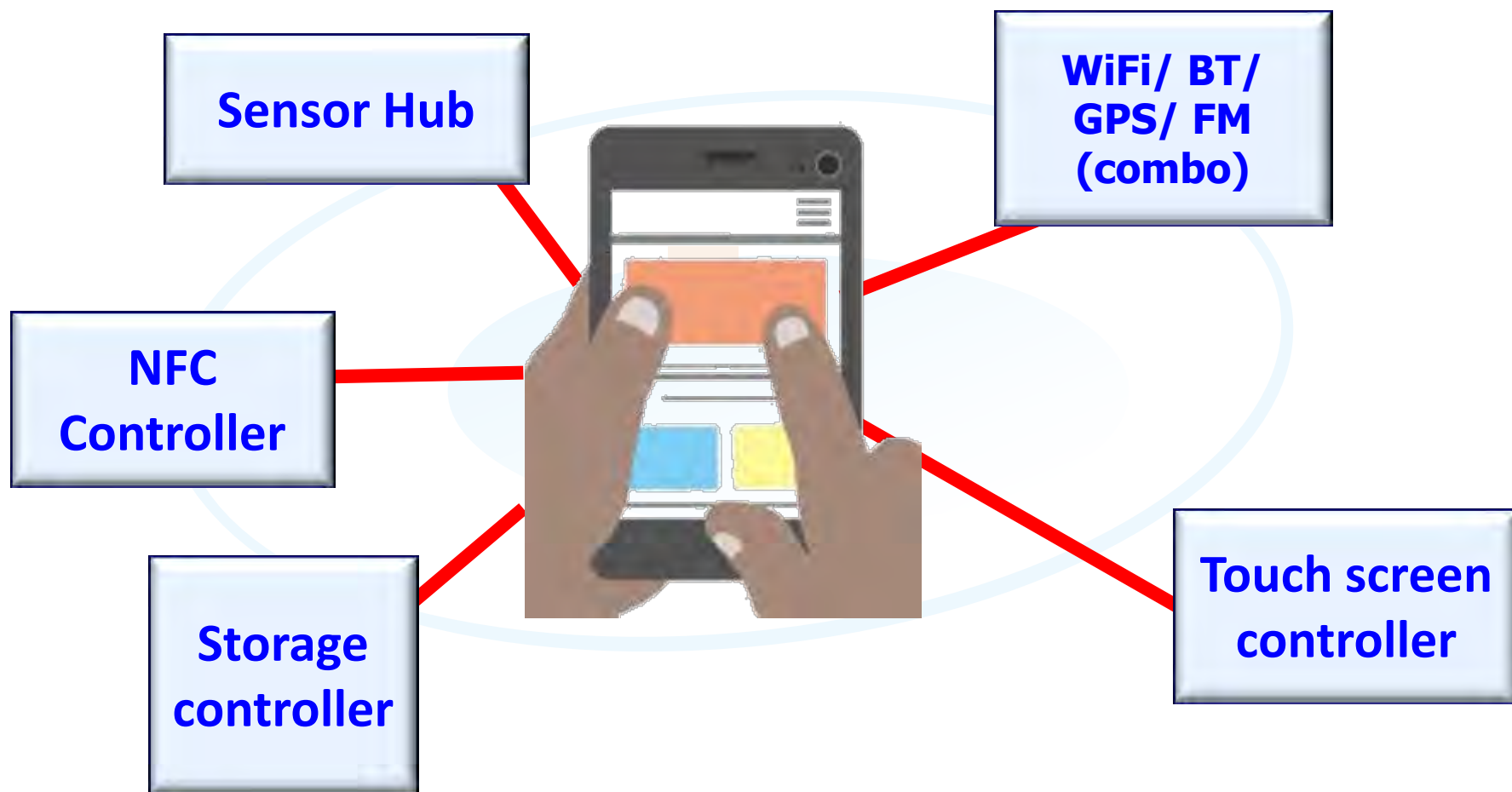
**Contactless payment
(NFC)**





Andes Embedded in Smart Phones

1 in 5 Smart Phones are with Andes Embedded worldwide



Andes Embedded in Consumer Devices, Cars and Datacenters



Switch:
MXIC Flash Ctrl



Echo Dot2:
Mediatek WiFi IoT



Bike Sharing:
GPS Ctrl



X-Trail:
ADAS Ctrl



- ❖ In leading machine learning computers for datacenter
- ❖ In tier-one switch routers for datacenter

- ❖ Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

New Products and Ecosystems

Product Lines



- ◆ New A-series Cores released in Andes Embedded Forum 2018

A N D E S



Andes RISC-V Product Overview



Best extensions to RISC-V

AndeStar™ Architecture V5



Highly optimized
design with
leading PPA

AndesCore™
Processors



Handy peripheral
IPs to speed up
SoC construction



AndeShape™ Platforms

AndeSight™
Tools



Professional IDE
with high code
quality



Extensive SW stacks
from bare metal,
RTOS to Linux

AndeSoft™ Stacks





V5 AndesCore™ Processors

N22

N25F/NX25F

A25/AX25

A25MP/AX25MP

Bring Andes Strength to RISC-V Core Family



- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure

The Latest Product Families



Launch of RISC-V Core IP Series

Cache-Coherent
Multicores



A25MP^a

V5, 32b, 1~4 Cores
L2 Cache Coherence
DSP, MMU, FPU, ACE ...



AX25MP^a

V5, 64b, 1~4 Cores
L2 Cache Coherence
DSP, MMU, FPU, ACE ...

Linux and
FPU/DSP

A25

V5, 32b, 5-stage, >1.2GHz,
MMU/PMP, DSP, FPU, ACE
...

AX25

V5, 64b, 5-stage, >1.2GHz,
MMU/PMP, DSP, FPU, ACE
...

Fast/Compact,
FPU/DSP



D25F: +DSP

N25F

V5, 32b, 5-stage, >1.2GHz
PMP, FPU, ACE...

NX25F

V5, 64b, 5-stage, >1.2GHz
PMP, FPU, ACE...

Slim and
Efficient



N22

V5/V5e, 32b, 2-stage
800MHz, 16/32 GPR

D22F

V5/V5e, 32b, 2-stage
800MHz, 16/32 GPR, DSP,
FPU

a. A25*MP: available Q1/2019

b. 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

V5 AndesCores: 25-series



❖ N25F: 32-bit, NX25F: 64-bit

- From scratch for the best PPA
- Very configurable

❖ AndeStar V5 ISA

❖ 5-stage pipeline

❖ Configurable multiplier

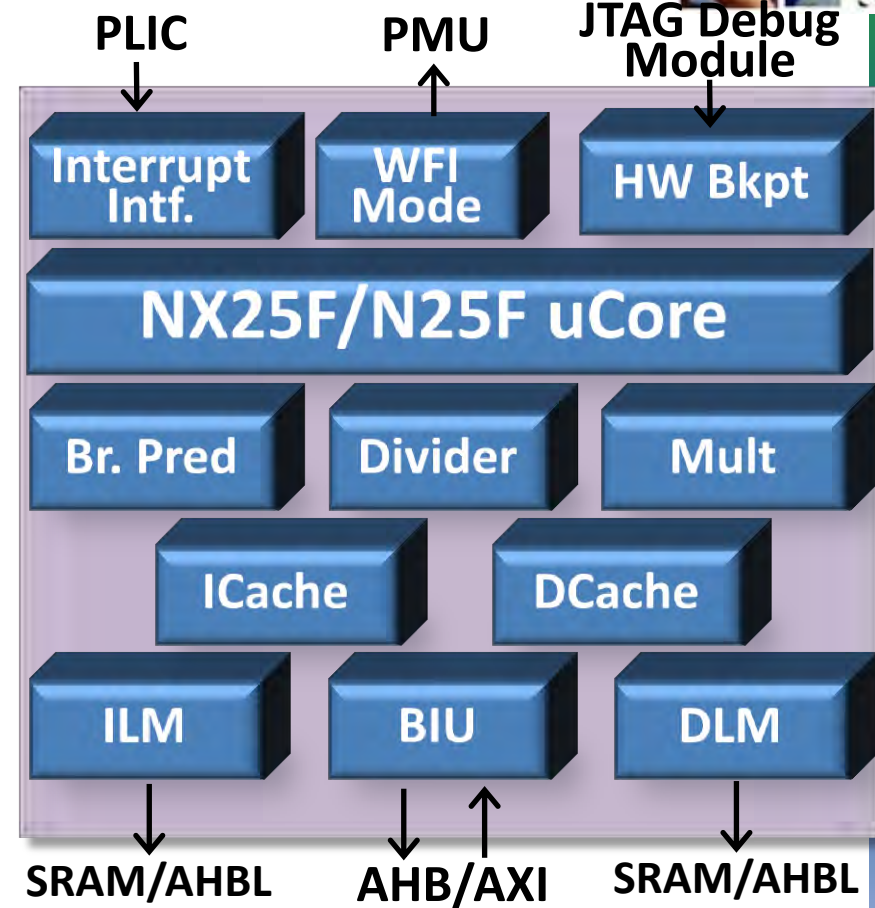
❖ Optional branch prediction

❖ Flexible memory subsystem

- I/D Local Memory (LM): to 16MB
- I/D caches: up to 64KB, 4-way
- Optional parity or ECC
- Hit-under-miss caches
- load/store: unaligned accesses

❖ N25F sample configurations @TSMC 28HPC+ RVT:

- Small config: 37K gates, 1.0 GHz (worst case)
- Large config: 130K gates, 1.2GHz (worst case)
- **Best-in-class Coremark: 3.58/MHz**



V5 AndesCores: 25-series



❖ **Fast-n-small for control tasks in AR/VR, networking, storage, AI**

❖ **N25F/NX25F: +FPU**

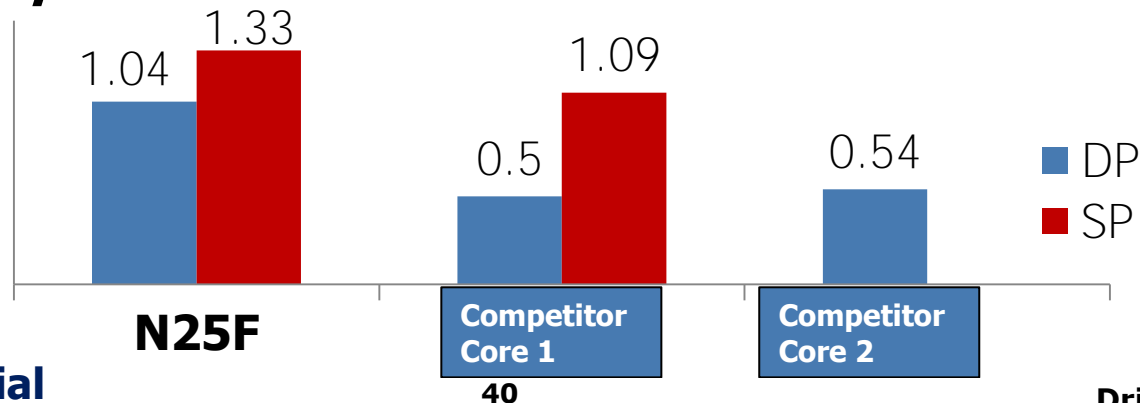
- $+$, $-$, \times , $\underline{x+}$, $\underline{x-}$: pipelined 4 cycles
- \div , $\sqrt{\quad}$: run in the background
 - ◆ 15 for SP, 29 for DP

- FP load/store: support HP

❖ **A25/AX25: +FP +Linux**

- Support RISC-V MMU and S-mode
- 4 or 8-entry ITLB and DTLB
- 4-way 32~128-entry Shared-TLB

❖ **Whetstone/MHz:**



V5 AndesCores: 22-series



❖ AndeStar V5 or V5e ISA

- RV32-IMC or RV32-EMC
- Plus Andes extension

❖ 2-stage pipeline with AHB-lite main bus

❖ Rich baseline options:

- I/D Local Memory (1KB~512MB), I cache
- Fast or small multiplier, branch predictions
- Up to 16-entry PMP, StackSafe
- M-mode, or M+U-mode
- APB private peripheral port, fast IO port
- WFI, WFE, and PowerBrake
- Vectored and preemptive interrupt controller

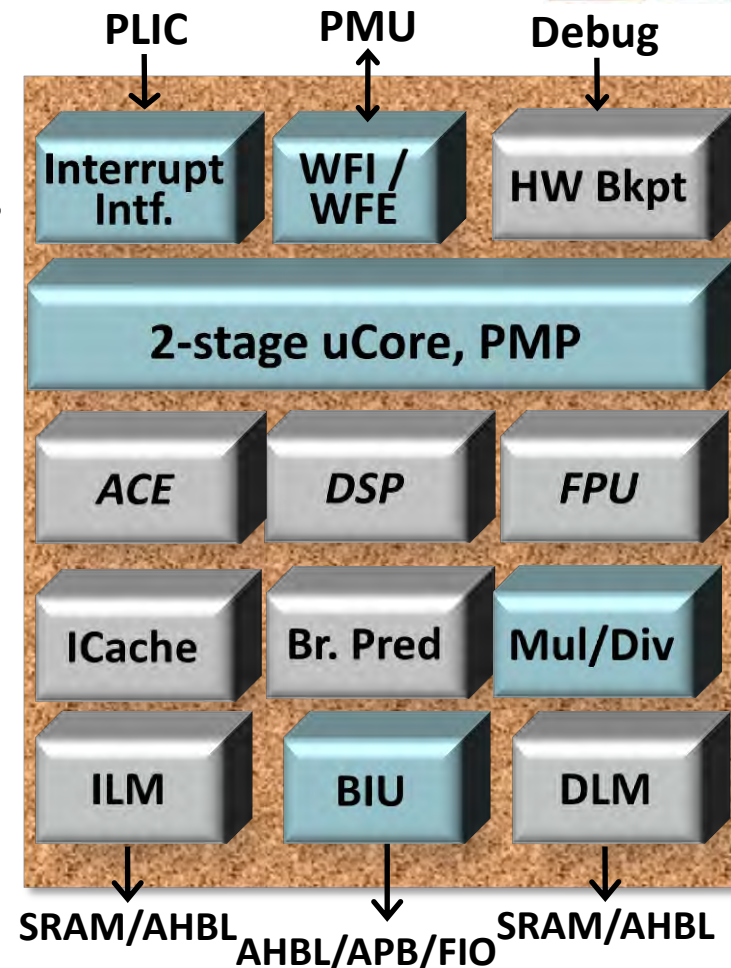
❖ Advanced options: *ACE, DSP, FPU*

❖ 28nm PPA:

- **>750 MHz** (worst case)
- **<15K gates** (minimal)

❖ Best per-MHz performance:

- **1.8 DMIPS** (no inline)
- **3.97 Coremark**



A(X)25MP Cache-Coherent Multicore



❖ 1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs

- RV-IMACFD ISA, supporting SMP Linux
- With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V

❖ Hardware Multicore Cache Coherence

- Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
- Support I/O coherence without data caches

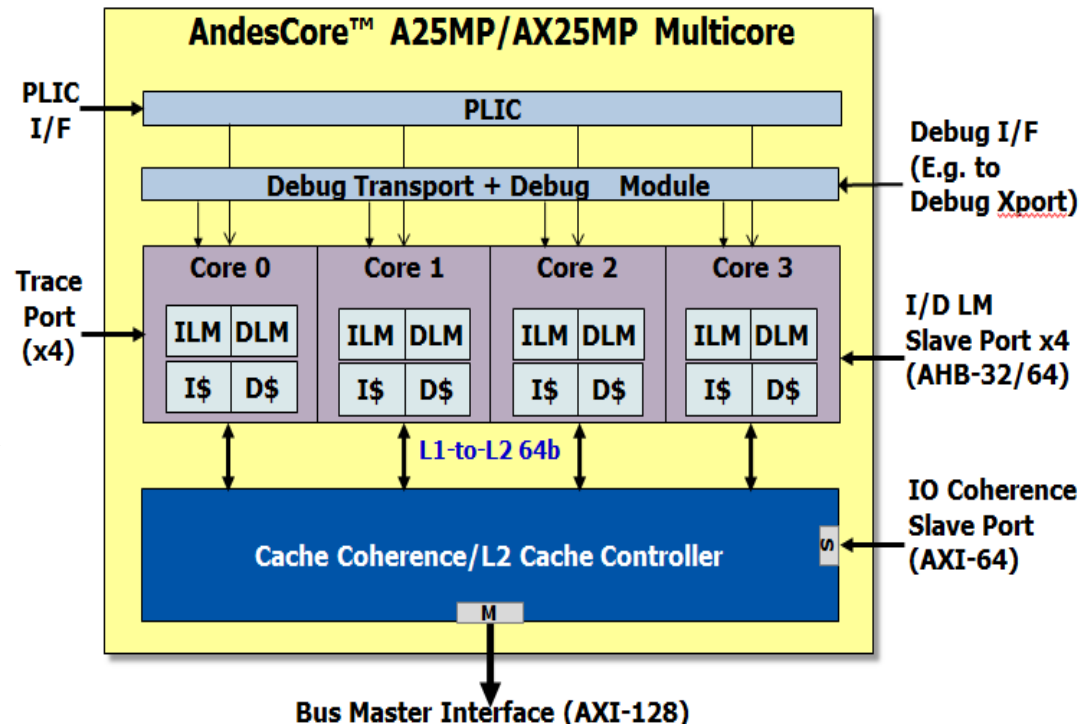
❖ Level-2 Cache Controller

- 0/128/256K...2MB, 32-byte line, 16-way
- ECC, SECDED support

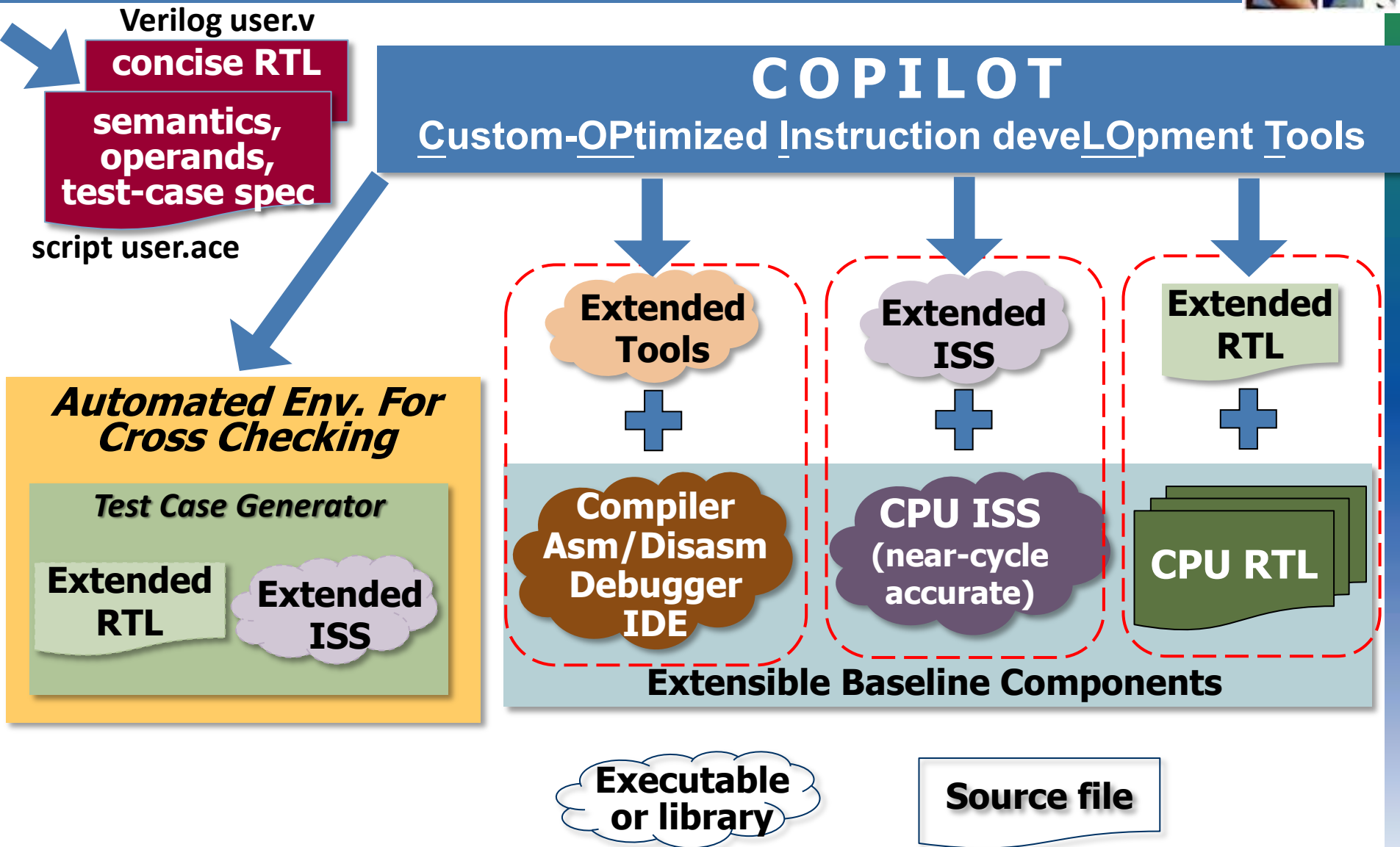
❖ Bus Interfaces

- AXI bus master interface
- Local memory slave port, for each A25/AX25 CPU
- I/O coherence slave port
- MP subsystem vs. bus interface synchronous N:1 clock ratio

❖ Platform Level Interrupt, Debug and Trace Support



ACE: Andes Custom Extension



Aggressive in RISC-V Community



Foundation Task Groups (partial list)



- ❖ **Contributing hardware architecture extensions**
 - Chair of the P-extension (Packed SIMD/DSP) Task Group
 - Co-chair of Fast Interrupts Task Group
 - Closely reviewing activities of other Task Groups

Andes Helps Strengthen RISC-V Ecosystem



- ▶ **More choices for customers are good**
- ▶ **Andes works closely with partners to grow RISC-V ecosystem**



RISC-V Software Ecosystem: GNU Toolchain



- ❖ **GCC, binutils**: May, 2017
- ❖ **Newlib**: Aug, 2017
- ❖ **Glibc (rv64i)**: Feb, 2018
- ❖ **GDB**: Mar, 2018
- ❖ **OpenOCD**: July, 2018
- ❖ **Glibc (rv32i)**:
 - Submitted in July 2018 (by Andes)
 - Review in progress

Barcelona
May 2018

The State of RISC-V Software

GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
- newlib: August, 2017
- "Probably not a compiler bug"

GNU Toolchains

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM
- RV32M/A/FD support upstream
- Clang, Go, and OpenJDK have run code

LLVM

RISC-V Linux Kernel Port

- Linux: January, 2018

Linux

RISC-V Software Ecosystem: LLVM Compilation



❖ LLVM:

- RV32IMAFDC: June, 2018
- Relaxation: May, 2018 (by Andes)
- 64b support: Nov, 2018
- Missing hard-float calling convention

❖ compiler-rt: Mar, 2018

❖ LLD: Aug, 2018 (by Andes)

- Initial port (relocation and TLS) in Oct. 2017
- Dynamic linking review in progress since Oct, 2017
- Missing link-time relaxation

Barcelona
May 2018

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RISC-V Linux Kernel Port

- Linux: January, 2018

LLVM

RISC-V System Software Ecosystem: Linux



- ❖ **U-boot**: Jan, 2018 (by Andes)
- ❖ **Kernel (rv64i)**: Jan, 2018
- ❖ **Key utilities**: (by Andes)
 - Perf: Feb, 2018
 - Kernel Module: May, 2018
 - Ftrace: May, 2018
- ❖ **Kernel (rv32i)**: Jun, 2018 (by Andes)
- ❖ **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)

Barcelona
May 2018

The State of RISC-V Software

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RISC-V Linux Kernel Port

- Linux: January, 2018

Linux

Andes Position in RISC-V



Complete product portfolio

Reliable RISC-V core IP provider

RISC-V cores that run Linux

Extreme low power consumption, high computing efficiency

World's leading Customer-Extension Capable RISC-V Core



2018 RISC-V Design Win



❖ Sixteen design wins for Andes RISC-V Core IPS:

- **NX25:** Enterprise SSD (Taiwan)
- **N25:** AI (China w/ ACE), Blockchain (China), HD-PLC (Japan), SSD (China), Fingerprint (Taiwan), AI (China x2), TDDI (Taiwan), SD/eMMC (Taiwan), Research/Academic (Taiwan x2)
- **N25/AX25:** FPGA for AI (US)
- **AX25:** FPGA for AI (China)
- **A25:** 5G (US), Automotive (Korea)

❖ Thirteen design service providers joined Andes RISC-V Easy Start Program:

- **US x 3, Europe x1, Korea x 1, China x 3, Taiwan x 5**



Summary of AndesCores vs. Competitors



AndesCore™	AndesCore/ Competitor	Competitors
	Power Efficiency ¹ (DMIPS/mW)	
<u>N7</u>	+42%	Cortex-M0+
<u>N8</u>	+43%	Cortex-M3
<u>N9</u>	+43%	Cortex-M3
<u>D10</u>	+48%	Cortex-M4
<u>N13</u>	+185%	Cortex-A5
<u>N13</u>	+45%	Cortex-R4
<u>D15F</u>	+121%	Cortex-M7

1. Power Efficiency is DMIPS/MHz divided by power consumption (mW/MHz) when running Dhrystone.

Two Ecosystems: Andes and Knect.me



Knect.me Ecosystem



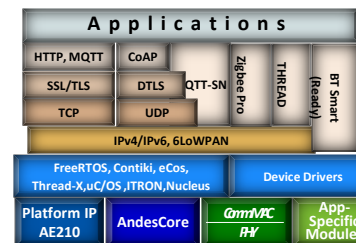
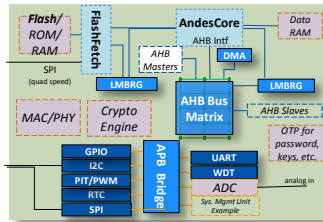
- ❖ **Built up Ecosystem knect.me to help IoT Developing**
 - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products

- ❖ **Includes:**

- SoC IP Platforms
- Software Stack
- Development Boards
- Development Tools

- ❖ **To Form a IoT League**

- to **knect** chip vendors, partners, application developers, system vendors



ectime™



Andes Awarded

Leader of the Emerging Technology



- “2018 Top25 emerging tech solutions provider”
— CIO Advisor Magazine



Concluding Remarks

Andes: Even Better Value in Future



- ❖ Andes revealed new RISC-V processor cores (N22, A(X)25MP, D25F) to fit in more applications from customers.
- ❖ Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.
- ❖ Andes has successively signed thirteen contracts with design service houses in 2018 to authorize ASIC design to embed RISC-V core (Andes RISC-V Easy Start Program). Andes aim to sign up 20 design service houses worldwide in a few months. These contracts will create a win-win situation for Andes, design service houses and customers.

[illegible]

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Q&A